Atmel CPLD Reference Designs Prove Logic Doubling™ Works

White Paper

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Summary

The first section of this paper describes the development of limitations in I/O connectivity and logic reusability in Complex Programmable Logic Devices (CPLDs) over their 20-year history. The second section describes the architectural enhancements (Logic Doubling) in Atmel's ATF15xx Families of CPLDs and how they address these limitations. The third section describes several reference designs that illustrate both the limitations and how Logic Doubling overcomes them and in each case compares Atmel's ATF15xx Families performance to that of typical industry-standard CPLDs.

The programmable logic designer is encouraged to download these reference designs and Atmel's design and fitter software, repeat these experiments and replicate results. Using these examples and tools, the PLD designer can then apply Logic Doubling techniques to new product designs, obtaining the benefits of more features in a smaller, and possibly less expensive chip, or spare logic resources for future revisions and reduced risk of PCB re-spin.

Logic Doubling Background

The first PAL devices in the late 1970's offered a single layer of simple logic: Inputs were routed to an AND/OR block and then to the outputs. PALs had a single, rising-edge CLK pin and a single register OE pin. If more layers of logic were needed, more pins were required.

Although extremely limited by current standards, PALs had two advantages: all I/O signals were available to all logic cells, and relatively little logic was wasted. Each new generation of programmable logic improved on the many other PAL shortcomings but not these two.

Over the first decade, PALs evolved into "CMOS" SPLDs, and the 16V8, 20V8 and 22V10 became standard parts. These devices remained 100 percent connected between the I/O pins and their logic cells. In the following decade, as the logic cells grew in complexity, adding Product Term clocks, multiple OE terms, etc., more of the logic in each cell was potentially left unused in the finished designs. The metric "usable gates" (generally a fraction of about half of the total number of physical gates on the chip) came into use as better way to describe the amount of logic typically accessible for use in a finished design.

However, as the number of macrocells in a single CPLD is increased, the required signal routing area and loading on these nodes also increases according to the square law. The resulting increased die size and speed penalty is simply too great, and so in larger devices all nodes cannot be fed into all macrocells.

As 44-pin CPLDs emerged, new layers of hierarchy were added to their structures. Macrocells were grouped into blocks usually of 16. Output enable functions were added, but often at the logic block level of hierarchy, thus having limited flexibility.

In defining their CPLD architecture, most manufacturers decided to sacrifice connectivity for minimized die size and maximized speed. Fan-in to the blocks became limited, logic utilization took another drop and routing flexibility, both within the macrocells and to the I/O pads, was compromised. The term "pin-locking" was introduced to describe the ability to preassign pins. Lack of pin-locking became a CPLD issue and was debated hotly by leading competitors.

Over the last decade, the CPLD version of Moore's law drove logic density higher. However, routing density, while improving, did not keep pace. The extra fuses and interconnect required to make the increasing amount of unusable logic more accessible would simply take up too much area on the chip, and rather than drive the already high cost of CPLDs even higher, the trend toward inaccessible logic in each macrocell continued.

Likewise, CPLDs still carried the limitation that to have more than one logic layer, another whole macrocell was consumed.

At Atmel, these trends were identified early, and our PLD architects took care to retain as much I/O connectivity and logic reusability as possible, introducing the 100 percent connected ATF1500 with 32 enhanced macrocells in 1996, followed by the ISP family members, ATF1502 with 32 macrocells, ATF1504 with 64 macrocells, and ATF1508 with 128 macrocells. Atmel's commitment to efficient, flexible architecture has continued and this paper will describe the current state of our art. We have coined the term "Logic Doubling" to refer to our efficient, flexible CPLD architecture, now available with second-generation EDA, second-generation fitters and current products as well as the enhanced second generation silicon.

Logic Doubling Theory

Readers already familiar with Logic Doubling concepts may wish to skip this section. Atmel has incorporated a number of features to the ATF15xx Family to address connectivity and reusability problems.

- More cross-point MUXs available for input node fan-in.
- Wider MUX channels into the Logic Blocks.
- Dual, independent feedback paths for each macrocell. The buried and pin-driver feedback paths are split, so a register output may be buried while independently driving a combinatorial pin, or vice versa. Thus, the unused macrocell logic can be accessed and used.
- EVERY macrocell may have separate Output Enable, a feature necessary for software control of data direction and often overlooked by other manufacturers who provide only a few OE terms.
- Selectable Global Clock Polarity, either rising or falling edge.
- Global RESET can combine (OR) with a local Product Term.

Global Routing

The 44-pin, 32-macrocell Atmel ATF1500 CPLD is the patriarch of the ATF15xx Family and provides 100 percent connectivity. The Global bus in the ATF1500 has all input and feedback signals available to all logic blocks, for a fan-in of 68, and the ATF1500 is thus ideal for designs needing maximum fan-in. Because the ATF1500 is 100 percent connected and all the logic cells look the same, most logic changes can be made without touching the pinouts. The 1500 is not immune to pin-locking problems, but it does avoid MUX induced pin shifts. (Atmel also offers the proprietary, 100 percent connected ATF2500, which has 48 registers with 17 product terms per macrocell in a 44-pin package.)

Of course this 100 percent connected approach has scaling issues, and so the rest of the ATF15xx Family devices use the global/regional bus hierarchy for cross-point allocation. Even so, Atmel's CPLDs maintain the highest connectivity of any CPLD Family.

Logic Block Routing and Fan-In

Number of Macrocells	32	32	64	128
Atmel Part Number	ATF1500	ATF1502	ATF1504	ATF1508
Atmel Mux Structure	68 (No MUX)	40 x 5 Matrix x 2	40 x 9 Matrix x 4	40 x 27 x 8
Typical Mux Structure	N/A	36 x 4 Matrix x 2	36 x 8 Matrix x 4	36 x 14 x 8

Because Atmel provides both wider fan-ins than typical, and more cross-points, the ATF15xx Family users have a higher Logic Ceiling (more headroom) for their designs. If you have ever moved up to a larger, costlier device just to get a bit more logic resource, you might have delayed, or avoided that move altogether with the ATF15xx Family.

Macrocell Routing

The following summarizes the Atmel Macrocell signal resources.

Each Macrocell has two main input paths into the five AND type product terms:

- 16 Unipolar Foldback Terms
- 40 Bipolar Signals selected from global pool, by UIM

Each Macrocell has additional inputs:

- 3 Global Clock choices
- 6 Output enable choices
- 1 Global Clear option
- 1 Cascade in, from adjacent MC

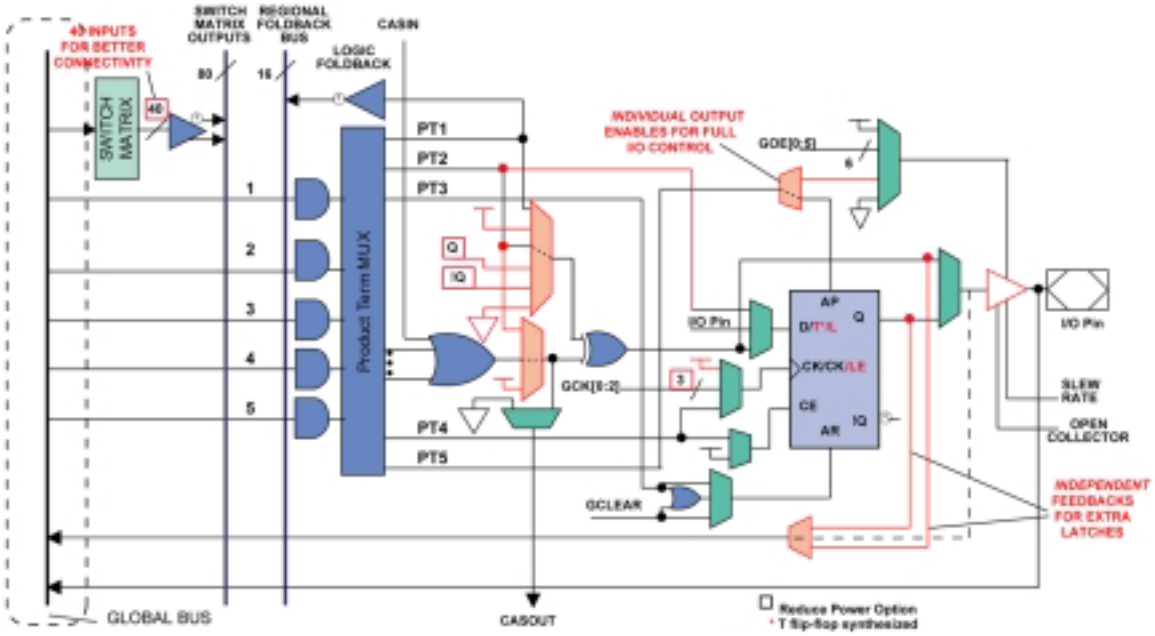
Each Macrocell has four output paths:

- 1 Regional Foldback (16 within each 16-macrocell logic block)
- 1 Buried Feedback (global)
- 1 Pin Drive (global)
- 1 Cascade output, for sharing unused product terms to and adjacent, higher macrocell

Compared to typical CPLDs, the ATF15xx Family provides extra Multiplexers within the macrocell for the register and combinatorial inputs and outputs. This extra routing allows:

1. Toggle flip-flop synthesis.
2. A transparent latch mode for the flip-flop, for ALE style BUS.
3. A buried D-type register, while the remaining combinatorial term drives the PIN.
4. A buried Latch-type register, where LE can be held at logic High, obtaining another combinatorial feedback, while the remaining combinatorial terms drive the PIN.
5. Fast input from the I/O pin.

Atmel Macrocell with Logic Doubling



Clock Resources

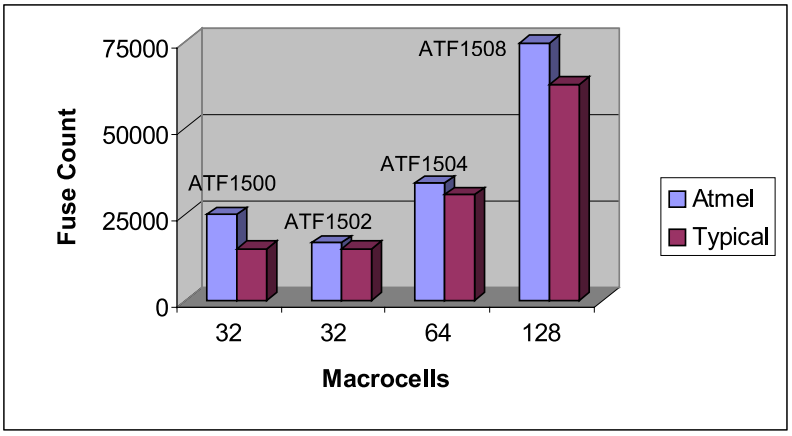
The Atmel ATF15xx Family provides three global clocks, with a choice of rising or falling edge, as well as a local product term clock. One of the global clocks is derived from an I/O pin, allowing a complex, shared clock. Typical CPLDs, from most other suppliers, provide two, with polarity fixed.

I/O Control Resources

Atmel's Logic Doubling architecture also provides an extra Multiplexer, so every macrocell can have it's own output enable. This allows fully soft control of Data Direction on every pin – surprisingly many CPLD families do not offer this.

Fuse Resources

Since fuses control the number of logic choices and paths, more fuses is an indication of more flexibility and usability. For CPLDs that have similar structures, the fuse count is proportionate to the number of resource usage alternatives the device affords, and can be considered a simple "IQ" indicator.



Fitter Capabilities

The second generation Atmel device fitters are designed to take optimal advantage of these Logic Doubling features.

The fitters place and route the design onto a specific Atmel ATF15xx Family device and report results to the designer for review. Besides pinout, the fitters produce a detailed report file that details logic resource usage as well as spare resources remaining for each macrocell. These details allow the designer to see what is going on and make seamless informed design choices as the design progresses.

Note: At the time of this writing, detailed fitter reports were still being enhanced.

Atmel's second generation Atmel ATF15xx Family device fitters support EDIF input (VHDL and Verilog®) as well as legacy PLA formats and produce SDF timing output files. They are fully integrated in Atmel's ProChip Designer™ EDA tool suite with fitter controls to make it easy to pack more features into the chip or to leave additional logic resources for future revisions, reducing the chance of a PCB re-spin.

Verification Capabilities

The SDF output files, when combined with the ATF15xx Family VITAL models, allow the designer to run timing simulations of the final design, including the effects of placement and routing. If a timing problem is detected, the designer can correct it before hardware testing begins. The Accolade PeakVHDL™ simulator is fully integrated in Atmel's ProChip Designer EDA tool suite, so this enhanced verification is easy to include in the design flow.

Logic Doubling Practice: Atmel Reference Designs

So the reader can see how all this stacks up, Atmel has placed these reference designs on it's web site (most CPLD vendors keep them secret) where the designer can easily access them and personally verify our claims.

These reference designs are free, compiler ready, "full chip" designs based on common design problems. Using these reference designs, you can:

- Quickly evaluate how much logic fits into a CPLD.
- Change the template details to suit your system.
- Use them as rapid language training examples.
- Use them as IP, merging their elements with other Logic into a larger Atmel CPLD.
- Anything else you can think of.

Parallel I/O Expander (ATF8255N)

Description

The Parallel I/O expander function is a widely used tool for getting high-bandwidth I/O from microcontrollers and microprocessors. Legacy silicon is still widely used for this, partly because alternatives have come up short. Often these "Legacy" devices are not available in QFP, have limited BUS speeds, and have low-drive capabilities, but there have been few upgrades until now.

Design Summary

To implement a parallel I/O expander, with software control of Port Direction on every pin, a device needs at least 25 OE terms. This design will fit in all ATF15xx Family devices, creating a scalable 82C55 and fits in none of the EPM7XXX devices! Relative to the 146823, the CPLD has much higher pin drive and is MUCH faster.

Enhancements

This design merges the best features of 82C55 and 68230 in that it provides 24 I/O pins, and also individual DDR control on each pin. To keep the pin count down, a Multiplex memory interface is used. The DDR design allows software control of pin types, and suits fully SOFT system designs, where the system software configures the in/out mix, and reprogram of the I/O devices is not needed.

Some Applications Areas

KEYPAD Scan: A single ATF1502 could scan 144 keys, needing just 12 pull-up resistors, or 132 keys + 12 status LED's multiplexed with the KeyScan, etc.

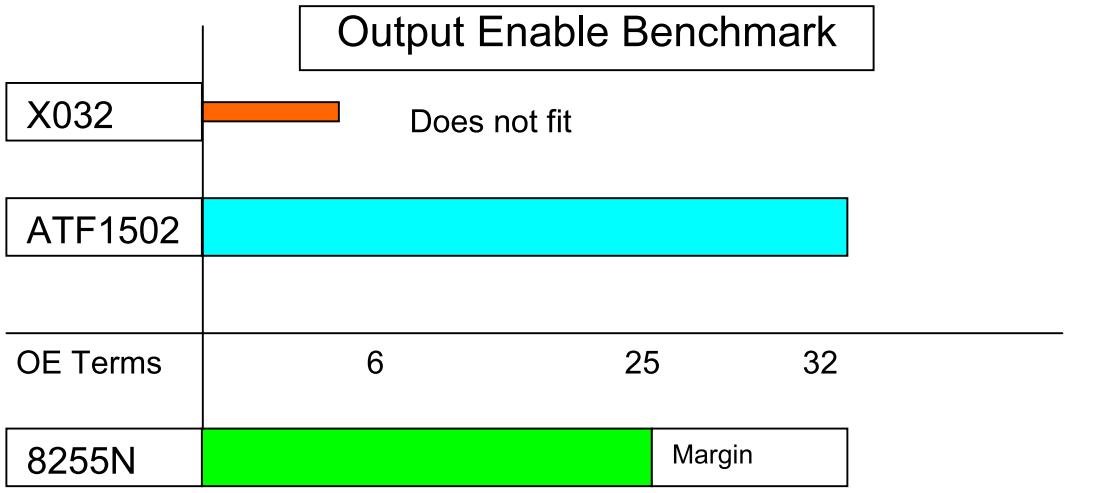
CABLE LOOM TESTERS/PCB bed of nails testers: Looking for OPEN, and Illegal Shorts, and Valid connections. A high speed parallel interface is needed for this, as the required number of nodes goes as the square of the wires. For each Node Write, typically ALL others are READ.

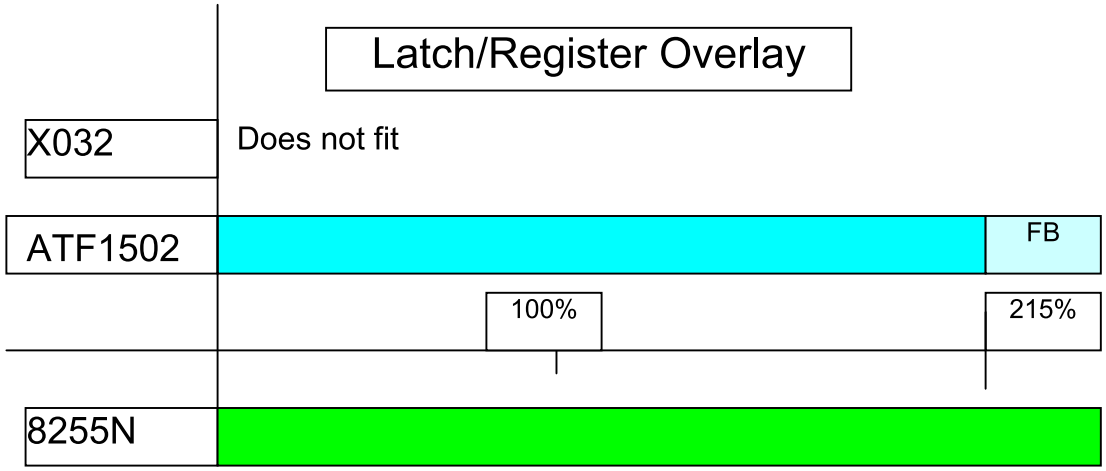
Fast Parallel Memory Interface:

ALE.WRN.RDN.CEN0 – Standard C51 Multiplex BUS Memory interface

DB0..7– Has Address when ALE is high, controlled by RDN, WRN otherwise

Results





Comparative Analysis

The parallel I/O expander simply does not fit in the typical CPLD, due to lack of OE terms.

FIT1502 ATF8255N Fitter Report

```
pin_num pin_name  output_type   feedback foldback cascade_out output_slew
MC1     4    DB0        reg       bAD0        --          --          slow
MC2     5    Pa2        reg       oePa2       NA          --          slow
MC3     6    Pa1        reg       oePa1       NA          --          slow
MC4     7    Pa0        reg       oePa0       NA          --          slow
MC5     8    Pb3        reg       oePb3       NA          --          slow
MC6     9    Pb2        reg       oePb2       NA          --          slow
MC7     11   Pb1        reg       oePb1       NA          --          slow
MC8     12   Pb0        reg       oePb0       NA          --          slow
MC9     13   Pc3        reg       oePc3       NA          --          slow
MC10    14   Pc2        reg       oePc2       NA          --          slow
MC11    16   Pc1        reg       oePc1       NA          --          slow
MC12    17   Pc0        reg       oePc0       NA          --          slow
MC13    18   Pa3        reg       oePa3       NA          --          slow
MC14    19   DB1        reg       GlOE        FbFWrPbL    --          slow
MC15    20   DB2        reg       bAD1        --          --          slow
MC16    21   DB3        reg       FbFWrPaL    FbFWrPcL    --          slow
MC17    41   Pa4        reg       oePa4       NA          --          slow
MC18    40   Pa5        reg       oePa5       NA          --          slow
MC19    39   Pa6        reg       oePa6       NA          --          slow
MC20    38   Pa7        reg       oePa7       NA          --          slow
MC21    37   Pb4        reg       oePb4       NA          --          slow
MC22    36   DB4        reg       HnWrPc      FbFWrPcU    --          slow
MC23    34   Pb6        reg       oePb6       NA          --          slow
MC24    33   Pb7        reg       oePb7       NA          --          slow
MC25    32   Pc4        reg       oePc4       NA          --          slow
MC26    31   Pc5        reg       oePc5       NA          --          slow
MC27    29   Pc6        reg       oePc6       NA          --          slow
MC28    28   DB7        reg       bAD2        --          --          slow
MC29    27   Pc7        reg       oePc7       NA          --          slow
MC30    26   DB6        reg       HnWrPa      FbFWrPaU    --          slow
MC31    25   DB5        reg       HnWrPb      FbFWrPbU    --          slow
MC32    24   Pb5        reg       oePb5       NA          --          slow
MC0     2    ALE        --        --          --          --          slow
MC0     1    CEN0       --        --          --          --          slow
MC0     44   RDN        --        --          --          --          slow
MC0     43   WRN        --        --          --          --          slow

   Array Block    Nodes/MCells  I/O Pins       Foldbacks     Cascades
A: LC1  - LC16    32/16(200%)   16/16(100%)    2/16(12%)     0
B: LC17 - LC32    32/16(200%)   16/16(100%)    3/16(18%)     0

Total dedicated input used:4/4 (100%)
Total I/O pins used32/32 (100%)
Logic Nodes+FB/MCells used69/32 (215%)
Total Foldback logic used 5/32 (15%)
Total cascade used 0
Total input pins 4
Total output pins 32
----------------  End fitter, Design FITS in ATF1502AS
```

Altera ATF8255N (All Devices) Fitter Summary

```
** ERROR SUMMARY **
Error: Project requires too many (25/10) Output Enable signals
```

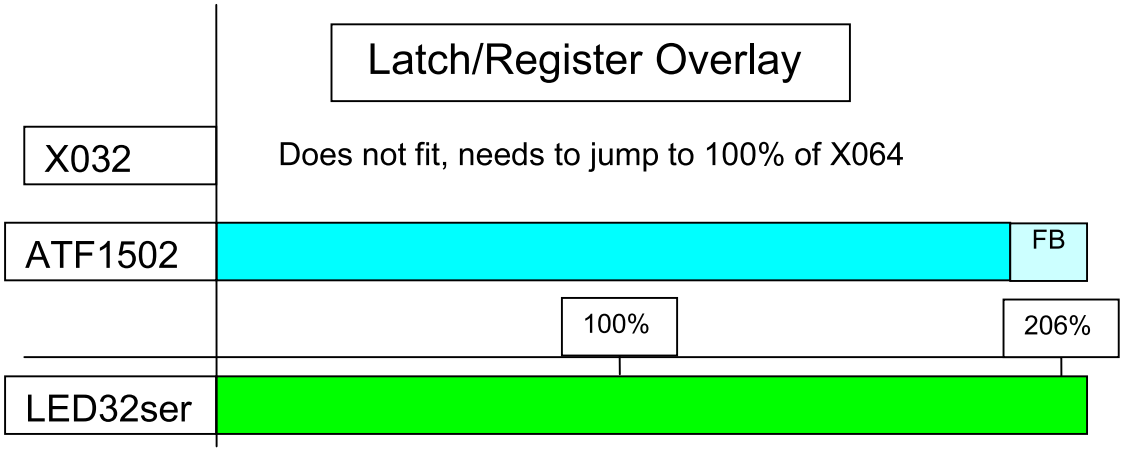
Serial I/O Expander and LED Driver (LED32ser)

Description

Serial I/O expanders like 4094/HC595 are widely used for low bandwidth I/O from microcontrollers and microprocessors. This example uses 100 percent of the CPLD I/O as output drive and so compares directly with these logic devices. More typically a CPLD design would also have some input support.

The CPLD has pin swap and a higher drive than 4094/HC595 devices and the low static I_{DD} of the ATF15xx Family “L” versions means all the package power ability can be used for LED drive. Many other CPLDs have static powers of hundreds of mW.

Results



Comparative Analysis

Currently, this cannot fit into any other 32-macrocell device, one must double the macrocell count to obtain a fit.

FIT1502 LED32Ser Fitter Summary

```
pin_num pin_name output_type feedback    foldback   cascade_out output_slew
MC1   4     IO0        reg       Shift0      --          --            slow
MC2   5     IO1        reg       Shift1      --          --            slow
MC3   6     IO2        reg       Shift2      --          --            slow
MC4   7     IO3        reg       Shift3      --          --            slow
MC5   8     IO4        reg       Shift4      --          --            slow
MC6   9     IO5        reg       Shift5      --          --            slow
MC7   11    IO6        reg       Shift6      --          --            slow
MC8   12    IO7        reg       Shift7      --          --            slow
MC9   13    IO8        reg       Shift8      --          --            slow
MC10  14    IO9        reg       Shift9      --          --            slow
MC11  16    IO10       reg       Shift10     --          --            slow
MC12  17    IO11       reg       Shift11     --          --            slow
MC13  18    IO12       reg       Shift12     --          --            slow
MC14  19    IO13       reg       Shift13     --          --            slow
MC15  20    IO14       reg       Shift14     --          --            slow
MC16  21    IO15       reg       Shift15     FbFollowL   --            slow
MC17  41    IO16       reg       Shift16     FbFollowU   --            slow
MC18  40    IO17       reg       Shift17     --          --            slow
MC19  39    IO18       reg       Shift18     --          --            slow
MC20  38    IO19       reg       Shift19     --          --            slow
MC21  37    IO20       reg       Shift20     --          --            slow
MC22  36    IO21       reg       Shift21     --          --            slow
MC23  34    IO22       reg       Shift22     --          --            slow
MC24  33    IO23       reg       Shift23     --          --            slow
MC25  32    IO24       reg       Shift24     --          --            slow
MC26  31    IO25       reg       Shift25     --          --            slow
MC27  29    IO26       reg       Shift26     --          --            slow
MC28  28    IO27       reg       Shift27     --          --            slow
MC29  27    IO28       reg       Shift28     --          --            slow
MC30  26    IO29       reg       Shift29     --          --            slow
MC31  25    IO30       reg       Shift30     --          --            slow
MC32  24    IO31       reg       Shift31     --          --            slow
MC0   2     DATI       --        --          --          --            slow
MC0   1     CSEL       --        --          --          --            slow
MC0   44    BPlane     --        --          --          --            slow
MC0   43    CLK        --        --          --          --            slow

Array Block       Nodes/MCells  I/O Pins       Foldbacks     Cascades
A: LC1  - LC16    32/16(200%)   16/16(100%)    1/16( 6%)     0
B: LC17 - LC32    32/16(200%)   16/16(100%)    1/16( 6%)     0

Total dedicated input used:4/4 (100%)
Total I/O pins used32/32 (100%)
Logic Nodes+FB/MCells used66/32 (206%)
Total Foldback logic used 2/32 (6%)
Total cascade used 0
Total input pins 4
Total output pins 32
----------------  End fitter, Design FITS in ATF1502AS
```

Altera (7032) Fitter Summary

```
Led32ser ** ERROR SUMMARY **
Error: Project requires too many (64/32) logic cells
```

Altera (7064) Fitter Summary

```
Total dedicated input pins used:                 4/4      (100%)
Total I/O pins used:                            32/32     (100%)
Total logic cells used:                         64/64     (100%)
Total shareable expanders used:                  0/64     (  0%)
Total Turbo logic cells used:                   64/64     (100%)
Total shareable expanders not available (n/a):  32/64     ( 50%)
Average fan-in:                                  3.00
Total fan-in:                                   192
```

Pulsewidth Modulator (PWM8x4)

Description

This design packs the maximum number of 8-bit resolution DACS, and PWM modulators, into a 44-pin PLCC 32-macrocell device.

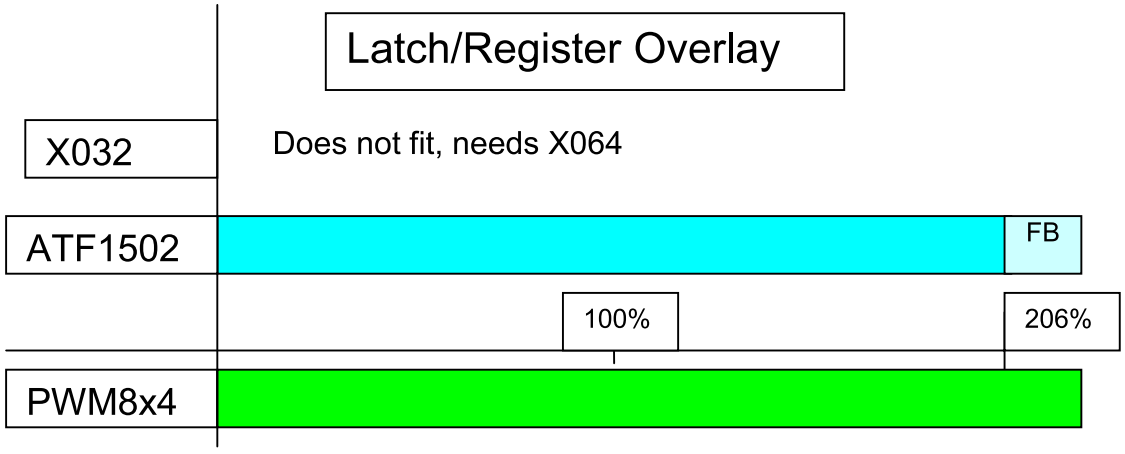
Pulse width modulation is often used for digital-to-analog conversion (with an output filter) and to drive Motors and Solenoids efficiently using switched mode.

Using the Logic Doubling, an ATF1502 can swallow four 8-bit PWM generators and their Value Latches.

The design has an 8-bit microcontroller BUS interface for write of the PWM values.

The circuit can run at full Clock Speed and has special trap for SetPoint of 0, so the output remains DC low when stopped. If always having a waveform is important to the application, removing the trap can force 1/256 to both 0 and 1. Typical add-on features could be a FAST protect reset, if Motor Driving, or system RESET input, to define the PWM output at reset.

Results



Comparative Analysis

PWM8X4 cannot fit into a typical 32-macrocell device, roughly double the macrocell count is required.

FIT1502 PWM8x4 Fitter Summary

```
pin_num pin_name output_type feedback    foldback   cascade_out output_slew
MC1   4     CEN         reg       PwCtr0       --         --           slow
MC2   5     WRN         reg       PwCtr1       --         --           slow
MC3   6     DB4         reg       PwmA6        --         --           slow
MC4   7     Adr1        reg       PwCtr3       --         --           slow
MC5   8     PwmD6       reg       PwCtr4       --         --           slow
MC6   9     PwmD7       reg       PwCtr5       --         --           slow
MC7   11    PwmC6       reg       PwCtr6       XXL_257    --           slow
MC8   12    PwmC7       reg       PwCtr7       XXL_256    --           slow
MC9   13    PwmAOUT     reg       --           XXL_255    --           slow
MC10  14    PwmBOUT     reg       --           XXL_254    --           slow
MC11  16    DB0         com       NEqB0_4      NA         --           slow
MC12  17    DB1         com       NEqA0_4      NA         --           slow
MC13  18    --          reg       PwmB6        fbWrPwmC   --           slow
MC14  19    --          reg       PwmB7        fbWrPwmD   --           slow
MC15  20    DB6         reg       PwCtr2       fbZeroAN   --           slow
MC16  21    DB7         reg       PwmA7        fbZeroBN   --           slow
MC17  41    PwmC0       reg       PwmA0        WrPwmCN    --           slow
MC18  40    PwmC1       reg       PwmA1        WrPwmDN    --           slow
MC19  39    PwmC2       reg       PwmA2        --         --           slow
MC20  38    PwmC3       reg       PwmA3        --         --           slow
MC21  37    DB2         com       NEqC0_4      NA         --           slow
MC22  36    PwmC5       reg       PwmA5        --         --           slow
MC23  34    PwmC4       reg       PwmA4        --         --           slow
MC24  33    DB3         com       NEqD0_4      NA         --           slow
MC25  32    PwmD0       reg       PwmB0        XXL_253    --           slow
MC26  31    PwmD1       reg       PwmB1        XXL_252    --           slow
MC27  29    PwmD2       reg       PwmB2        XXL_251    --           slow
MC28  28    PwmD3       reg       PwmB3        XXL_250    --           slow
MC29  27    PwmD4       reg       PwmB4        fbWrPwmC   --           slow
MC30  26    PwmD5       reg       PwmB5        fbWrPwmD   --           slow
MC31  25    PwmCOUT     reg       --           fbZeroCN   --           slow
MC32  24    PwmDOUT     reg       --           fbZeroDN   --           slow
MC0   2     DB5         --        --           --         --           slow
MC0   1     Reset       --        --           --         --           slow
MC0   44    Adr0        --        --           --         --           slow
MC0   43    CLK         --        --           --         --           slow

Array Block         Nodes+FB/MCells  I/O Pins      Foldbacks     Cascades
A: LC1- LC16       20/16(125%)14/16(87%)  8/16(50%)0
B: LC17- LC32       28/16(175%)16/16(100%)   10/16(62%)0

Total dedicated input used:4/4 (100%)
Total I/O pins used30/32 (93%)
Logic Nodes+FB/MCells used66/32 (206%)
Total Foldback logic used 18/32 (56%)
Total cascade used 0
Total input pins 14
Total output pins 20
----------------  End fitter, Design FITS in ATF1502AS
```

Altera PWM8x4 (7032) Fitter Summary

```
pwm8x4  ** ERROR SUMMARY **
Error: Project requires too many (48/32) logic cells
```

Altera PWM8x4 (7064) Fitter Summary

```
Total dedicated input pins used:                 2/4      ( 50%)
Total I/O pins used:                            32/32     (100%)
Total logic cells used:                         48/64     ( 75%)
Total shareable expanders used:                  9/64     ( 14%)
Total Turbo logic cells used:                   48/64     ( 75%)
Total shareable expanders not available (n/a):   8/64     ( 12%)
Average fan-in:                                  7.39
Total fan-in:                                   355
```

Latch for Multiplex BUS (LatchSyn)

Description

This modular example demonstrates ways to synthesize a Transparent Latch, commonly used in Multiplex BUS system, so you can place a HC573/373 into a corner of your CPLD, and save PCB real estate. The macrocell of the ATF15xx family offers options on the method used to create a transparent latch:

- Use the macrocell .L, LE support directly.
- Use a make-before-break 2:1 MUX, using the PIN Feedback.
- Use a .D register, like a -ve clock HC374/574.

This file implements both and packs both into one macrocell as a demonstration. In a real system, one can choose to bury some address terms, or drive all 8 to Pins, and bury 8-D registers in the same macrocells. Besides the pins used, the HC573/373 can have minimal impact on the LOGIC used, and give a significant PCB area saving, and better security.

FIT1502 LatchSyn Fitter Summary

```
pin_num pin_name output_type feedback    foldback    cascade_out output_slew
MC1   4     uDB0       reg         --          --          --             slow
MC2   5     uDB1       reg         --          --          --             slow
MC3   6     uDB2       reg         --          --          --             slow
MC4   7     uDB3       reg         --          --          --             slow
MC5   8     uDB4       reg         --          --          --             slow
MC6   9     uDB5       reg         --          --          --             slow
MC7   11    uDB6       reg         --          --          --             slow
MC8   12    uDB7       reg         --          --          --             slow
MC9   13    PinL0      reg         StdL0       --          --             slow
MC10  14    PinL1      reg         StdL1       --          --             slow
MC11  16    PinL2      reg         StdL2       --          --             slow
MC12  17    PinL3      reg         StdL3       --          --             slow
MC13  18    PinL4      reg         StdL4       --          --             slow
MC14  19    PinL5      reg         StdL5       --          --             slow
MC15  20    PinL6      reg         StdL6       --          --             slow
MC16  21    PinL7      reg         StdL7       --          --             slow
MC17  41    --         com         PinLFollowN --          --             slow
MC18  40    --         --          --          --          --             slow
MC19  39    --         --          --          --          --             slow
MC20  38    --         --          --          --          --             slow
MC21  37    --         --          --          --          --             slow
MC22  36    --         --          --          --          --             slow
```

```
MC23   34     --          --          --          --          --          slow
MC24   33     --          --          --          --          --          slow
MC25   32     DLat0       reg         --          --          --          slow
MC26   31     DLat1       reg         --          --          --          slow
MC27   29     DLat2       reg         --          --          --          slow
MC28   28     DLat3       reg         --          --          --          slow
MC29   27     DLat4       reg         --          --          --          slow
MC30   26     DLat5       reg         --          --          --          slow
MC31   25     DLat6       reg         --          --          --          slow
MC32   24     DLat7       reg         --          --          --          slow
MC0    2      --          --          --          --          --          slow
MC0    1      --          --          --          --          --          slow
MC0    44     RDN         --          --          --          --          slow
MC0    43     ALE         --          --          --          --          slow

-----------  End fitter, Design FITS in ATF1502AS
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Conclusion

Atmel's ATF15xx Family of CPLDs provides enhanced I/O connectivity and logic utilizability. Atmel's Logic Doubling architecture combined with Atmel's second-generation device fitters, extends CPLD place and route efficiency. For example with double independent buried feedback designers can pack more logic (particularly shifters and latches) into smaller CPLDs. This stretching of CPLD resources in some cases increases the nominal register/latch count to 200 percent or more. The more flexible routing and denser packing of logic enables the designer to use a smaller, often less costly device or leave spare room for later design revisions at no additional design effort.