

## Discussion

Chip Diode devices for use in integrated circuits and hybrid integrated circuits have proliferated in the last few years. Today circuit designer is faced with a multiplicity of alternatives in the involving tradeoffs of particular advantages and disadvantages. The obvious advantages in the use of chip diodes in hybrid integrated circuit applications are their very small size and potentially lower cost. Small size and simplicity of structure give the benefit of minimal parasitics, but as the size of the diode becomes smaller, handling and production problems increase. By outlining our conclusions, we hope to help the designer overcome some of the difficulties encountered when using chips in MIC applications. M/A-COM Tech manufactures a large selection of chip and packaged diodes for hybrid integrated circuits. Obviously not all diode types are available in all configurations. Characteristics such as breakdown voltage or capacitance may limit the size of the chip or its form.

### Silicon Chip Devices

- CERMACHIP™ PIN Diodes
- Oxide Passivated PIN Chips
- Beam Lead PINs
- Snap Varactor Chips
- Tuning Varactor Chips
- MNS Chip Capacitors
- Schottky Chips
- Beam Lead Schottky Diodes
- PF transistor Chips (Low Noise)

### Silicon Chip Devices

- Gunn Diodes
- GaAs Tuning Varactors
- Beam lead GaAs Tuning Varactors
- GaAs Multipliers
- GaAs Schottky Mixers
- GaAs Abrupt and Hyperabrupt Tuning Varactors
- GaAs Beam lead Schottky

## Microstrip Packages and Chip Carriers

Chip diodes usually require specialized equipment for die attachment to the circuit and for wire or strap bonding to the top of the chip. These operations require a clean work environment and special handling equipment such as vacuum pickups, hot gas bonders and/or thermal compression bonding equipment.

Not all MIC circuits require chips. In many cases (especially for conventional stripline circuits) a hybrid circuit package or carrier will give satisfactory results and can be handled much more easily without a large investment in fabrication equipment. M/A-COM Tech supplies a broad band of diodes in stripline or carrier packages.

## Chip Bonding Methods

The biggest problem in using chip diodes is the damage encountered when assembling chips into circuits. In general, the value of the integrated circuits far exceeds the cost of the chip itself. When packaged diodes are used, the critical die attach and top contact operations are performed by M/A-COM tech and all devices are RF tested after assembly into the package. When the circuit fabricator performs the die attach and wire bonding operation on a complex substrate, he /she runs the risk of losing or damaging a chip during the bonding operation which can result in the loss of the whole circuit or in an expensive rework cycle.

The most common problems that arise when bonding chips to the circuit are: the introduction of excessive series resistance, especially under forward bias conditions due to the improper bonding of the chip to the ground plane; poor reliability due to the entrapment of fluxes under the bond; and mechanical failure of the bond under thermal shock or temperature cycling. All three conditions are the results of improper wetting of the die to the ground plane and are usually caused by inadequate cleanliness or inadequate bonding conditions,

## The Influence of the Circuit Board on Chip bonding Methods

Selection of the chip bonding method must take into consideration the characteristics of the circuit board material being used.

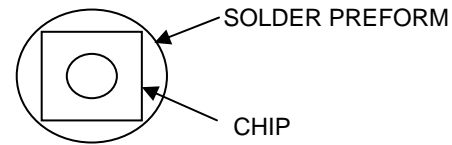
Stripline teflon fiberglass circuits should be soft soldered. Most eutectic solders melt at temperatures too high (250-300°C) to be used with teflon fiberglass boards. Conductive epoxies can also be used, but the results may not be reliable. The use of Gunn diodes on teflon fiberglass circuits is not recommended because the major problem in operating these diodes is removal of heat. It is absolutely essential that eutectic solders or thermal compression bonding be used to bond these diodes to achieve the best thermal resistance. Soft solders and conductive epoxies are not acceptable methods for bonding Gunn diodes. The use of beam lead diodes with teflon fiberglass boards is not generally recommended. Because these boards are flexible, they may bend during or after bonding and cause the diode leads to break.

In many cases conductive epoxies will give good results with little or no complex equipment required. Although the high temperature and long term reliability of this type of bond is not generally as good as eutectic solder, the use of conductive epoxies is an acceptable and simple way to fabricate most circuits.

## Bonding, Handling, and Mounting Procedures for Chip Diode Devices

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Soft solders, such as the eutectic composition of antimony or lead tin, give excellent reliability and good high temperature characteristics. The use of flux for soldering is not recommended at any time. Instead, a cover gas such as a forming gas (80% N<sub>2</sub>, 20% H<sub>2</sub>, or 95% N<sub>2</sub>, 5% H<sub>2</sub>) should be used. When applicable, probably the best die down procedure is an ultrasonic silicon gold thermal compression bond or a high temperature eutectic solder (such as gold tin eutectic— 80% Au, 20% Sn) with a melting point of approximately 280°C.



### Chip Die Down Bonding Techniques

#### Hot Gas Bonding of Chips

The hot gas bonder is one of the most convenient ways of bonding chips onto a metal ground plane or circuit. Both silicon and GaAs may be bonded using similar techniques.

GaAs is brittle and softer than silicon. The use of gold tin solder perform (80% Au, 20% Sn) with an eutectic melting point of 280°C is recommended. A clean, gold plated surface is required to insure good wetting. The perform should be large enough to insure that the die fits within the area shown. The perform should be ~1 mil thick.

The heating stage should be set at 250 ± 5°C. An 80% N<sub>2</sub>, 20% H<sub>2</sub> forming gas is effective as the hot gas jet. The temperature at the tip should be approximately 400°C. The wetting time after the solder reflow is critical for strong bonding. It should be carefully controlled; 3 sec ± 1 sec. If done correctly, the shear strength of a 10 X 10 mil die will average 250-300 grams.

#### Ribbon and Wire Attachment

It is recommended that thermo-compression bonding be used. The bonding tip should be smaller than the anode contact. The exact conditions will depend on the tool types used. It is recommended that a half hard gold wire or strap be used. The wire or strap diameter should be smaller than the diameter of the anode contact. Typical bonding force should be 20 to 15 grams, and should not exceed 30 grams. When wire bonding, a thermal compression wedge bonder is recommended using a heated stage and heated tip. The stage temperature should be ~ 240°C ± 10°C and the recommended temperature for the tip is 120°C. Ultrasonic scrubbing is not recommended.

#### Furnace Solder of Dice

A moving belt furnace is also an excellent method for soldering chips. A belt furnace with an 80-20 forming gas atmosphere and nitrogen curtains on the ends of the furnace is recommended. All parts should be clean and free of oil and grease.

The temperature and speed of the belt should be adjusted so that the parts reach ~ 25-50°C over the melting point of solder for a period of 2 to 5 minutes. Adequate tooling and furnace temperatures are usually necessary to obtain good alignment. "Clean" gases are also very important. The criteria for acceptable solder die is shown on the following page.

Die Down Method	Resultant Thermal Resistance	Temperature Required	High Temperature Capabilities	Power Handling Capability	Ease of Operation	Special Equipment Required	Potential Problems
Conductive Epoxy	Good with proper technique	Room temp to 150°C	Good	Low to medium power	Easiest to apply	Little to none	High series or thermal resistance
Soft solder i.e., Pb-Sn-Ag (90,5,5) Pb-Sn (60,40)	Good to very good	200 - 280°C 180 - 200°C	Good	Good to very good for low or high power	Simple application	Heated stage hot gas bonder or gas curtain and furnace	Flux is usually required with lead solders. Cleaning of flux must be done carefully
Eutectic Solder Au-Sn (80,20) Sn-Sb (97,3)	Very good	Approx. 300°C Approx. 230°C	Good	Very good	Simple application	Heated stage or hot gas bonder	Needs clean reducing atmosphere
Gold silicon Eutectic (Thermal Compression Bond)	Very good	Approx. 380°C	Good	Very good	Most difficult	Ultrasonic bonder with heated stage & tip preferable	Cleanliness, proper bonding conditions

2

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## Chip Die Down Bonding Techniques (Cont'd)

### Ultrasonic thermal Compression bonding of Dice

In a small circuit, ultrasonic bonding gives a very reliable and strong bond. The die should be free of oxides and have no metallization. The bonding surface should have ~2.5 micrometers of a soft gold, preferably from a high cyanide gold bath.

The stage of the bonder should be set at ~ 200-250°C and the bond pressure ~ 400 grams / mm<sup>2</sup>

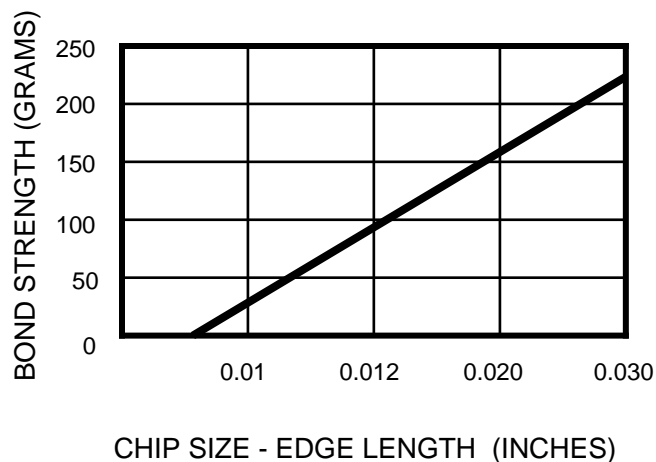
i.e.: ~ 50 grams for 0.010 X 0.010 inch die  
~ 200 grams for 0.020 X 0.020 inch die  
~ 300 grams for 0.030 X 0.030 inch die

These values can vary rather widely and some experimentation may be necessary to find the best results.

The criteria for a good thermal compression bond should be the same as for a soldered joint.

### Die Bonding with Conductive Epoxies

Although some military and telecommunications systems do not allow the use of conductive epoxies, satisfactory die down bonds may be obtained using these epoxies. The following precautions should be observed to obtain consistently strong bonds.



### Cleanliness

Everything should be clean and degreased. It is a good idea to clean the circuit in an alkaline solution to remove any traces of plating solutions. The circuit should then be degreased.

### Shelf Life

The conductive epoxy must be within the warranty shelf and/or pot life. It is advisable to use one half the listed pot life since manufactures tend to be optimistic on pot life estimates. Thus, if the pot life is stated to be 2 days, it is much safer to use new epoxy every day.

### Curing

The epoxy must be cured in the air or in an oxidizing atmosphere. The reaction requires oxygen. The epoxy oven should be clean (not used for other functions) and should have a good air flow to carry fumes. The epoxy will not cure well if there are other solvent fumes in the atmosphere.

### Carrier Fluid

The carrier fluid must not be allowed to flow on the top of the chip. Not only will it make the chip unbondable, it will be almost virtually impossible to detect under normal bonding procedures. If a vacuum tip is used to put the chip in place remove the vacuum when the chip is 10 to 30 mils from the epoxy. Static charge will hold the chip to the tip. If the vacuum tip touches the epoxy it will become coated with epoxy carrier fluid and contaminate the next chip with the carrier material. This same problem may occur with the use of tweezers. The tweezers should be cleaned before pickup another chip if they touch the epoxy.

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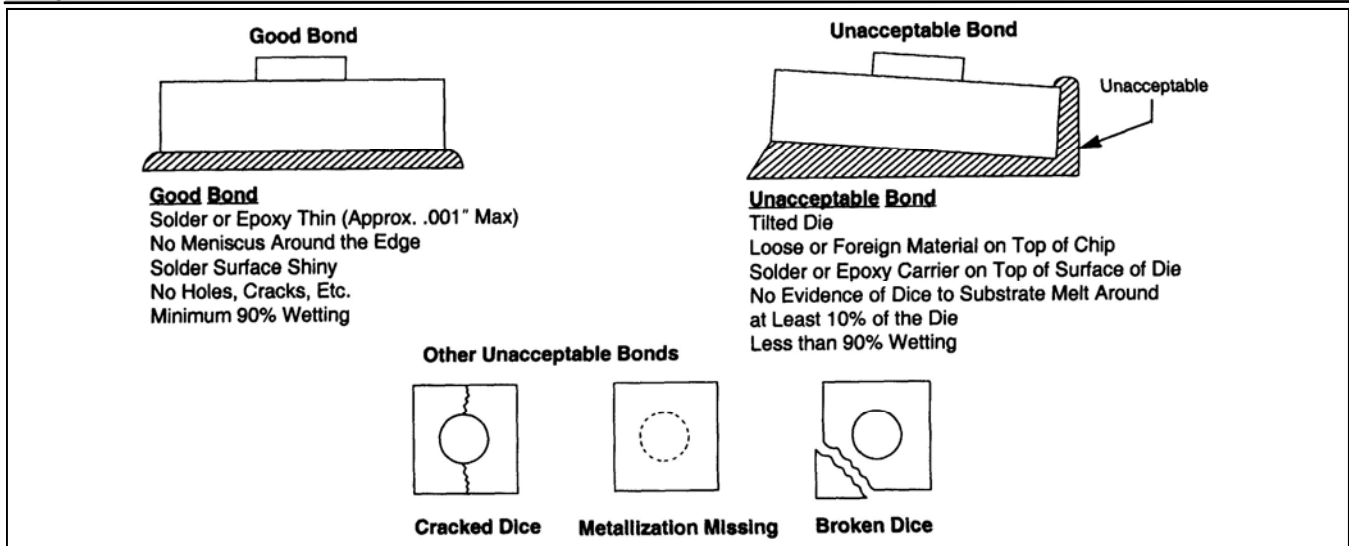


Figure 3. Die Bonding Criteria

Table 2. Visual Inspection for Good Die-Down Bonds (Using a 5-15x Microscope)

Die Down Method	Visual (Good Bond Criteria)	Typical Bond Strength (In Stress)	Extra R <sub>s</sub> From <sup>1</sup> Die Down (0.020" Chip)
Conductive Epoxy	Flat and max epoxy thickness ~0.001 inch - 90% min wetting	~ 50-100 kgms/cm <sup>2</sup>	Less than 0.15 ohms
Soft Solder	Flat - max solder thickness 0.001 inch - 90% min wetting	~ 70-100 kgms/cm <sup>2</sup>	Less than 0.10 ohms
Gold-tin Eutectic Solder	Flat - max solder thickness 0.001 inch - 90% min wetting	~ 100-150 kgms/cm <sup>2</sup>	Less than 0.10 ohms
Thermal Compression Bond	Flat - 90% min wetting	~ 100 kgms/cm <sup>2</sup>	Less than 0.10 ohms

Note: 1. This is the approximate extra RF series resistance from an ideal lossless bond of 0.020" x 0.020" chip

Table 3. Methods for Top-Bonding Diode Chips

Type of Chip	Type of Circuit Board	
	Ceramic	Teflon Fiberglass Metal Ground
Planer Chip with Gold Metal on Anode	Wedge bond 0.002 diameter gold wire or 0.001 x 0.005 strap. Bonding tool must be smaller than anode pad.	
Beam Lead	Ultrasonic bond Bonding tip size 0.002 minimum Special tools are available for beam leads	NOT RECOMMENDED
Schottky Diodes with Planer Contacts	Wedge bond 0.0007 diameter gold wire. Bonding tip size 0.001 maximum	
Hermetic CERMACHIP™	Wedge bond. 0.001 x 0.005 strap is best Bonding tip size 0.005 maximum	Wedge bond, or parallel gap Or welded strap
Planer Chips with Very Small Node Pads (less than 0.002)	Wedge bond 0.0007 to 0.001 diameter gold wire. Bonding tip size 0.001 maximum	
Mesa Diodes (Small)	Wedge bond. Use 5 mil strap, if possible Bonding tool tip size 0.001 to 0.002.	

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**Reliability Problems**

Silver conductive epoxies should not be used where they will come into contact with lead tin solders or high tin solder. There can be an anodic reaction which may cause failure of the bond.

**Bond Strength**

The shear bond strength of good epoxy joint can approach that of solder 50-100Kgms/cm<sup>2</sup>. The thickness of the conductive epoxy should be kept at 0.001" or less.

- The shear bond strength should be about:
- 40-60 grams for 0.010 X 0.010 inch chip
- 150-250 grams for 0.020 x 0.020 inch chip
- 350-500 grams for 0.030 x 0.030 inch chip

In general the epoxy will shear before the chip breaks. Weak bonds are usually caused by the use of old epoxy, bonds that are too thick, or lack cleanliness.

**Thermal Resistance**

Although the thermal resistance of silver conductive epoxy bonds is a little higher than that of gold tin eutectic solder, it is still satisfactory for all but the highest power applications as long as the epoxy is kept thin.

**Visual Inspection**

Die down bonds should be checked regularly using a 5-15X microscope and should meet visual criteria shown in table 2.

**Top Bonding to the Chip**

Most chips can be bonded with a wedge bonder. The size and shape of the contact will depend on the size of the bonding pads and the parasitic inductance or capacitance requirement of the circuit.

A gold strap is effective for the majority of applications. Critical criteria in this procedure are cleanliness, bonding tip shape, tip pressure, and stage temperature.

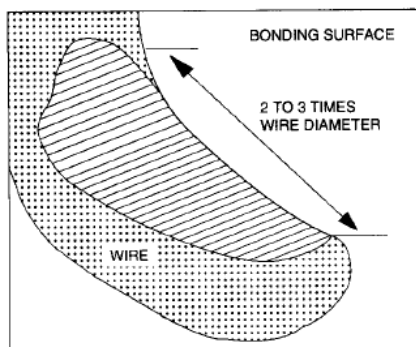


Figure 4. Typical Strong Wire Bond

**Top Contacting Methods**

The usual criteria for choosing a specific top bonding technique are the size of the top contact of the chip, the type of chip, the sensitivity of the chip to temperature and pressure, the type of circuit board and the equipment available. Table 3 illustrates some suggested top bonding methods listed by type of the chip and circuit applications. Usually the simplest contacts are gold strap 0.001 X 0.005 inch or a 0.0007 to 0.001 inch diameter wedge bonded gold wire. The inductance of a 1 mil diameter wire will be ~ 0.05 nH for a 0.20 inch long lead. This inductance can be reduced considerably by using multiple contact wires or by using straps (a technique which also increases reliability).

**Selection of Bonding Equipment Tools & Tips**

The choice of bonding equipment and tools depends greatly on the type of circuit and chips to be used. Most bonding equipment manufactures have useful literature available.

**Wire Bonding**

It is very difficult to give definite parameter values of force pressure time and temperature for an optimum bonding schedule. Different wires or strap sizes, bonding surfaces or semiconductor die characteristics require different bonding conditions. In general, the bonding parameters should be adjusted to maximize reproducibility at a high bond pull strength.

Most problems are caused by improper bonding machine and tool settings as well as improper maintenance and cleanliness. It is important to control the movement of the part being bonded, alignment of tools, tool height, angle, and tool condition.

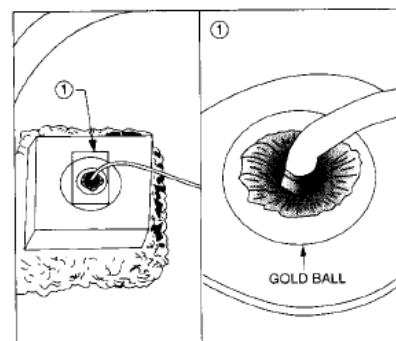


Figure 5. Sketch of a Good Nail Head Bond

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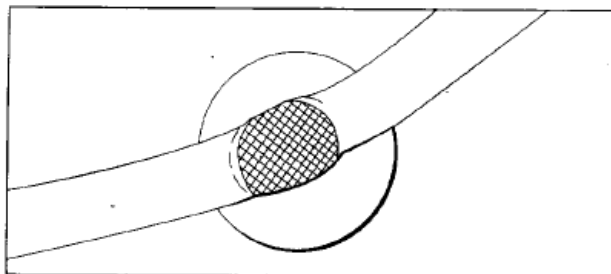


Figure 6. Single Strap Bond

In general, the die will crack or “crater” if too hard a wire or excessive pressure is used. Too little pressure results in small, weak bonds.

A good wire bond should be stronger than the wire and should also be two or three times the wire diameter as illustrated.

Also illustrated are drawings of another type of wire bond, the ball bond. As with all top bonds to planar die, the wire (or strap) should break during a pull test before the bond breaks.

When wire bonding, the deformed width of the wire should be about 1.3 to 1.8 times the wire thickness as shown in the wire bond sketch below.

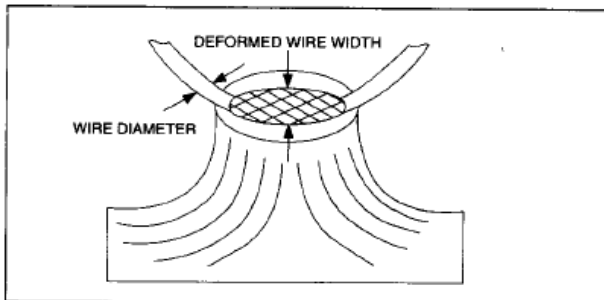


Figure 7. Appropriate Wire Bond Deformation for Maximum Strength

If the deformed width is too small, the bond will tend to lift off. If it is too large (greater than 1.8 times the wire diameter) the wire tends to weaken and break.

Also shown is a curve of the pull strength vs deformed width of ultrasonic bonded wire.

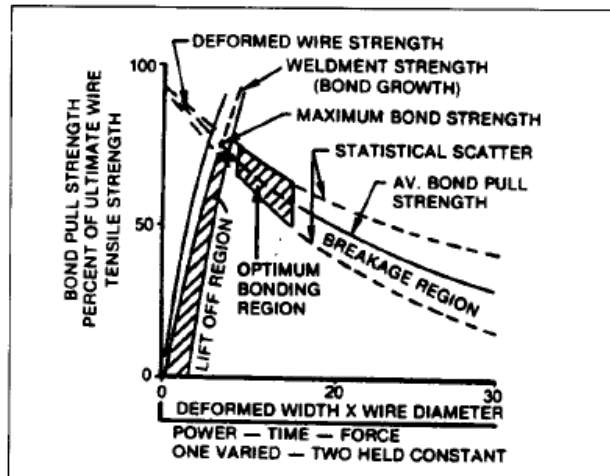


Figure 8. Pull Strength vs. Deformation for a Wirebond

Wire Bonding to GaAs Junctions

GaAs is very brittle, and although the above mentioned procedures apply, the following extra precautions should be taken when wire bonding.

Wire bonds to the junctions are best made using a thermal compression wedge bonder with a heated stage and tip. A stage temperature of 240°C and a tip temperature of 120°C is recommended. Typical bonding force should be the region of 20 grams for the smallest junctions but less than 40 grams for all others junctions. It is recommended that dead soft gold wire be used with a diameter of 0.0007 inches for the smallest mesa and 3 mil X 0.0005 ribbon for the largest mesa and 50 ohms attachment. For GaAs diodes, such as PIN diodes in parallel configuration, two ribbons are preferable.

Strap Bonding

When bonding a strap, the bond should not deform the strap by more than 50%. The tool and conditions should be selected to provide a bond that has at least the same cross sectional area as the strap itself. For example, a 0.5 mil x 5 mil strap should have a bond cross section of 2.5 mils square or greater. The schematic shown illustrates a typically strong single strap bond to a large mesa. Cross strapping is used for low parasitic inductance. Careful heat and pressure control must be exercised in order to form a strong, damage free cross strap bond.

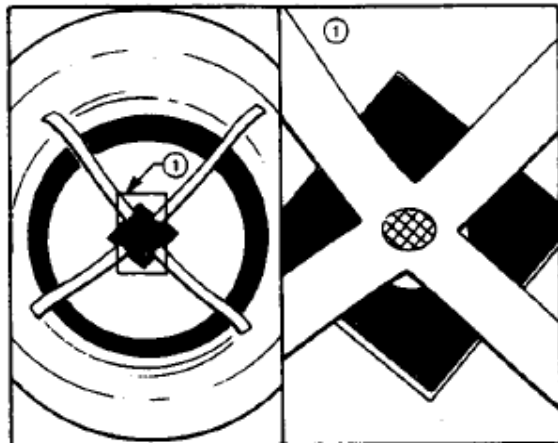


Figure 9. Cross Strap Bonding in a Packaged Device

### Bonding to Small Mesas

When bonding to a small mesa type diode, it is suggested to always use a strap. The strap, in many cases, may be larger than the top of the mesa (the larger the cross section area of the strap, the lower the parasitic inductance). In the case, it is advisable to bond all or as much to the entire top of the mesa as possible.

### Good Bonding Criteria

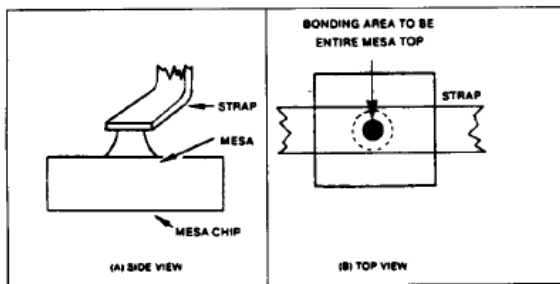


Figure 10. Mesa Bonding

When testing a mesa diode, if the bond is good, the mesa will usually break off before the bond or strap breaks. For all other bonds, the bonds should be as strong as the wire or strap when tested by pulling. Improper top bonding usually results in one of the following problems:

Cracking or stressing the die through excessive pressure.

Weak bonds from inadequate cleanliness or improper bonding conditions.

Excessive parasitic capacitance from overlapping wire or strap.

### Acceptable Bonds

- Wire or strap does not separate when tested.
- No fractures in bond.
- No separation of metallization.
- Wire breaks before bonds

### Bad Bonds

- Wire separates from bond.
- Bond fractures at weld
- Separation of metallization

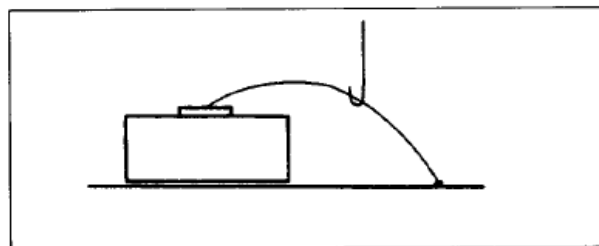


Figure 11.

### Bond Strength Pull Test

It is extremely important to maintain good quality control procedures in order to ensure good bonding. The following figures and tables illustrate criteria for visual inspection and for testing of bond strength.

Wire or Ribbon Size (inches)	Minimum Pull Strength (grams)
0.0007 wire diameter	1.5
0.001 wire diameter	3.0
0.002 wire diameter	9.0
0.00025 X 0.002 strap	1.0
0.00025 X 0.005	4.0
0.00025 X 0.010 strap	6.5
0.001 X 0.005 strap	10.0
0.001 X 0.010 strap	16.0

Table 4. Bond Strength Criteria (Gold Wire or Strap)

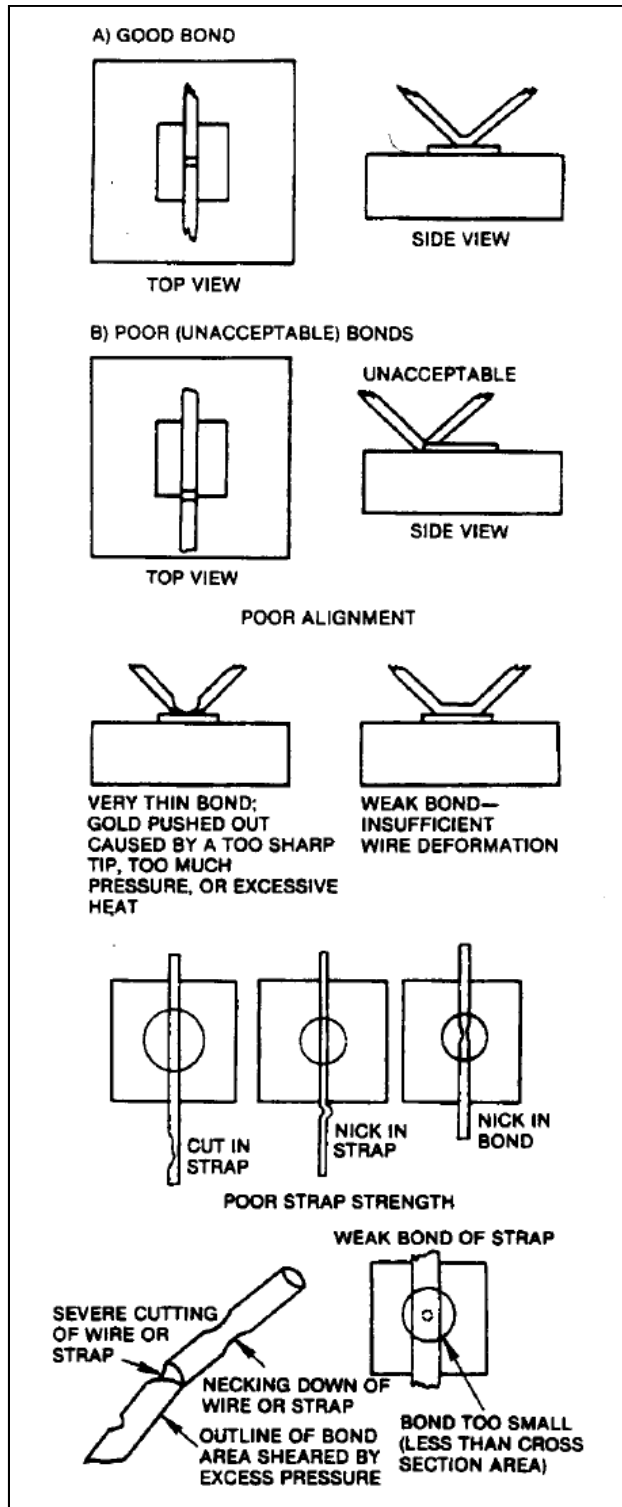


Figure 12. Visual Bond Inspection Criteria  
(Gold Wire or Strap Bonds)

## Bonding Beam Lead Diodes

Selection of the beam lead bonding method must take into consideration the characteristics of the circuit board material used. Hard substrates such as alumina and quartz are recommended. Various bonding techniques are described below and may all be used on hard surfaces.

The beam lead diode is a silicon chip with planar gold leads which extend from the top surface of the chip (~0.010 to 0.030 inches). Beam lead diodes are generally the smallest size chips available. They must be handled with care because the leads may easily be distorted or broken by the normal pressure of tweezers handling. Most vacuum tips are too large. A vacuum pencil with a #27 tip is recommended. A pointed wooden stick such as a sharpened Q tip or toothpick which has been dipped in isopropyl alcohol can also be used as a pick and place tool since the beam lead will adhere to the moistened point. This work should be performed under 10X to 30X magnification.

Beam lead diodes are easily damaged by static electricity and/ or current from a small low impedance ground loop in the circuit. When mounting the diode in the circuit, contact should never be made across the gap. A static discharge from the operator may flow through the diode and destroy it. The circuit should always be grounded before the second lead of the diode is attached.

The preferred methods for bonding a beam lead diode are thermal compression bonding and parallel gap welding. For thermal compression bonding, the beam lead diode is placed down (gold beam to gold plated substrate) with the leads resting flat on the pad and the bond made by using a heated wedge. Heat and pressure form a metallurgical bond. A minimum of 100 microinches of gold on the substrate is recommended for optimum bonding.

In the parallel gap technique, current is first passed through the substrate metallization, then through the device lead. Most of the heat is generated at the interface. Extreme care must be taken to see that the step welder does not discharge through the diode junction, or the diode will be destroyed. The bonding pressure should be ~ 900 gms / mm<sup>2</sup>.

The major advantage of the parallel gap technique is that a cold ambient may be used. Heat is only generated in the vicinity of the bond itself. Caution must be taken when making the second bond because if the diode is placed in tension, the leads may break.



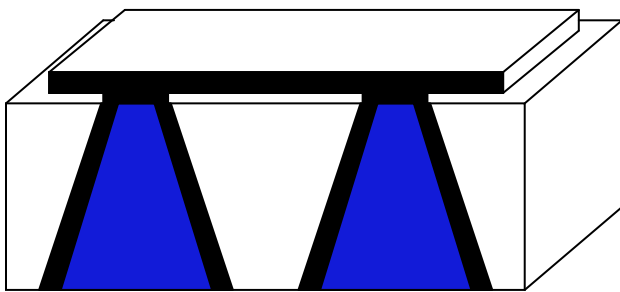
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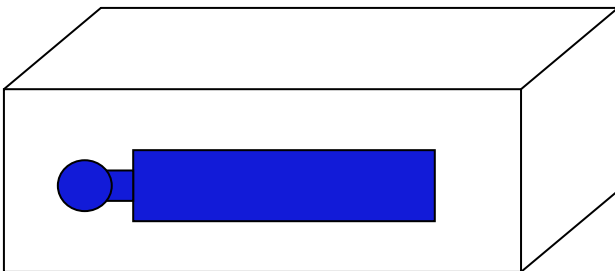
The following precautions will ensure better results when bonding beam leads:

To minimize the lead inductance, the wedge, or heated tips should be placed as close as possible to the chip without touching it. The chip is very easily damaged and care must be taken that the bonding tip does not contact the chip at any time during the bonding process.

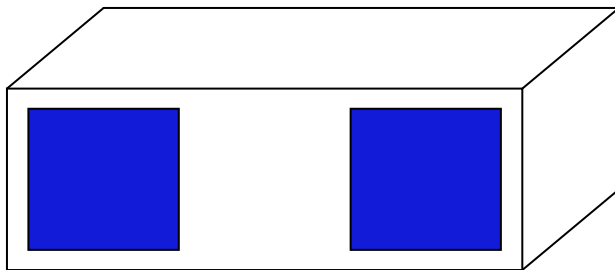
The bonding tip must be perpendicular to the beam during bonding, to prevent a torsional force which will pull the beams apart. This is particularly important when bonding the second lead.



**Cross Section**



**Top View**



**Bottom View**

**Handling and Bonding**

The rugged construction of SURMOUNT chip devices allows the use of standard handling and die attach techniques. It is important to note that industry standard electrostatic discharge (ESD) control is required at all times, due to the nature of Schottky junctions.

**Handling**

The devices can be handled with #3c tweezers for manual placement. The top surface of the die has a protective coating to minimize damage. These devices are compatible with vacuum pencil or automatic pick and place installation.

**Bonding**

Die attach for these devices is made simple through the use of surface mount die attach technology. Mounting pads are conveniently located on the bottom surface of these device and are removed from the active junction locations. The devices are well suited for high temperature solder attachment onto hard substrates. The use of 80% gold, 20% tin solder is recommended, but lead tin solders are acceptable. Conductive epoxy may also be used for die attach.

When soldering these devices to a hard substrate, hot gas die bonding is preferred. We recommend utilizing vacuum tip and force of 60 to 100 grams applied normal to the top surface of the device. When soldering to soft substrates, it is recommended to use a lead-tin interface at the circuit board mounting pads. Position the die so that its mounting pads are aligned with the circuit board mounting pads, and reflow the solder by heating the circuit trace near the mounting pad while applying 60 to 100 grams force perpendicular to the top surface of the die. Solder reflow must not be accomplished by causing heat to flow through the die. Consequently, the solder joints must be made one at a time, or a multi-tip soldering iron could be used to simultaneously reflow all the solder joints.

Since the HMIC glass is transparent, the edges of the mounting pads closest to each other can be visually inspected through the die after die attach is completed.