Drivers for GaAs FET MMIC Switches and Digital Attenuators

Rev. V3

Application Note

M/A-COM's Microelectronics Division produces a silicon CMOS Application Specific Integrated Circuit (ASIC) that drives GaAs Field Effect Transistor (FET) based switches or digital attenuators from a single TTL or compatible IC. These ASICs are available in single (SW-109) or squad-channel (SWD-119) plastic packages. This application note provides technical and application information to simplify the use of these drivers.

Introduction

GaAs MMIC control devices like switches and digital attenuators typically employ FET technology. The most common FET is the N-channel depletion mode device which has low source-to-drain resistance when there is no bias. When a negative voltage is applied to the gate, the electric field narrows the channel, increasing the source-to-drain resistance. The voltage that closes off the channel and created the highest resistance of the FET is known as the "pinch-off" voltage. For M/A-COM FETs, the pinch-off voltage is typically -2.5 volts.

FETs can be arranged in series and/or shunt configurations, then biased to provide varying insertion loss values. By varying the gate voltage between zero volts and some value greater than pinch-off (typically -5 to -8 volts), the FET acts as a voltage variable resistor. If the device is biased at the extremes (0 V and -5 V), *on* and *off* switching results, providing the basis for both the GaAs MMIC switches and digital attenuators. Switches require low loss (*on*) and high loss (*off*) paths during operation. Digital attenuators use bits of different loss values to switch in or out of the transmission path, either individually or in combination.

FET based control devices are most often configured in series/shunt arrangements, resulting in the broadest bandwidth for the available size. In these configurations, the driver output must be complementary, supplying different voltage levels to the series and shunt mounted FETs. This is usually accomplished with level translation and multiple IC chips, increasing the complexity, size, and DC power dissipation of the device.

Design Considerations

To accommodate the need for a large output voltage swing and low DC power dissipation, the ASIC design uses a standard CMOS analog fabrication process. A buffering stage is added so that the driver will switch with standard TTL, as well as CMOS logic levels, increasing the flexibility and ease of use for system designers. The ASIC driver requires only a single control input per channel, further simplifying the external drive requirements.

TTL Input Buffer

The input buffer operates at standard TTL input levels, despite being fabricated with a CMOS process. The CMOS process keeps the quiescent current in the microamp range when the input control signal is close to V_{CC}. When the control signal level drops, the quiescent current increases. At a control voltage of 2.9 volts, the current increases to only 0.7 mA.

As the block diagram shows, the TTL input buffering is followed by additional buffering stages that take the input TTL signal and generate two complementary signals. The two signals, noninverting and inverting, are also buffered to ensure they are at the proper levels. The need for complementary signals arises, as described earlier, from the series-shunt schematic of most GaAs MMIC based control devices.

Voltage Translator

The input buffering is followed by a voltage translator. This stage translates the 0-V and 5-V TTL levels to the voltage levels required to switch the GaAs MMIC device to the *on* and *off* states. As described earlier, switching in a GaAs FET MMIC occurs when the incident voltages change from 0 V to a level greater than pinch-off. These drivers include a feature in the translator section that allows the user to optimize the performance of the GaAs MMIC device being driven.

At pinch-off, the electric field on the gate closes the channel of the FET resulting in the high resistance state of the FET. If the gate voltage is near the pinch-off value, the incident RF voltage may modulate this resistance.

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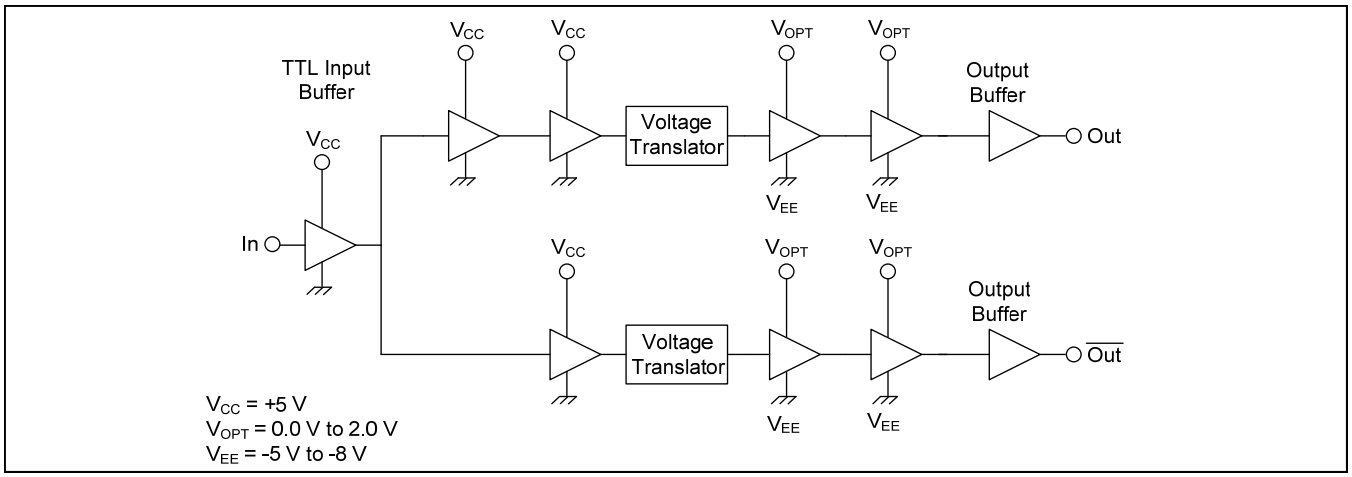

Figure 1. Driver Block Diagram

This effect can be minimized by increasing the gate voltage. With higher gate voltage, the incident RF voltage needs to be at a higher level to cause the same resistance modulation. The gate voltage level affects performance in two regards.

First, if the RF signal level is high enough to cause the resistance to modulate, the insertion loss of the MMIC may increase, a condition known as compression. The common measurement of this phenomenon is the 1-dB compression point. This is a measure of the power level where the loss of the device increases by 1 dB from the low power loss levels. If the gate voltage increases, the incident RF power must be higher to cause compression. The net result is an increase in the 1-dB compression point, allowing the device to operate at higher input power levels. The voltage that biases the gate, shown as V_{EE} in the block diagram, is adjustable from -5 V to -8 V and appears directly at the gate of the GaAs FET.

The second impact occurs in the intermodulation performance. The modulation described above causes the FET to become more non-linear as the resistance of the GaAs FET acquires a time varying component. Modulation increases the distortion of the GaAs FET, degrading the harmonic and intermodulation performance. Increasing the gate voltage minimizes the modulation effect for a given power level.

Since the GaAs FET is a voltage variable resistance from 0 V to pinch-off, it follows that the same modulation effect may occur at the 0-V bias level. M/A-COM has found that if a GaAs FET is biased slightly positive, this effect is minimized. In this case, the resistance of the GaAs FET may increase during the negative portion of the incident RF signal. A small positive offset minimizes this, improving the intermodulation performance. The voltage is referred to in these switch drivers as V_{OPT}. The drivers will accommodate this voltage being varied from 0 V to +2 V to optimize intermodulation performance.

Output Buffer

The final section of the driver is an output buffer that occurs after the voltage translation and is composed of successively larger buffer stages. A GaAs FET MMIC control component usually consists of several FETs with the gates of multiple devices tied together. Since each device has finite isolation, tying the gates together presents a cross-talk isolation concern. The standard technique to minimize this is to add capacitance to ground on the control lines, shunting any RF energy on the control lines to ground. The buffering stages are designed to allow the driver to drive a load capacitance up to 25 pF.

Performance

For guaranteed maximum ratings and performance over temperature, please refer to the SWD-109 and SWD-119 datasheet.

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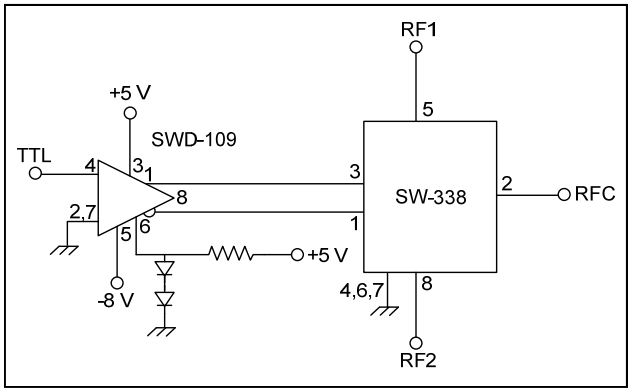

Figure 2. SWD-109 Single-Channel Driver and SW-338 GaAs MMIC Switch

TTL Input	Outputs	
C1	A	B
Logic 0	V_{EE}	V_{OPT}
Logic 1	V_{OPT}	V_{EE}

Control Inputs		RF Common to:	
A	B	RF1	RF2
1 (V_{EE})	0 (V_{OPT})	On	Off
0 (V_{OPT})	1 (V_{EE})	Off	On

Additional Notes

1. To achieve the fastest switching performance, the GaAs FET MMIC die should be floated at a potential of +5 V.
2. V_{OPT} of 1.4 V can be derived from a circuit consisting of a resistor from the +5 volt supply to a pair of diodes mounted to ground (see Fig. 2).
3. The single-channel driver (SWD-109) is available in an SOIC 8-lead plastic package. The quad-channel driver (SWD-119) is available in an SOIC 16-lead plastic package.
4. The SWD-109 is supplied with two ground pins (Pin 2 and 7). Only one of the two pins need to be grounded.
5. If V_{OPT} is not required, the pin should be grounded.

Summary

M/A-COM Microelectronics Division has introduced a silicon CMOS ASIC driver for GaAs FET MMIC control devices. This driver is designed to operate with TTL or CMOS input logic levels, without the need for any external components. The ASIC driver requires positive (+5 V) and negative (-5 V to -8 V) voltages for operation. A third voltage (VOPR) can be supplied to improve the low frequency performance of GaAs FET MMIC control devices.