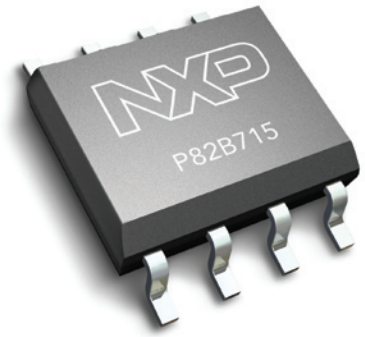

NXP I²C-bus extender P82B715

Extend the reach of any I²C-bus system without special offset voltage levels

This analog bipolar IC retains all the features of the I²C-bus including interoperability with all master/slaves and bus buffers while extending the I²C-bus well beyond the limits of the standard 400-pF bus capacitance without having to use special offset voltage levels and their inherent loss in noise margin.

Key features

- Dual, bidirectional, unity voltage gain buffering without special offset voltages
- Wide supply voltage range (3 to 12 V)
- Compatible with I²C-bus, SMBus and PMBus devices
- 10x bus impedance transformation allows total loading of 3000 pF on the system
- Logic signal levels may include V_{CC} and ground
- Rugged bipolar process with excellent ESD performance
- 8-pin SO and DIL packages

Applications

- Extending the communication distances of the I²C-bus over wires
- AdvancedTCA radial bus architecture
- Allowing more capacitance within one system without having to isolate individual legs or use buffers with special voltage levels

The NXP P82B715 extends the reach of the I²C-bus by buffering both the data (SDA) and the clock (SCL) lines.

The standard bus capacitance of 400 pF restricts practical communication distances to a few meters. Using one P82B715 at each end of a long cable (connecting Lx/Ly to Lx/Ly) reduces the cable loading capacitance of the I²C-bus by a factor of 10 which lets the total system capacitance load (all devices, connectors, traces, and wires connected to the I²C-bus) to be increased to about 3000 pF with maximum of 400 pF on each devices Sx/Sy side. As a result, longer cables or low-cost, general-purpose, wiring can be used to connect I²C-based systems point to point or multi-point without worrying about the special voltage levels used by other I²C-bus buffers like the P82B96 which isolate capacitance to each node.

Multiple P82B715 devices can be connected together, via their Lx/Ly ports, in a star or multi-port architecture, as long as the total capacitance of the system remains less than about 3000 pF and each Sx/Sy connection remains below 400 pF. In this kind of configuration, the master and/or slave devices are

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attached to the Sx/Sy port of each P82B715 and all devices can communicate with each other.

The impedance-transforming action of the P82B715 means that a single, low-cost external transistor is all that's needed to implement logic-level shifting if voltage translation is required.

There is no restriction on interconnecting the Sx/Sy I/Os, and, because the device output levels are always held within 100mV of input drive levels, all the I/Os are compatible with bus buffers that use voltage-level offsets. This feature makes them useful in Radial IPMB applications in AdvancedTCA where dynamic level offset hot swap buffers are required to be used..

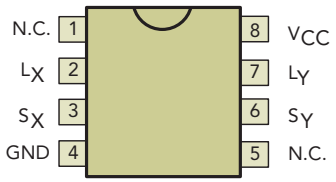
The operating voltage range is 3 to 12 V and the operating temperature range is -40 to 85 °C. It supports clock frequencies from 0 to 400 kHz.

Ordering information

Package	Container	Drawing	12NC	Part Number
SO 8	Tube	SOT96-1	935154770112	P82B715TD
SO 8	T & R	SOT96-1	935154770118	P82B715TD
DIP 8	Tube	SOT97-1	935154220112	P82B715PN

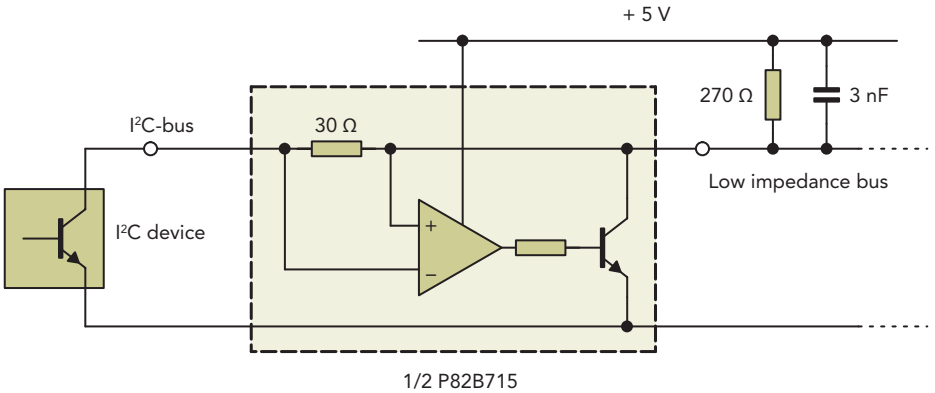
Pin configurations

8-Pin Dual In-Line or SO
P82B715

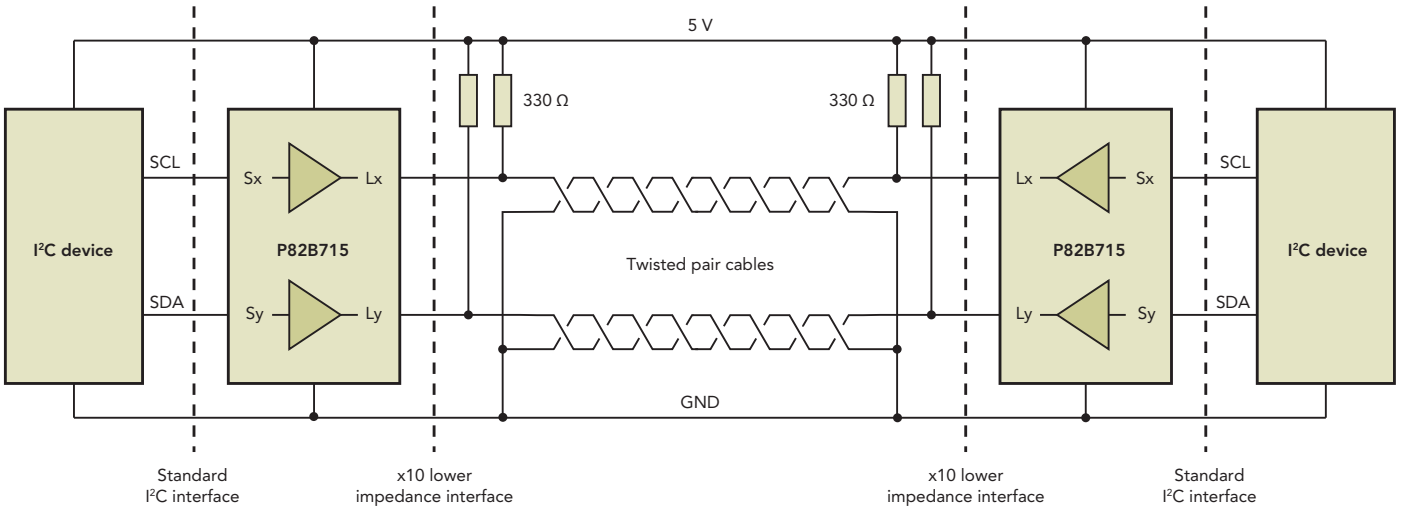


Pinning

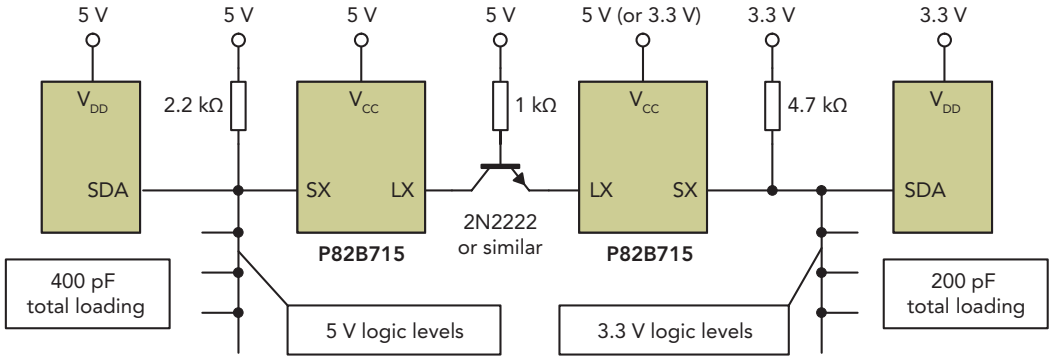
Pin	Symbol	Function
1	N.C.	No connect
2	L_X	Buffered bus, LDA, or LCL
3	S_X	I²C-bus, SDA, or SCL
4	GND	Negative supply
5	N.C.	No connect
6	S_Y	I²C-bus, SCL, or SDA
7	L_Y	Buffered bus, LDA, or LCL
8	V_{CC}	Positive supply



Typical P82B715 voltage follower implementation



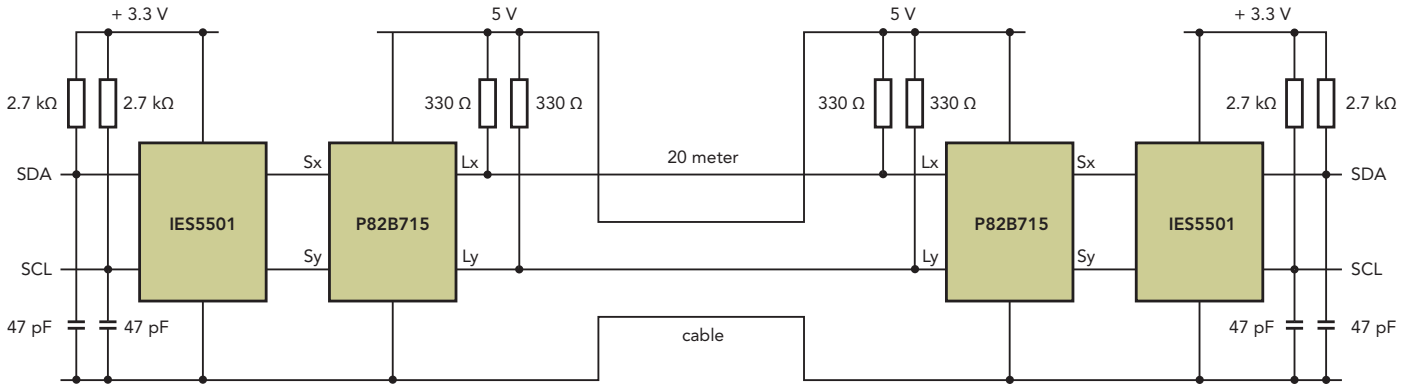
Minimum Sub-System with P82B715



Using simple discrete for logic level translation

P82B715 Characteristic	Simplifies application	Restrictions
Bus logic signal levels are independent of Vcc supply.	Handles all logic voltages in the range 0V to Vcc. I/O levels are set by the connected components.	Logic voltage levels must be less than Vcc.
Wide supply voltage range (3V to 12V).	Can handle all logic levels up to 12V.	Has derated performance for supplies below 4.5V but typically retains full performance at 3.3V.
Allows simple paralleling of multiple ICs on either its input or output sides.	Allows all bus configurations, on input and output, for example star or multi-drop architectures.	Usual I²C limitation of 400pF (effective) applies on the Sx/Sy side and x10 scaled limit on Lx side.
x10 drive capability on one side (Lx/Ly).	Driving low impedance buses with large capacitance (to at least 3000pF) or driving long cables.	Load on Lx side is not isolated, it is 'transformed' so it appears as 1/10 actual load. Cable limit about 40m.
Output bus signal voltage always equals input bus signal voltage (max difference 100mV).	Does not alter the bus logic levels used by I²C or any derivative buses using TTL levels, such as SMBus. Can be used without restriction with buffers having special (low) switching levels that are not I²C or TTL compliant.	Logic voltage level shifting is not supported - but is easy using minimal additional low cost components.
Controlled slew rate.	Minimizes ringing/overshoot when driving long cables. Very tolerant of different cables/configurations.	Reduced top speed. Best for 100kHz and below but can be applied up to 400kHz.
Built with rugged bipolar IC process.	Tolerates significant ESD energy and overloading. No latch-up, provides some protection for connected ICs.	Data sheet limits should be observed. Add conventional components for maximum protection.
Has clamp diodes from I/Os to Vcc.	Improves ESD and overload characteristics.	Not allowed by Fast Mode 400 kHz specs. Pulls connected buses low if its Vcc supply fails.

Easy-to-implement long distance cable application



The P82B715 coupled with the IES5501 can drive cables is a proven application backed by testing (tested to 20m and good for at least 30-40m). It's non-critical on how the circuit is built because the IES5501 provides true buffering and isolation at the SDA/SCL terminals. These I/Os loadings are not affected by the cable loading and may be included in systems in the same way as standard I^2C interfaces. They may be paralleled to allow driving multiple branches each with 20-40m cabling.

Date of release: November 2007
Document order number: 9397 750 16080
Printed in the USA