NXP bidirectional voltage level translators NVT20xx

Flexible, efficient voltage translation for open-drain and push-pull apps

Available in several channel options to accommodate a wide number of applications, these devices perform bidirectional low-voltage translation with less signal distortion and lower propagation delay, and without using a directional control pin.

Key features

- Bidirectional voltage translation without the need for directional control pin
- Lowest standby current (<5 µA for all supply voltages)
- Allows voltage level translation between
  - 1.0 V ($V_{ref(A)}$) and 1.8, 2.5, 3.3, or 5 V ($V_{ref(B)}$)
  - 1.2 V ($V_{ref(A)}$) and 1.8, 2.5, 3.3, or 5 V ($V_{ref(B)}$)
  - 1.8 V ($V_{ref(A)}$) and 3.3 or 5 V ($V_{ref(B)}$)
  - 2.5 V ($V_{ref(A)}$) and 5 V ($V_{ref(B)}$)
  - 3.3 V ($V_{ref(A)}$) and 5 V ($V_{ref(B)}$)
- High impedance I/O (An and Bn pins) when no supply voltage or EN = LOW
- Bus isolation for power supply fault
- Improved ON-state resistance (R_{ON} = 3.5 Ω) over existing GTL devices
- Flow-through pin-out for easier PCB trace routing
- Less than 1.5 ns maximum propagation delay
- 5 V tolerant I/O ports to support mixed-mode signal operation
- Ideal for open-drain and push-pull applications
- Packages: SO, TSSOP, XQFN, DHVQFN, HVQFN, XSON, HXSON

NXP's NVT20xx family is a series of bidirectional voltage level translations that operate from 1.0 to 3.6 V ($V_{ref(A)}$) and 1.8 to 5.5 V ($V_{ref(B)}$). They perform bidirectional translations between 1.0 and 5 V without the need for a directional output pin in open-drain and push-pull applications and support widths from 1 to 10 bits. They are designed for applications that use a transmission speed of less than 33 MHz, an open-drain system with a 50 pF capacitance, and a pull-up of 197 Ω.

When the An or Bn port is LOW, the clamp is in the ON-state and a low-resistance connection exists between the An and Bn ports. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by $V_{ref(A)}$. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage [$V_{pu(D)}$] by the pull-up resistors. This functionality allows a seamless translation between higher and lower user-selected voltages without the need for directional control.

When EN is HIGH, the translator switch is on and the An I/O is connected to the Bn I/O. This allows bidirectional data flow between ports. When EN is LOW, the translator switch is off and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by $V_{ref(B)}$. To ensure a high-impedance state during power-up or power-down, EN must be LOW.

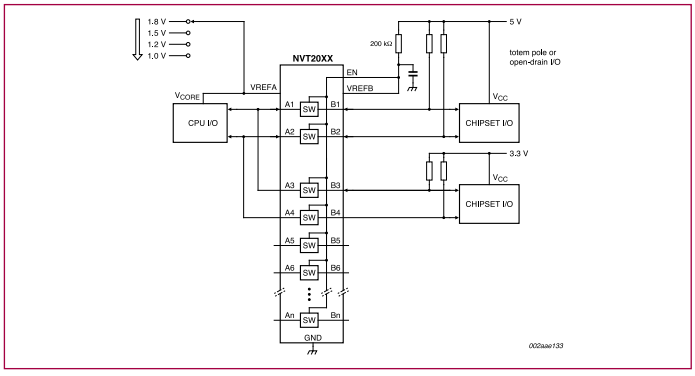
All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical.

The translator provides excellent ESD protection to lower-voltage devices, while at the same time protecting devices that are less resistant to ESD.

Bidirectional voltage translation

To configure the translators for bidirectional clamping, the $V_{ref(B)}$ input must be connected to EN and both pins must be pulled up to high-side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor at $V_{ref(B)}$ is recommended.

Bidirectional voltage translation to multiple higher voltage levels



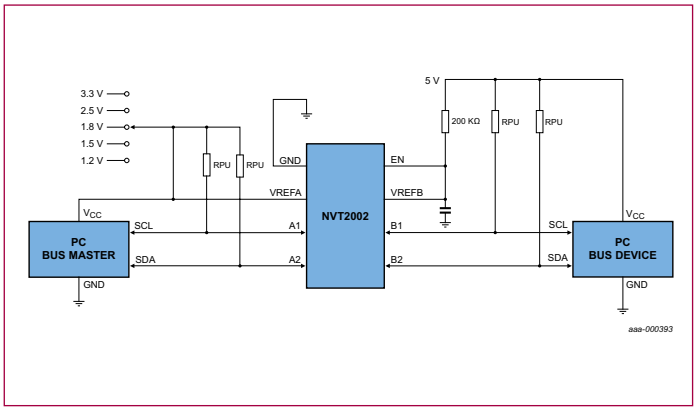
Channel options

# CH	New	OLD	Usage
1	NVT2001	-	Clock
2	NVT2002 PCA9306	GTL2002	I²C, I²S, SMBUS
3	NVT2003	-	I²C, server
4	NVT2004	-	SPI
6	NVT2006	-	I²C + SPI
8	NVT2008	GTL2003	Digital RGB
10	NVT2010	GTL2010	Data Bus

The CPU or the I²C bus master I/O can be set as totem pole or open drain (pull-up resistors are required to pull the Bn outputs to V_{CC}). No directional control is needed if both outputs are set as open drain. If either output is set to totem pole, there may be high or low contentions in either direction. To prevent this, set the data as unidirectional or use 3-stateable outputs with a mechanism for directional control.

On the low-power supply side, $V_{ref(A)}$ is connected to the CPU power supply voltage. When $V_{ref(B)}$ is connected through a 200 kΩ resistor to V_{CC}, and $V_{ref(A)}$ is set between 1.0 V and V_{CC} minus 1.0 V, the output of each An has a maximum output voltage equal to $V_{ref(A)}$ and the output of each Bn has a maximum output voltage equal to the drain pull-up supply voltage (e.g. 5 V).

Typical applications (NVT2002)



Ordering Information:

Package [1]	NVT2001	NVT2002 [2]	NVT2003	NVT2004	NVT2006	NVT2008 [3]	NVT2010 [4]
SO8	-	NVT2002D	-	-	-	-	-
TSSOPx	-	NVT2002DP	NVT2003DP	-	NVT2006PW	NVT2008PW	NVT2010PW
HVQFNx	-	-	-	-	NVT2006BS	-	NVT2010BS
DHVQFNx	-	-	-	-	NVT2006BQ	NVT2008BQ	NVT2010BQ
XSONxU XSONx	- NVT2001GM	NVT2002GD NVT2002GF	- -	- -	- -	- -	- -
XQFN8U	-	NVT2002GM	-	-	-	-	-
HXSONxU	-	NVT2002TL	-	NVT2004TL	NVT2006TL	-	-

(1) Suffix x denotes the number of leads; (2) GTL2002 = NVT2002; (3) GTL2003 = NVT2008; (4) GTL2010 = NVT2010

www.nxp.com

Date of release: September 2011
Document order number: 9397 750 17135
Printed in the Netherlands