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3G/4G Multimode Cellular Front End Challenges

Part 3: Impact on Power Amplifier Design

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Key Concepts Discussed:

- Power amplifier background.
- Low Power Mode versus DC-DC converters: impact on battery current.
- Quadrature versus single-ended architectures.

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Introduction

3G technologies are growing at a rapid pace in today's cellular industry. The outlook for multimode devices is growing more positive year over year as 2G cellular products mature in their life cycle. Handset users today demand higher data rates than ever before, which is increasing the complexity of the 3G system. To complicate the front end even more, the number of bands in which the modulations must operate has increased significantly. In order to meet these demands new standards are being developed, which will enable higher data rates through different modulation schemes across multiple frequency bands. WCDMA (Wideband Code Division Multiple Access) release 99 was released for voice capabilities followed by HSDPA (High Speed Downlink Packet Access), which increased the throughput capability of WCDMA. Now to satisfy user demand, even greater requirements are being placed on the system with HSUPA (High Speed Uplink Packet Access) and the follow-on standard of LTE.

As these modulation schemes become available, problems arise for the handset designer when it comes to current consumption of the front end. Each modulation scheme requires a different amount of linearity requirements, as well as inconsistent post-PA loss for different bands, which leads to increased current consumption when operating in any of the other modes and/or bands. In this paper, Part 3 of our three-part series on 3G/4G multimode handsets, the authors will examine the fundamental challenges engineers face when designing front ends to be multi-band and multi-standard across different modulations.

Power Amplifier Background

Prior to discussing the in-depth technical requirements on the power amplifier (PA), it will be worthwhile to review some basic concepts in amplifier design. One of the first steps in amplifier design is to determine the saturated power capability of the amplifier at a given battery voltage. The relationship between battery voltage, power, and load resistance is given in Equation 1.

Equation 1

$$PdBm := 10\log\left[\left[\frac{(2\cdot Vcc - Vsat)^2}{8\cdot Rload\cdot 10^{-3}}\right]\right]$$

Battery voltage and/or load resistance are the only two variables in the above equation that can affect the output power capabilities of a given design. This is a key concept in understanding this inefficiency in the multimode front end and in further realizing what can be done from a design selection standpoint to solve the issue.

Modulation Difference Explained

As mentioned earlier in this white paper, future handsets will have to support many different modulation protocols. The issue with supporting voice, HSDPA, HSUPA, and even LTE further in time, centers on the different linearity requirements between all of these modulations. Each of these modulations requires a different P1dB compression point on the amplifier. Figure 1 illustrates the power requirements for these modulations and the peak-to-average ratio (PAR).

Figure 1. Peak-to-Average Ratio

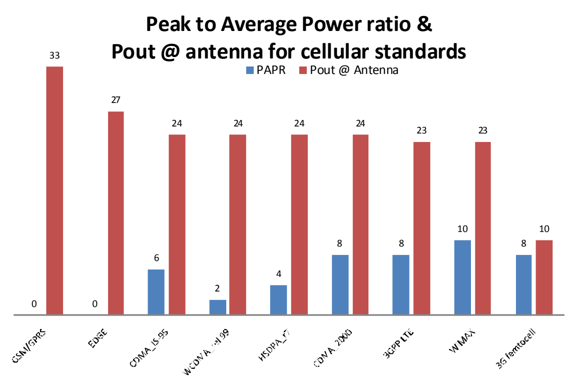
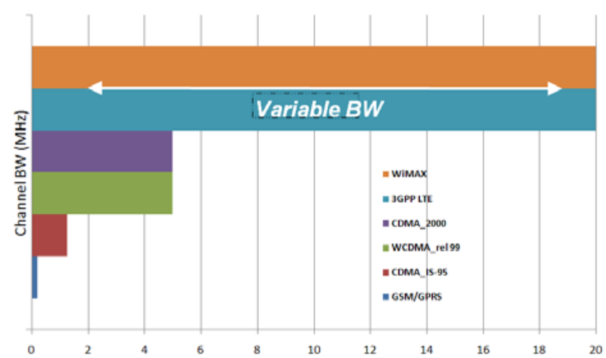
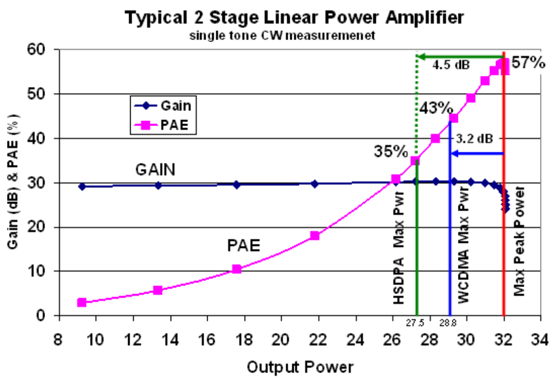


Figure 2. Channel Bandwidth of Cellular Standards



In this discussion, focusing on the 3G modulations allows the reader to conclude that each of these modulations requires a different P1dB compression point even with the allowed backed-off power amounts. This is the fundamental problem that handset designers must solve in order to not suffer large inefficiencies in their systems. Figure 3 shows the amount of back-off from the P1dB point that each of the modulations will require in the system.

Figure 3. Power Back-off Requirements from P1dB Point

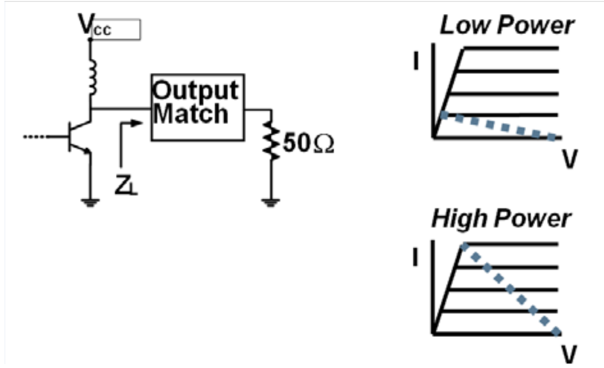


As the reader will recall, the only two variables that can be changed in order to alter the output power capabilities of the design is the load resistance or the battery voltage. Not actively changing either of these two will require that the design is optimized for the most stringent modulation, and performance in other modulations will degrade. For example, in order to meet the HSDPA requirements, the PA is designed for a P1dB point of approximately 32 dBm. This will allow good performance when the handset is operated in HSDPA, but in voice mode, the efficiency of the system will degrade significantly. This is due to the added built-in headroom, for HSDPA will require further back-off from the P1dB point compared to voice mode. The further back-off will give to much linearity margin at the expense of current consumption. The only way to solve this problem is to either change the load resistance between the modes or change the battery voltage as Equation 1 has shown. Each of these techniques is described in the following sections.

Load Switching

Assuming that a load switching circuit could be designed efficiently, this is one option in which the performance can be optimized between the two modes of operation. For higher power requirements in HSDPA and LTE, lower impedance is shown to the collector of the PA. For voice modulation, a switch would change the load that is presented to the collector to a higher impedance, therefore limiting the amount of headroom in the amplifier. Figure 4 illustrates this concept on the IV curves.

Figure 4. Load Switching



Realistically, this approach is not feasible with today's size requirements and the number of switch points that would be required. This technique requires multiple matching circuits, switches, or shared components, which makes it difficult to fully optimize both modes of operations.

Collector Voltage

The simplest way to optimize different modulations is by changing the collector voltage supplied to the PA. Changing the collector voltage will allow dynamic control of the load line since Vcc is one of the variables that affects output power. This approach is easily accomplished with the use of a DC-DC converter. DC-DC converters allow the voltage to be dynamically controlled very efficiently. Most converters on the market today approach efficiency of 95 percent at full current draw (meaning full power).

Low Power Mode (LPM) versus DC-DC

The previous paragraphs should provide a solid introduction to the fundamentals of PAs, which will allow the discussion to move to a more in-depth analysis into a debate that takes place in the world of amplifier design for 3G/4G systems today. Currently the two most common techniques commercially available to lower the current consumption in the front end are DC-DC converters and LPM PAs. Earlier in the paper, the authors mentioned two problems facing designers–multi-band and multi-standard. In exploring LPM versus DC-DC, the reader can conclude which approach may be the best option for his or her particular design, depending on which problem has more merit than the other. LPM (Low Power Mode) PAs are PAs that operate in two or three modes of operation–high power mode, which operates at full power, mid power mode to cover the mid power range, and finally, an LPM to cover the lower power levels. This method has been used for quite some time and has been very effective in the past for an inexpensive approach to lowering current consumption. The advantage to this approach versus a DC-DC is the board space required for an extra device and inductor.

The main concern with this approach moving forward is the inability to change the load resistance, which prevents a full optimization of the system when changing between modulations. For example, a PA P1dB is set by the most stringent modulation requirement that is needed for that particular device. If the PA is required to operate at 27dBm HSDPA, then this requirement sets the load line of the PA. If the collector voltage is held constant at 3.4 V to meet this requirement, as the user changes modes from HSDPA to WCDMA voice a significant amount of efficiency will be lost in the system as the P1dB required for voice is much less than HSDPA. When operated as described, the design has too much ACPR margin for voice and lower efficiencies than if this ACPR would have been traded off for better efficiency. Table 1 illustrates the delta in efficiency when operated in this mode.

Table 1

Converter	Modulation	Freq	V_{CC}	TP_{OUT}	Gain	PAE	ACPMax	ALTMax
None	Voice	1980	3.4	27	27.61	27.86	-42.74	-57.53
	HSDPA	1980	3.4	27	27.44	28.82	-39.93	-58.15
DC-DC	Voice	1980	3.4	27	27.61	31.76	-37.37	-55.58
	HSDPA	1980	3.4	27	27.44	33.45	-40.82	-52.98

If a DC-DC converter is used, the problem is easily solved, as the collector voltage could be set to 3.4 V for HSDPA and then bucked down to 3.1 V for voice modulation. Table 1 reveals that when using a converter the voice modulation was optimized by lowering the ACPR margin and increasing the efficiency by 4 to 5%.

The other main concern is the requirement to cover multiple bands. Unfortunately, not all frequency bands have the same post-PA losses due to the different requirements for the duplexers to handle the different transmit (TX) to receive (RX) separations. Band 2 duplexers generally have 0.9 to 1.0dB more loss compared to a Band 1 duplexer. If the same PA chain is to be used to cover both bands, then the load line must change to account for the different post-PA losses. Much like the previous example, the Band 2 will set the P1dB requirement for the amplifier design. To operate the PA in Band 1 the PA will require that the power to be backed off by 1dB to account for the differences in post-PA losses. This creates added headroom in the PA, which gives to much margin to the ACPR at the expense of current. If a DC-DC is used, then the voltage can easily be changed to accommodate different power requirements, which will give the designer the ability to maintain the correct relationship between ACPR and efficiency at any power level. Table 2 illustrates the performance difference when such a scenario is realized. If a DC-DC converter is utilized in the system then no matter the battery voltage or the post-PA loss, the DC-DC can control the collector voltage such that the power-added efficiency (PAE) will remain constant compared to the no-converter solution.

Table 2

Converter	Freq	V_{CC}	TP_{OUT}	Gain	PAE	ACPMax	ALTMax
None	1980	3.4	27	28	27.68	-44.2	-57.62
	1980	3.7	27	28.08	25.3	-45.28	-59.41
	1850	3.4	28	28.96	30.69	-42.04	-55.62
	1850	3.7	28	29.11	28.07	-43.62	-57.43
DC-DC	1980	3.4	27	27.13	36.66	-40.82	-52.98
	1980	3.7	27	26.94	36.62	-42.93	-55.04
	1850	3.4	28	28.57	36.65	-39.72	-53.16
	1850	3.7	28	28.19	36.8	-39.25	-53.38

To further explore the differences to the LPM versus DC-DC, a common metric can be used to measure expected performance. DG09 current is a common metric used in the industry to calculate current consumption based on the WCDMA user profile, which places the most emphasis on the lower power levels where the handset is operated for the largest percentage of time. Table 3 gives the expected DG09 differences between the two solutions

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when the devices were designed for Band 1 operation, and the only differences were LPM versus DC-DC converter. The same hardware was used for both experiments, with the only difference being the addition of the DC-DC converter and the PA configured for HPM operation all of the time.

Figure 5. PAM LPM versus DC-DC Converter

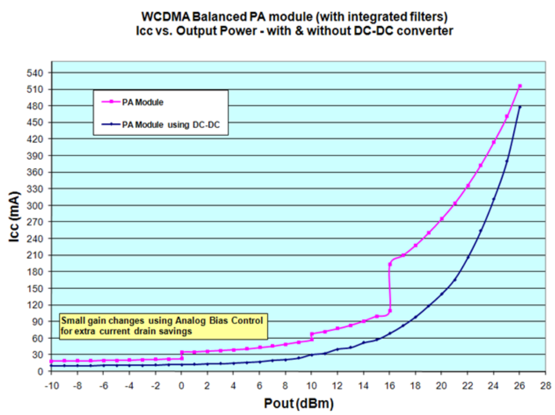


Table 3

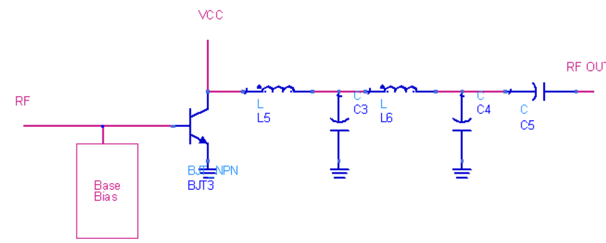
DG09 Data	LPM
Calculation Result Summary	
Avg Ibat=32.33mA	

DG09 Data	DCDC
Calculation Result Summary	
Avg Ibat=19.709mA	

Quadrature versus Single-Ended PA Architectures

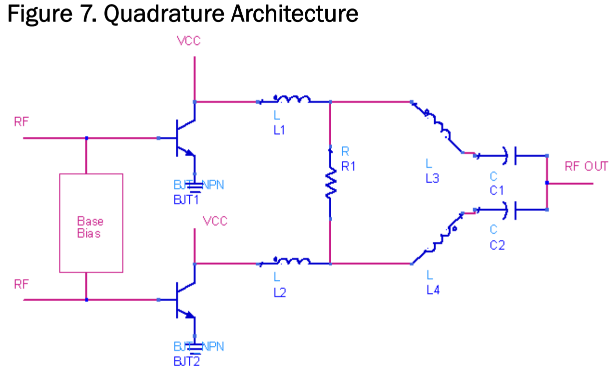
Another area of exploration in the front end is the PA architectures. As more demand is placed on data compared to voice, concerns with total radiated power (TRP) and VSWR performance has become more and more important to the handset designer. A choice can be made, depending on the chosen PA architecture, that may solve both the VSWR concerns as well as the multi-band problem. Two types of architectures that the authors will discuss in this writing are single-ended and quadrature. The single-ended architecture is the most common on the market today and includes a final stage followed by a low-pass matching circuit depicted in Figure 6.

Figure 6. Single-ended PA Architecture



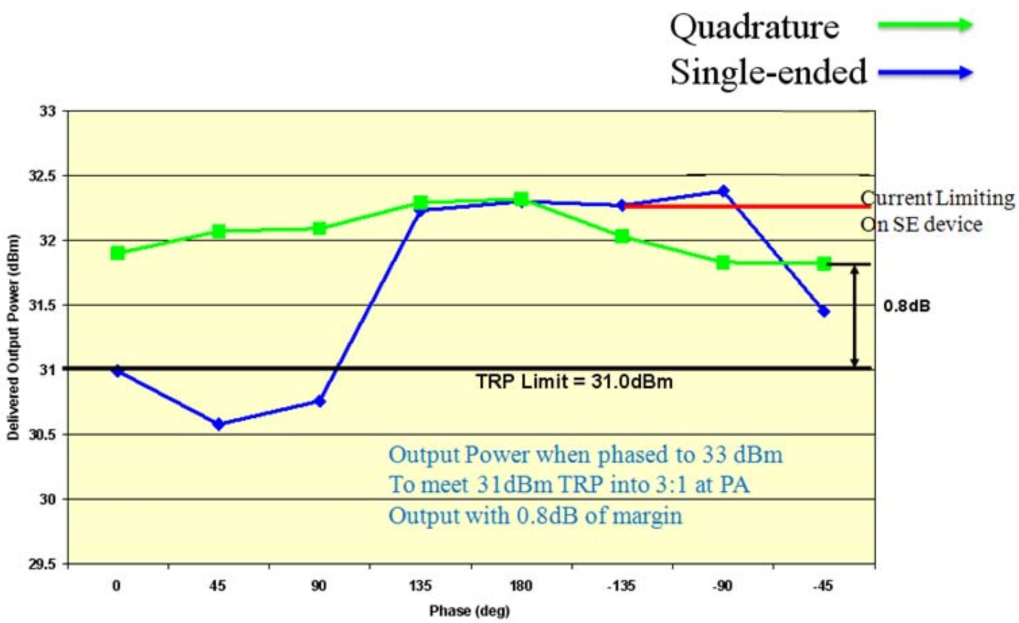
Another type of architecture is known as a quadrature design. This is shown in Figure 7 and has two parallel paths that are combined at the output with a lead lag matching network.

Figure 7. Quadrature Architecture



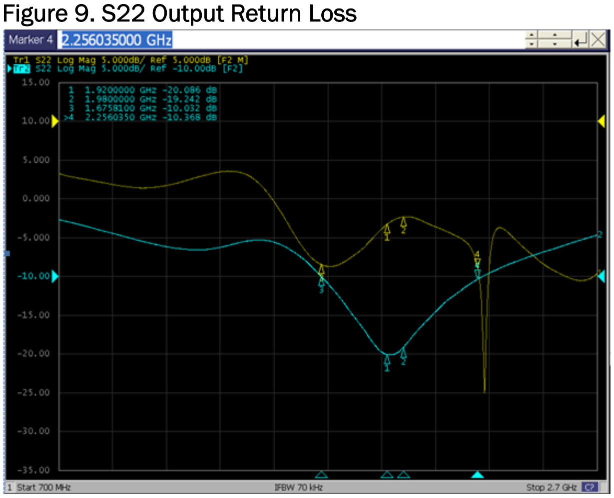
There are advantages and disadvantages to both approaches. The single-ended approach gives the best overall peak efficiency, as the matching network has minimal losses. The quadrature has a slight efficiency degradation due to the combiner losses compared to single-ended devices but will have very good VSWR performance. One way to overcome this small increased current consumption is by phasing the radio to lower output powers. TRP and VSWR performance generally drive the power level targets that a phone will be phased to in the factory. If a quadrature design is chosen the phone can be phased at about 0.5 dB lower output power and still have better TRP performance compared to the single-ended companion. Figure 8 shows the VSWR performance of quadrature design compared to a singled-ended device when both PAs are set to 33dBm of output power into 50 ohms and then load pulled into a 3:1 VSWR.

Figure 8. Output Power versus Phase



Another added benefit with the quadrature design is the ability to cover multiple bands. The quadrature PA has a much broader bandwidth compared to the single-ended PA architecture. Figure 9 shows the S22 output return loss of two such devices for illustration purposes.

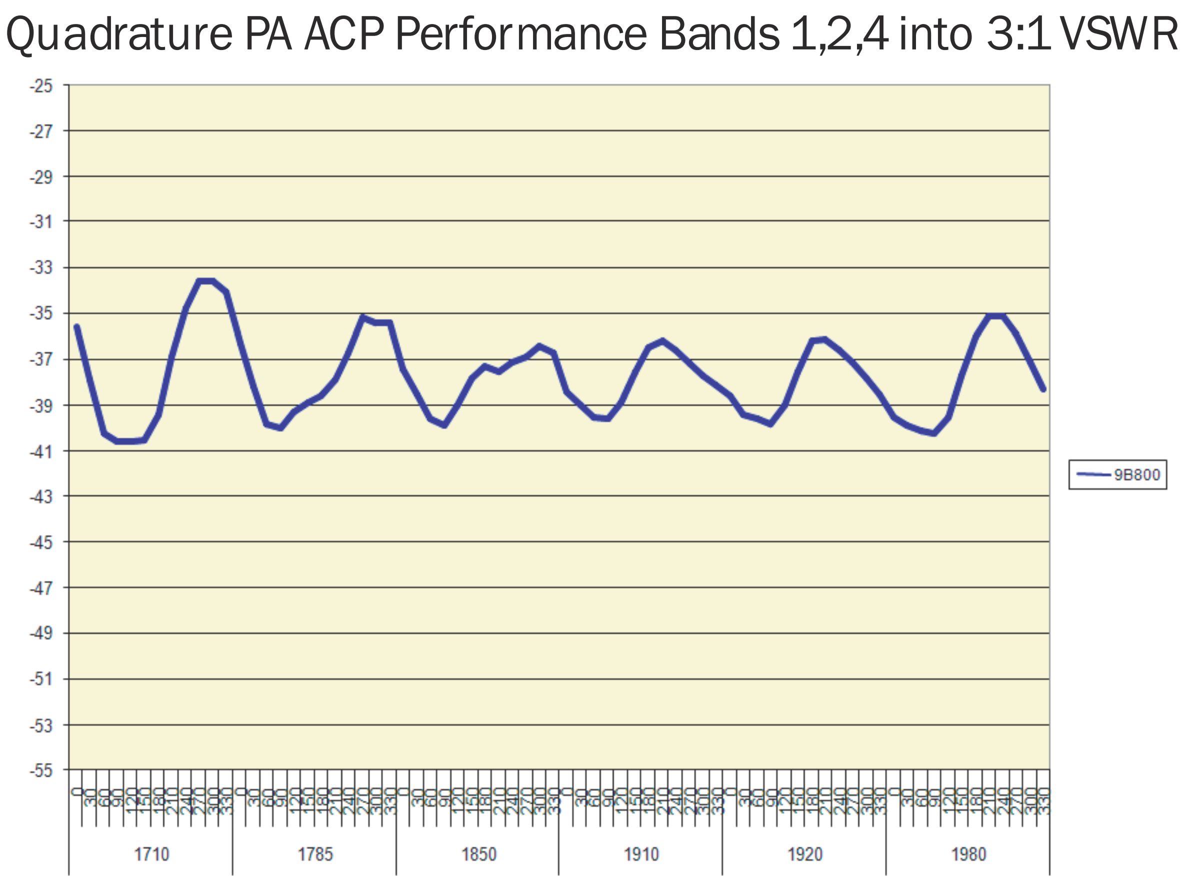
Figure 9. S22 Output Return Loss



The blue trace in Figure 9 is the quadrature design, which has a bandwidth (BW) of approximately 200MHz or so with an output return loss of -20dB or better. The yellow trace depicting the single-ended device is much less for BW and output return loss. The broadband characteristic of a quadrature PA can be used to help solve the issue of multi-band complexity of 3G/4G systems. Figure 10 shows the broadband characteristics and VSWR performance of the quadrature PA. The VSWR performance is maintained into a 3:1 VSWR for both bands 1 and 2 with very little degradation observed in band 3. This allows the same PA chain to cover multiple bands with the use of band switching post-PA to remove cost from the system without intolerable performance trade-offs.

When the total solution is required to cover multiple bands and multiple modulations a quadrature design with the addition of the converter may offer the handset designer the greatest flexibility. This is accomplished by providing large BWs to cover multiple bands due to the PA architecture. The ability to adjust the load line dynamically with the converter will also allow multiple modulations to be supported.

Figure 10.



This overview of the impact of 3G multimode requirements on PA design should leave you with a sense that a multimode design in any form is far more challenging than its single-mode counterpart.

Summary

In this series we have examined the challenges put forth in trying to optimize 3G front end for global performance in handsets and data cards. The complexity derived from numerous frequency band combinations, modulation requirements, as well as standard RF concerns such as layout and routing all contribute to a high degree of difficulty in optimizing for a single front end solution. We have found that making a multimode solution that is optimized for 3G data networks (wideband CDMA, HSPA plus, LTE) as well as being backward compatible to 2G networks is no trivial task. Design teams all over the globe are working to optimize solutions to reduce the number of trade-offs required to get small size, low cost, and optimal performance. While surveying the most common solutions available or soon to be available to the market, we look forward to even greater improvements as 3G multimode solutions become mainstream.

Contributors

Please feel free to contact the authors with any questions at RFMD.com

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