Advance Spec.

Product Technical Brief
S3C2440X Series
Rev 2.0, Oct. 2003

S3C2440X is a derivative product of Samsung's S3C24XXX family of microprocessors for mobile communication market. The S3C2440X's main enhancement over the baseline product, S3C2410X, is the addition of camera interface for multimedia messaging services.

The S3C2440X features an ARM920T core, a 16/32-bit RISC microprocessor, to provide hand-held devices and general applications with cost-effective, low-power, and high performance micro-controller solution in a small form-factor. The S3C2440X is developed using 0.13 um CMOS standard cell and a memory compiler. In addition, it adopts a new bus architecture called Advanced Microcontroller Bus Architecture (AMBA).

By providing a comprehensive set of common system peripherals, the S3C2440X minimizes the overall system costs and eliminates the need to configure additional components. The S3C2440 includes the following components: separate 16 KB instruction and 16 KB data cache, MMU to handle virtual memory management, TFT& STN LCD controller, NAND flash boot loader, system manager (chip select logic and SDRAM controller), 3-ch UART, 4-ch DMA, 4-ch timers with PWM, I/O ports, RTC, 8-ch 10-bit ADC and touch screen interface, camera interface, AC97 audio codec interface, IIC-BUS interface, IIS-BUS interface, USB host, USB device, SD host & multimedia card interface, 2-ch SPI and PLL for clock generation.

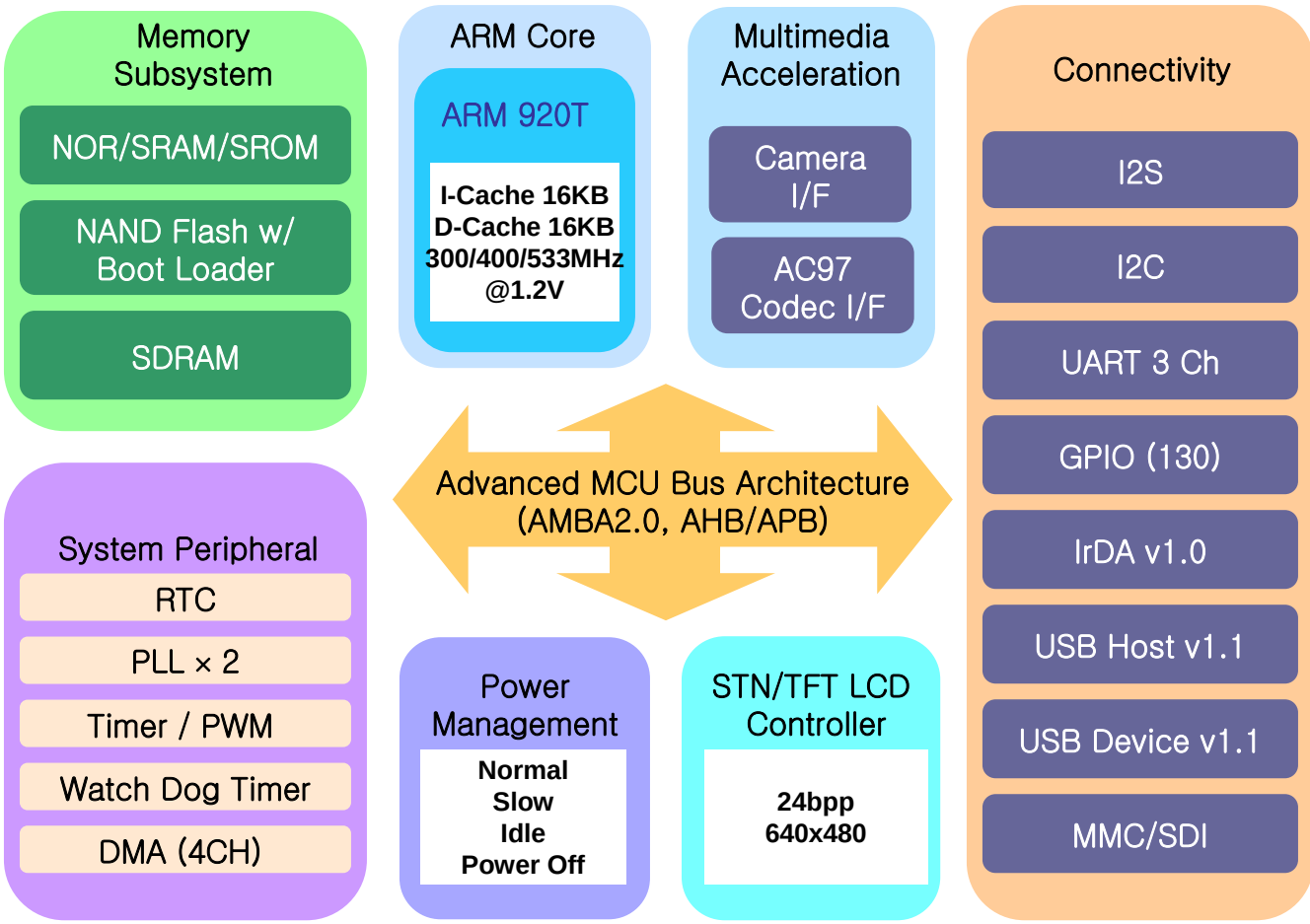
1. Feature Summary

- S3C2440X is developed using ARM920T core, 0.13 um CMOS standard cells and a memory complier
- Operating frequency 300/400/533 MHz @1.2V
- A new bus architecture called Advanced Microcontroller Bus Architecture (AMBA)
- 16 KB I-Cache and 16 KB D-Cache
- External memory controller with chip select logic
- LCD controller (up to 4K color STN and 256K color TFT) with 1-ch LCD dedicated to DMA
- Camera interface supporting up to 4096x4096 (supports ITU601/ ITU656 input format)
- AC97 audio codec interface
- 2 port USB Host (Version 1.1 Complaint)
- 1 port USB Device (Version 1.1 Complaint)
- 4-channel general DMA with external request pins
- 3-channel UART with IrDA 1.0 (Including 64-byte FIFO)/2-ch SPI
- 1-ch multi-master IIC-BUS/1-ch IIS-BUS controller
- SD Host interface version 1.0 & Multi-Media Card Protocol version 2.11 compatible
- 4-channel PWM timers and 1-ch internal timer
- 130 general purpose I/O ports/24-ch external interrupt source
- 8-ch 10-bit ADC and touch screen interface
- Watch dog timer
- RTC with calendar function
- On-chip clock generator with PLL

Ordering Information:

Part Number	Core Speed	Operating Voltage	Bus Speed
S3C2440X01	300/400/533 MHz	1.2 V	100 MHz

2. Functional Block Diagram



4. Product Details

4.1 ARM Core

- Integrated system for hand-held devices and general embedded applications
- 16/32-Bit RISC architecture and powerful instruction set with ARM920T CPU core
- Enhanced ARM architecture MMU to support WinCE, Symbian OS and Linux
- Instruction cache, data cache, write buffer and physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance
- ARM920T CPU core supports the ARM debug architecture.
- Internal Advanced Microcontroller Bus Architecture (AMBA) (AMBA2.0, AHB/APB)

4.2 Memory Subsystem

- NAND flash memory for boot loader and data storage
  - Supports booting from NAND flash memory
  - 4KB internal buffer for booting
  - Supports storage memory for NAND flash memory after booting
- NAND Interface
  - Supports industry standard NAND interface
  - 2.5V or 3.3V interface voltage
  - x8, x16 data bus
  - Density Support: 128Mb(x8/x16), 256Mb(x8/x16), 512Mb(x8/x16), 1Gb(x8/x16)
- SDRAM Interface
  - Standard 3.3V SDRAM interface or 2.5V/3.3V Mobile SDRAM Interface
    - 100MHz bus speed
    - x32 data bus
    - Interface voltage :2.5V or 3.3V
    - Density support : 128Mb(x16), 256Mb(x16), 512Mb(x16)
    - Can support Mobile SDRAM Interface, but can not support Mobile SDRAM specific Feature
- SRAM/ROM/NOR Flash Interface
  - x8 or x16 data bus
  - Interface voltage : 3.3V
  - Density support : Up to 128Mb(x16)
- Memory MCP support
  - Users can use memory MCP that integrates NAND flash and SDRAM on one package
  - Memory MCP can be directly connected to the application processor in the same manner as connecting discrete memory components

4.3 Multimedia Acceleration

4.3.1 Camera Interface

- ITU601/ITU656-format input support (8-bit)
- Up to 4096x4096 resolution
- YCbCr 4:2:2 to 4:2:0 down-sampling

4.3.2 AC97 Audio CODEC Interface

- 48KHz 16-bit sampling
- 1-ch stereo PCM inputs/1-ch stereo PCM output/1-ch MIC input

4.4 Display Controller

- STN LCD Interface
  - 4-bit dual scan, 4-bit single scan, and 8-bit single scan display type support
  - 256 colors and 4095 colors support
  - 640x480, 320x240, 160x160 or other display resolutions
  - Max. 2K x 2K virtual screen size
  - Max. 4095x1024, 2048x2048, 1024x4095 virtual screen size in 256 color mode, and others
- TFT LCD Interface
  - 1/2/4/8 bpp palletized or 16 bpp non-palletized color-TFF support
  - Supports maximum of 16M color TFT at 24 bpp mode
  - 640X480, 320x240, 160x160 or other display resolutions
  - Max. 2K x 2K virtual screen size
  - Max. 2048x1024 virtual screen size in 64K color mode, and others
- A/D Converter and Touch Screen Interface
  - 8-ch multiplexed ADC
  - Maximum 500KSPS and 10-bit resolution

4.5 Connectivity

4.5.1 IIC-Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode
- Up to 400 Kbit/s in the fast mode

4.5.2 IIS-Bus Interface

- 1-ch IIS-bus for audio interface with DMA-based operation
- Serial 8 or 16-bit per channel data transfers
- 128 Bytes (64-Byte + 64-Byte) FIFO for receive/transmit
- Supports IIS format and MSB-justified data format

4.5.3 UART

- 3-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Supports external clocks for the UART operation (UARTCLK)
- Programmable baud rate
- Supports IrDA 1.0
- Each channel has internal 64-byte Tx FIFO and 64-byte Rx FIFO

4.5.4 USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with USB Specification version 1.1

4.5.5 USB Device

- 1-port USB Device
- 5 Endpoints for USB Device
- Compatible with USB Specification version 1.1

4.5.6 SD Host Interface

- Compatible with SD Memory Card Protocol version 1.0
- Compatible with SDIO Card Protocol version 1.0
- Bytes FIFO for Tx/Rx
- DMA based or interrupt based operation
- Compatible with Multimedia Card Protocol version 2.11

4.5.7 SPI Interface

- Compatible with 2-ch Serial Peripheral Interface Protocol version 2.11
- 2x8 bits Shift register for Tx/Rx
- DMA-based or interrupt-based operation

4.6 System Peripherals

4.6.1 Clock & Power Manager

- On-chip MPLL and UPLL
  - UPLL generates the clock to operate USB host/device
  - MPLL generates the clock to operate MCU at maximum 300/400/533Mhz @ 1.2V
- Clock can be fed selectively to each function block by software
- Power mode: Normal, Slow, Idle, and Power-off mode
  - Normal mode: normal operating mode
  - Slow mode: Low frequency clock without PLL
  - Idle mode: the clock for only CPU is stopped
  - Power-off mode: the core power including all peripheral is shut down
- Woken up by EINT[15:0] or RTC alarm interrupt from Power-Off mode

4.6.2 Interrupt Controller

- 59 Interrupt sources (One Watch dog timer, 5 timers, 9 UARTs, 24 external interrupts, 4 DMA, 2 RTC, 2 ADC, 1IIC, 2 SPI, 1 SDI, 2 USB, 1 LCD, 1 Battery Fault, 1 NAND, and 2 Camera)
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

4.6.3 Timer with Pulse Width Modulation (PWM)

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

4.6.4 Real Time Clock (RTC)

- Full clock feature: msec, second, minute, hour, date, day, month, and year
- 32.768 KHz operation
- Alarm interrupt
- Time tick interrupt

4.6.5 DMA Controller

- 4-ch DMA controller
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

4.6.6 Watchdog Timer

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

4.6.7 GPIO

- 24 external interrupt ports
- Multiplexed input/output ports

4.7 Electrical Characteristics

4.7.1 Operating Voltage Range

- Core: 1.2V
- Memory: 1.8V/2.5V/3.3V
- I/O: 3.3V

4.7.2 Operating Frequency

- Up to 300/400/533 MHz