AN4028
Application note

50 W wide-range high power factor flyback converter using the L6564

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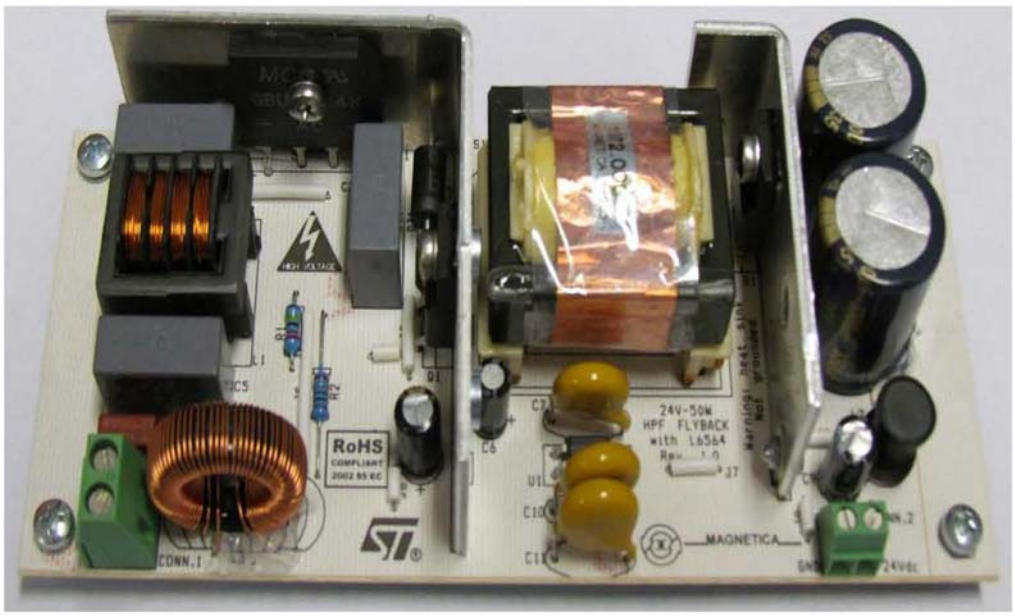
Introduction

This application note describes a high power factor flyback demonstration board based on the transition-mode PFC controller L6564 and presents the results of its bench evaluation. The board implements a 50 W, wide-range mains input, power factor corrected, power supply suitable for all low power applications needing high PF, such as lighting applications, LED power supplies, etc. To make it possible, the use of a low-cost device like the L6564 combined with a simple topology such as the flyback one provides for a very competitive solution.

Figure 1. EVL6564-50WFLB: L6564 50 W high PF flyback demo board



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1 Main characteristics and circuit description

The main characteristics of the SMPS are listed here below.

Table 1. Main characteristics of the SMPS

Parameter	Value
Line voltage range	90 to 265 V_{AC}
Minimum line frequency (fl)	47-63 Hz
Minimum switching frequency	44 KHz
Reflected voltage	140 V
Regulated output voltage	24 V
Rated output power	50 W
Power factor (load ≥ 50%)	0.9 minimum
Minimum efficiency at full load	88% at full load
Maximum 2fl output voltage ripple	1.1 V pk-pk (V_{IN}=230 V_{AC}, Pout=50 W)
Maximum ambient temperature	50 °C
Conducted EMI	In acc. with EN55022 Class-B
PCB type and size	Single side, 35 um, CEM-1, 140 x 60 mm

The main feature of this converter is that the input current is almost in phase with the mains voltage; therefore the power factor is close to unity. This is achieved by the controller, the L6564, shaping the input current as a sinewave in phase with the mains voltage. The topology of this power supply is a typical flyback converter using a transformer to provide the required insulation between the primary and secondary side. The converter is connected after the mains rectifier and the capacitor filter that, in this case, is very small so as not to affect the shape of the input current. The flyback switch is represented by the Power MOSFET Q1, driven by the L6564. The board is equipped with an input EMI filter designed for a 2-wire input mains plug. It is made up of one common mode line-filter stage connected after the input connector. A varistor is also connected at the input of the board, improving the immunity against input voltage fast transients.

At startup the L6564 is powered by the Vcc capacitor (C8) that is charged via the startup network made up of R3, R4, R7, D2, DZ2, Q2 and PTC1. When the device begins to switch, this network is opened by the diode DZ6, R2, R43 and Q3, decreasing the power dissipation during normal operation. After startup operation, the L6564 is supplied by the T1 auxiliary winding (pins 5-6) generating the Vcc voltage rectified by D5 and R17. The auxiliary winding is also connected with R33, providing the transformer demagnetization signal to the L6564 ZCD pin, turning on the MOSFET at any switching cycle.

The voltage on the auxiliary is even used to detect an abrupt rise of the output voltage or a feedback disconnection via the diodes D5 and D6 and the divider made up of R32 and R12. When the voltage on the INV pin (#1) is lower than 1.66 V and the PFC_OK pin (#5) is greater than 2.5 V, the OVP is active and the L6564 is latched.

The MOSFET is the STF11NM80, a standard and inexpensive 800 V device housed in a TO-220FP package. The rectifier D3, the Transil DZ1 and capacitor C12 clamp the peak

voltage spike at MOSFET turn-off. The resistor R10 senses the current flowing into the transformer primary side. Once the signal at the current sense pin via resistor R11 has reached the level programmed by the internal multiplier of the L6564, the MOSFET turns off.

The divider R1, R5, R8 and R13 provides, to the L6564 multiplier pin (#3), the information of the instantaneous voltage used to modulate the current flowing into the transformer primary side. The capacitor C16 and the parallel resistor R14 complete an internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage signal at this pin, a DC level equal to the peak voltage on pin #3 (MULT), is provided to a second input to the multiplier for 1/V2 function necessary to compensate the control loop gain dependence on the mains voltage.

Additionally, pin VFF (#5) is internally connected to a comparator providing the brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The L6564 restarts as the voltage at the pin rises above 0.88 V. The transformer is layer type, using a standard ferrite size EER-28L, manufactured by Magnetica. The flyback reflected voltage is ~140 V, providing enough room for the leakage inductance voltage spike with still enough margin for reliability of the MOSFET.

Employing the L6564 ensures a cleaner current sinewave than the old PFC devices (with L6562D/L6562A the startup resistance on pin INV was necessary) and it implements the VFF function, especially useful in wide-range input voltage, to have a more constant overload protection regardless of mains voltage. Moreover, the L6564 offers a better immunity against external noise thanks to the characteristics of its OVP function (without current OVP) and a dedicated function to manage the Burst mode condition is even available.

On the secondary stage, the divider R26, R28 and R42, is dedicated to sensing the output voltage. Capacitor C17 and diodes D7 and D8 provide a soft-start at turn-on. The output regulation is done by means of an isolated voltage loop by the optocoupler U1 and using an inexpensive TS2431A (U4) to drive it. The optotransistor modulates the input voltage of the L6564 internal amplifier via R31 and R35. R21, R25 and C21 close the voltage loop. The output rectifier is a fast recovery type, selected according to the maximum reverse voltage, forward voltage drop and power dissipation. A small LC filter has been added on the output, filtering the high frequency ripple.

2 Electrical diagram and bill of material

Figure 2. EVL6564-50WFLB demonstration board: electrical schematic

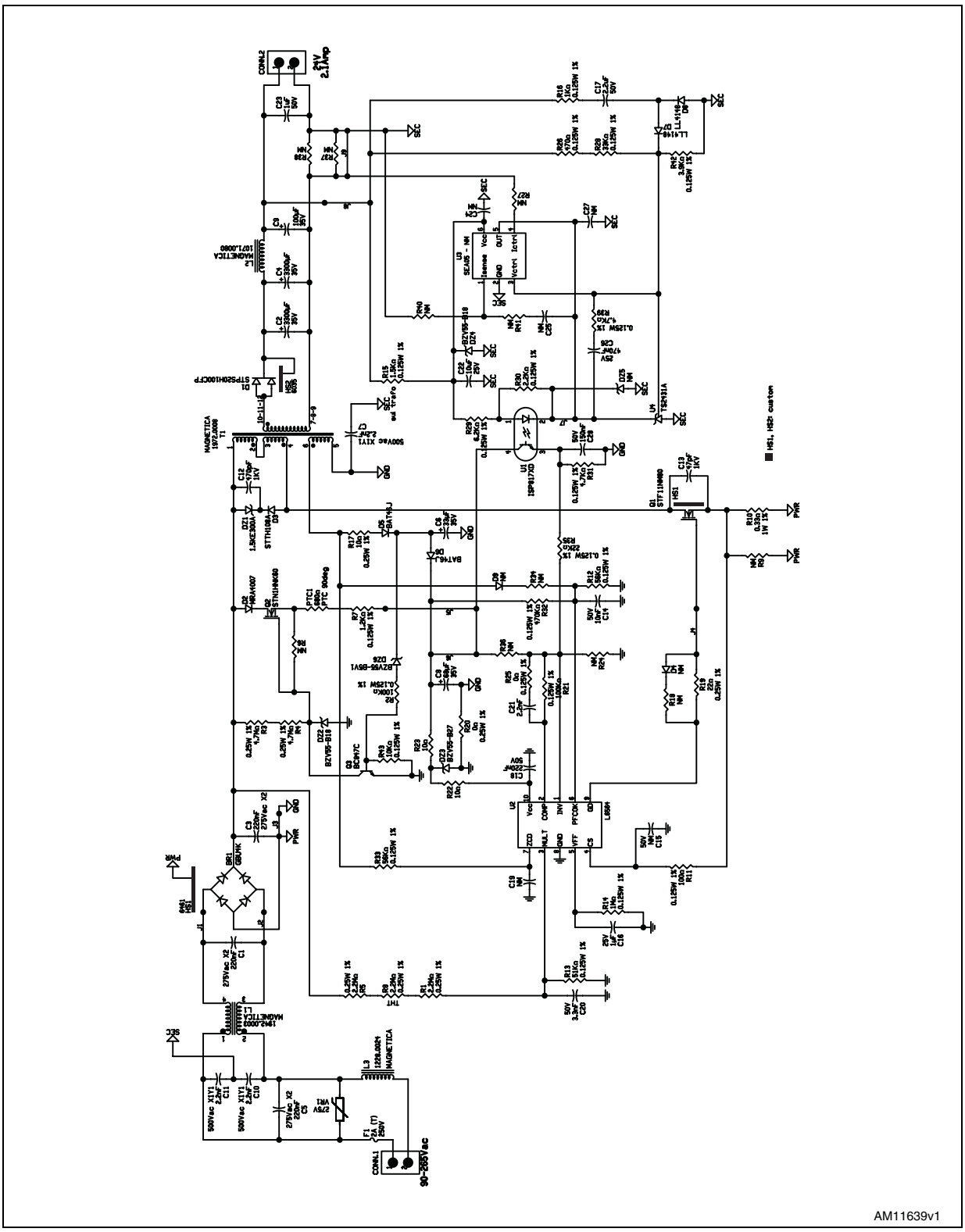


Table 2. Bill of material

Des.	Part type/part value	Case/package	Description	Supplier
BR1	GBU 4K	Style GBU	Bridge rect. 4 A 800 V	Vishay
Conn .1	V_{AC}-IN	MKDS 1.5/2-5.08-PS.5.08	Conn.MKDS 1.5/2-5.08-PS.5.08	Phoenix
Conn .2	V_{DC}-OUT	MKDS 1/2-3.81-PS.3.81	Conn.MKDS 1/2-3.81 - PS.3.81	Phoenix
C1	220 nF	DWG	X2 filmcap-R46-560 V_{DC} PS15	Arcotronics
C3	220 nF	DWG	X2 filmcap R46-560 V_{DC} PS15	Arcotronics
C5	220 nF	DWG	X2 filmcap R46-560 V_{DC} PS15	Arcotronics
C2	3300 uF	DWG	Aluminium Elcap 105 °C	Panasonic
C4	3300 uF	DWG	Aluminium Elcap 105 °C	Panasonic
C6	33 uF	DWG	Aluminium Elcap 105 °C	Rubycon
C7	2.2 nF	DWG	CERCAP.X1/Y1 +- 20% B-PS10	Vishay
C10	2.2 nF	DWG	CERCAP.X1/Y1 +- 20% B-PS10	Vishay
C11	2.2 nF	DWG	CERCAP.X1/Y1 +- 20% B-PS10	Vishay
C8	68 uF	DWG	Aluminium Elcap 105 °C	Panasonic
C9	100 uF	DWG	Aluminium Elcap 105 °C	Rubycon
C12	470 pF	1206	Aluminium Elcap 105 °C-X7R 10% 1206-SMD	AVX
C13	47 pF	1206	CAP.HV-COG-NP0-10% EIA1206-SMD	AVX
C14	10 nF	0805	CERCAP-X7R 10%-EIA0805-SMD	Murata
C26	470 nF	0805	CERCAP-X7R 10%-EIA0805-SMD	Murata
C16	1 uF	0805	CERCAP-X7R 10%-EIA0805-SMD	Murata
C17	2.2 uF	1206	CERCAP-X7R 10%-EIA1206-SMD	Murata
C18	0.22 uF	1206	CERCAP.X7R 10% EIA1206-SMD	Kemet
C20	3.3 nF	0805	CAP.X7R 10% EIA0805-SMD	Kemet
C21	2.2 nF	0805	CAP.X7R 10% EIA0805-SMD	Kemet
C22	10 uF	1206	CERCAP-X5R 10%-EIA1206-SMD	Murata
C23	1 uF	1206	CERCAP-X7R 10%-EIA1206-SMD	Murata
C28	150 nF	1206	CERCAP-X7R 10%-EIA1206-SMD	Murata
DZ1	1.5KE300A	DO201	TVS.-UNID.1500 Wp	ST
DZ2	BZV55-B18	SMD	Diode-Zener-2%-Sz 14.4 mV/K-SMD	NXP
DZ4	BZV55-B18	SMD	Diode-Zener-2%-Sz 14.4 mV/K-SMD	NXP
DZ3	BZV55-B27	SMD	Diode-Zener-2%-Sz 22.7 mV/K-SMD	NXP
DZ6	BZV55-B5V1	SMD	Diode-Zener-2%-Sz 6.4 mV/K-SMD	NXP
D1	STPS20H100CFP	TO220	Diode-Schottky–Vf 0,77 V@25 °C 10 A	ST
D2	MRA4007	SMD	Diode-Rect.SMD-MKR17	ON-MRA4007T3

Table 2. Bill of material (continued)

Des.	Part type/part value	Case/package	Description	Supplier
D3	STTH108A	SMD	Diode-ultrafast-75nS-SMD-MK H08	ST
D5	BAT46J	SMD	Diode-Schottky-SMD-MK 46	ST
D6	BAT46J	SMD	Diode-Schottky-SMD-MK 46	ST
D7	LL4148	SMD	Diode-fast-4nS-COL. B/G-SMD	Fairchild
D8	LL4148	SMD	Diode-fast-4nS-COL. B/G-SMD	Fairchild
D9	NM	Not mounted		
F1	Fuse	DWG	Fuse A 250 V 8.5x4-392/TE05-time-lag	Littelfuse
HS1	Heatsink	DWG	Heatsink for BR1&Q1	Magnetica
HS2	Heatsink	DWG	Heatsink for D1	Magnetica
J1	PS20mm	Jumper 0 Ω	Jumper 0 Ω	
J2	PS12mm	Jumper 0 Ω	Jumper 0 Ω	
J3	PS5mm	Jumper 0 Ω	Jumper 0 Ω	
J6	PS5mm	Jumper 0 Ω	Jumper 0 Ω	
J9	PS5mm	Jumper 0 Ω	Jumper 0 Ω	
J4	PS10mm	Bridge 0 Ω	Bridge 0 Ω	
J5	PS21mm	Jumper 0 Ω	Jumper 0 Ω	
J7	PS7.5mm	Jumper 0 Ω	Jumper 0 Ω	
J8	PS7.5mm	Jumper 0 Ω	Jumper 0 Ω	
L1	19mH-1942.0003	DWG	Com.mode chokes-270 V_{AC} max.	Magnetica
L2	3uH-1071.0080	DWG	Diff.chokes-drum core-10 mO hm	Magnetica
L3	320uH-1228.0024	DWG	Differential chokes	Magnetica
PTC1	680	0805	PTC-680 Ω90 °C SMD	Epcos
Q1	STF11NM80	TO220FP	MOSF-N-0.4 Ω - tr/tf 17/15ns-Ins.2500 V_{DC}	ST
Q2	STN1HNK60	TO92	MOSF-N-8 Ω - MK-N1HNK60	ST
Q3	BC847C	SMD	BJT.NPN SMD-MK1G	NXP
R1	2.2 M	PTH	Res.1%	Vishay
R2	100 K	PTH	Res.1%	Vishay
R3	4.7 M	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R4	4.7 M	1206	RES.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R5	2.2 M	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R8	2.2 M	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R7	1.2 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R10	0.33	1210	Res.1% EIA1210-SMD	Panasonic
R11	100	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R12	56 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay

Table 2. Bill of material (continued)

Des.	Part type/part value	Case/package	Description	Supplier
R13	51 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R14	1 M	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R15	1.5 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R16	1 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R17	10	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R19	22	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R20	0	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R21	100 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R22	10	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R23	10	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R25	0	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R26	470	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R28	33 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R29	6.2 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R30	2.2 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R31	4.7 K	1206	Res.1%-200 $V_{AC/DC}$-EIA1206-SMD	Vishay
R32	470 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R33	56 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R34	Not mounted	Not mounted		
R35	22 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R39	4.7 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R42	3.9 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
R43	10 K	0805	Res.1%-150 $V_{AC/DC}$-EIA0805-SMD	Vishay
T1	1972.0008	Power transformer	Transf. flyback 24 V/2.1 A-50 Khz-450 uH	Magnetica
U1	ISP817XD	OPTOIS.35V CTR300-	OPTOIS.35 V CTR300-600% PS.300 mls	Isocom
U2	L6564	SSOP-10	Transition-mode PFC controller	ST
U4	TS2431A	SOT23	PROG. Shunt voltage reference	ST
VR1	275 V	DWG	VDR-275 V_{AC}-350 V_{DC}-40 J(10/1000usec)D7 mm	Panasonic

Note: C28 and R43 have been added as a new reworking position.

3 Test results and significant waveforms

3.1 Harmonic content measurement

One of the main purposes of this converter is the correction of input current distortion, decreasing the harmonic contents below the limits of the actual regulations. Therefore, the board has been tested according to the European standard EN61000-3-2 Class-C and Japanese standard JEIDA-MITI Class-C, at full load and both the nominal mains input voltages. As reported in the following figures, the circuit is capable of reducing the harmonics well below the limits of both regulations.

Figure 3. EVL6564-50WFLB compliance with EN61000-3-2 Class-C limits @ full load

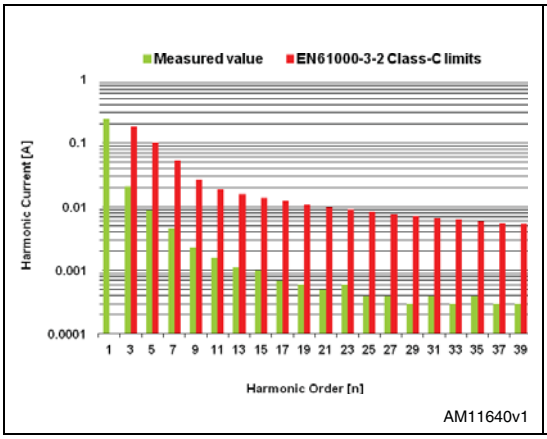
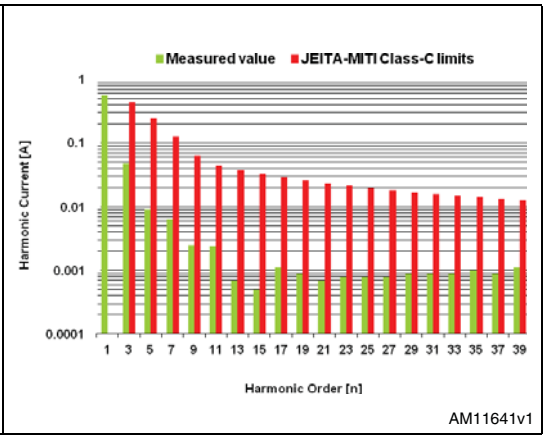


Figure 4. EVL6564-50WFLB compliance with JEIDA-MITI Class-C limits @ full load



3.2 Power factor, Vout and total harmonic distortion

The power factor (PF) has also been measured and the results are reported in *Figure 5*. As seen, the PF remains very close to unity throughout the input voltage mains range and it is also higher than 0.9 for a load equal to or greater than 50% of nominal load.

Figure 5. EVL6564-50WFLB power factor vs. V_{IN} & load

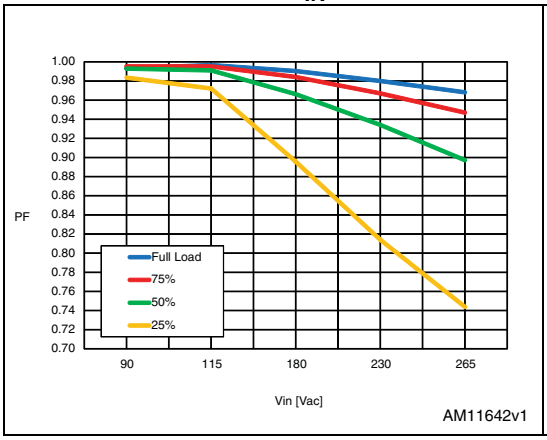


Figure 6. EVL6564-50WFLB static Vout regulation vs. V_{IN} & load

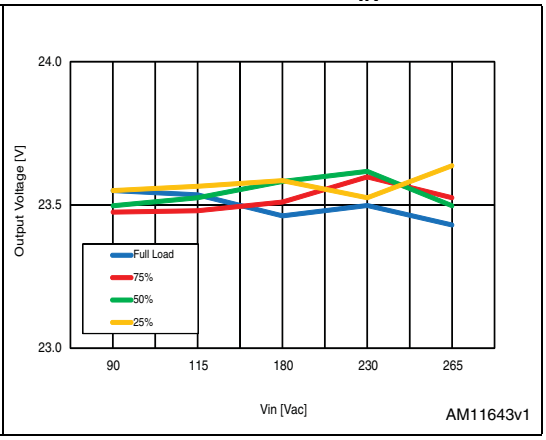
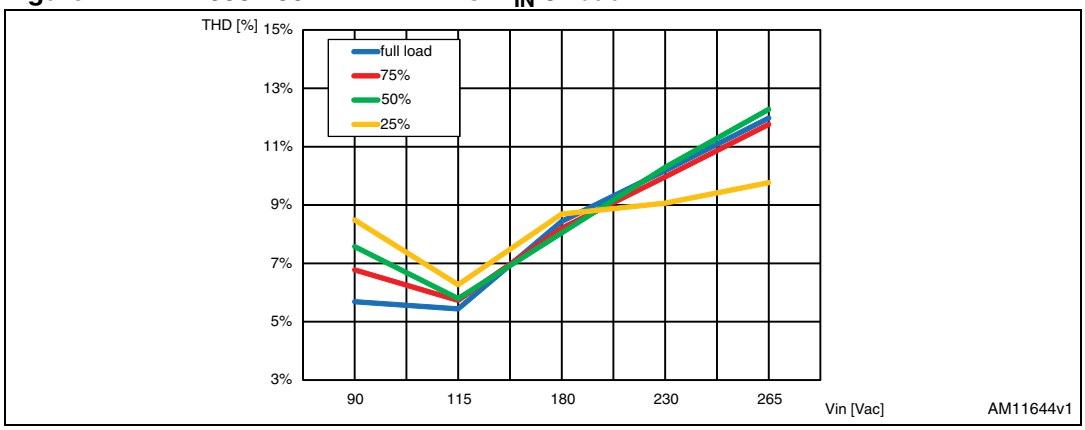


Figure 6 reports the output voltage measured at different line and load conditions. As seen, the voltage regulation over all the input voltage range is excellent at any output power level.

Total harmonic distortion (THD) has been measured too and the results are reported in *Figure 7*.

Figure 7. EVL6564-50WFLB THD vs. V_{IN} & load



3.3 Efficiency and light load performance

The converter efficiency has been measured and it is significantly high at all load and line conditions. The data are reported in *Figure 8*. At full load the efficiency is about 90% (88.6% at 90 V_{INAC} is the worst condition), making this design suitable for high efficiency power supplies. Also at lower output load (25% of nominal load @ 265 V_{INAC}), the efficiency is always better than 84%.

Figure 8. EVL6564-50WFLB efficiency vs. V_{IN} & load @ full load

Figure 9. EVL6564-50WFLB efficiency vs. V_{IN} & Pout @ low load

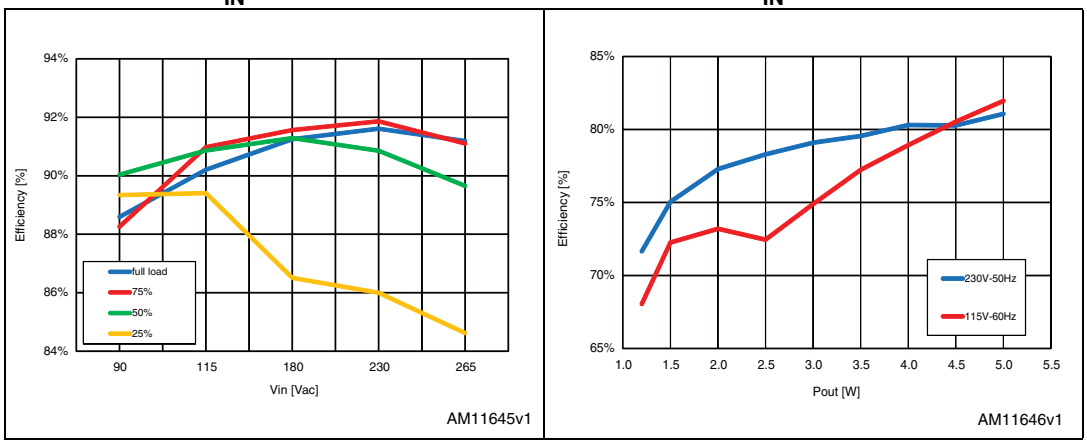


Figure 9 shows the efficiency with Pout minor, equal to 5 W. As seen, the efficiency is about 65% for output power of 1.2 W, crossing even 80% when the output power is 5 W. This measurement has been taken with 115 and 230 V_{INAC}. However, to better understand the efficiency in full load conditions and during low load operations see *Table 3* and *Table 4*.

Table 3. Efficiency full load

Test condition	Item[%]	Pin[W]	Pout[W]	Eff.[%]	Av. eff.[%]
115 V-60 Hz	100	54.690	49.334	90.21	90.36
	75	40.726	36.580	90.98	
	50	27.086	24.612	90.87	
	25	13.739	12.283	89.40	
230 V-50 Hz	100	53.769	49.257	91.61	90.08
	75	40.364	37.080	91.86	
	50	27.195	24.708	90.86	
	25	14.259	12.262	86.00	

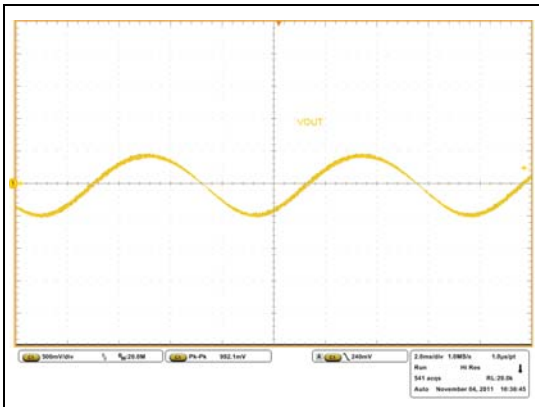
Table 4. Low power efficiency

230 V-50 Hz					115 V-60 Hz				
Pin	V_{OUT}	Iout[mA]	Pout	Eff.[%]	Pin[W]	Vout	Iout [mA]	Pout[W]	Eff.[%]
6.12	23.65	0.21	4.96	81.07	6.04	23.63	0.21	4.95	81.96
5.53	23.54	0.19	4.44	80.27	5.53	23.59	0.19	4.45	80.53
4.94	23.65	0.17	3.96	80.31	5.01	23.59	0.17	3.95	78.93
4.35	23.59	0.15	3.46	79.55	4.49	23.64	0.15	3.47	77.24
3.75	23.64	0.13	2.97	79.10	3.97	23.61	0.13	2.97	74.89
3.16	23.61	0.10	2.47	78.29	3.42	23.61	0.10	2.47	72.46
2.56	23.65	0.08	1.98	77.29	2.70	23.63	0.08	1.98	73.20
1.97	23.64	0.06	1.48	75.05	2.05	23.62	0.06	1.48	72.26
1.62	23.62	0.05	1.16	71.66	1.71	23.63	0.05	1.16	68.06

3.4 Output voltage ripple

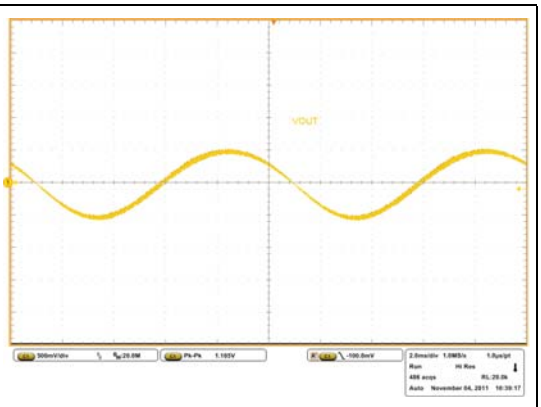
In *Figure 10* and *Figure 11* the output voltage ripple with 115 and 230 V_{INAC} input mains has been captured. As seen, Vout voltage pk-pk is about 1 volt.

Figure 10. EVL6564-50WFLB output voltage ripple at 115 V_{AC} - full load_1 V pk-pk



CH1: VOUT AM11647v1

Figure 11. EVL6564-50WFLB output voltage ripple at 230 V_{AC} - full load_1.1 V pk-pk

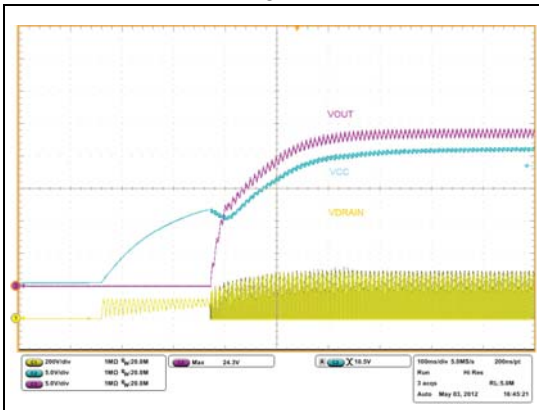


CH1: VOUT AM11648v1

3.5 Startup

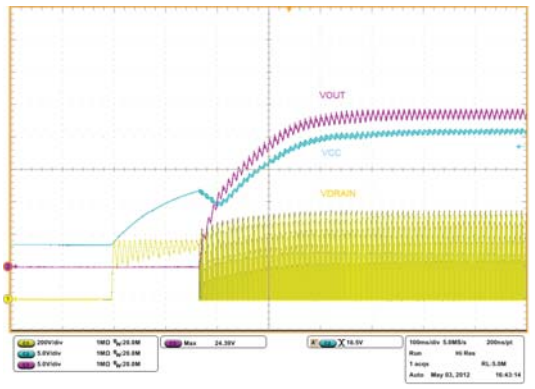
Figure 12 and *Figure 13* show the rising slope of the output voltage during the startup operations. The images show as Vout rises and reaches 24 V, without anomalous behavior.

Figure 12. EVL6564-50WFLB startup @ 90 V_{AC} - full load



CH1: VDRAIN
CH2: VCC
CH3: VOUT AM11649v1

Figure 13. EVL6564-50WFLB startup @ 265 V_{AC} - full load

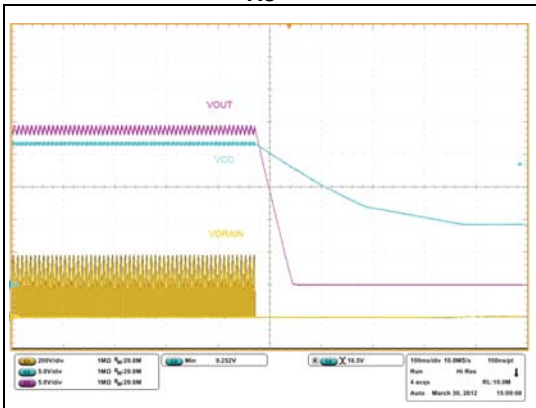


CH1: VDRAIN
CH2: VCC
CH3: VOUT AM11650v1

3.6 Turn off

Even during turn-off operations, the transition is clean without any abnormal behavior. *Figure 14* and *Figure 15* below, show turn-off events with 90 and 265 V_{INAC} mains input voltage.

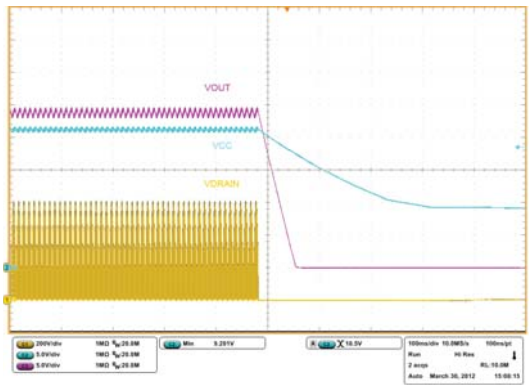
Figure 14. EVL6564-50WFLB turn-off @ 90 V_{AC} - full load



CH1: VDRAIN
CH2: VCC
CH3: VOUT

AM11651v1

Figure 15. EVL6564-50WFLB turn-off @ 265 V_{AC} - full load



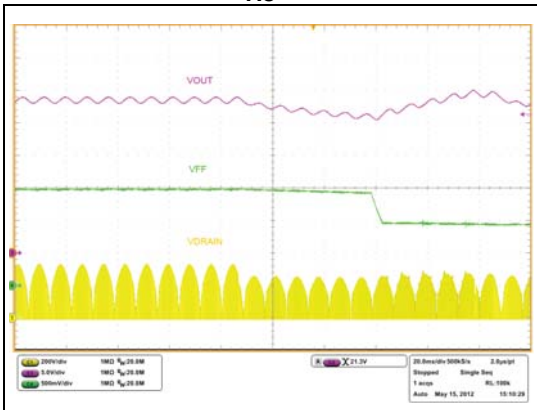
CH1: VDRAIN
CH2: VCC
CH3: VOUT

AM11652v1

3.7 Voltage feed-forward and brownout function

The L6564 realizes an innovative voltage feed-forward which, with a technique that makes use of just two external parts, overcomes time constant trade-off issues whichever voltage change occurs on the mains. Moreover, VFF function is useful in wide-range input voltage, to have a more constant overload protection regardless of mains voltage, as previously described. *Figure 16* to *Figure 19* show Vout behavior during input mains dip and surge.

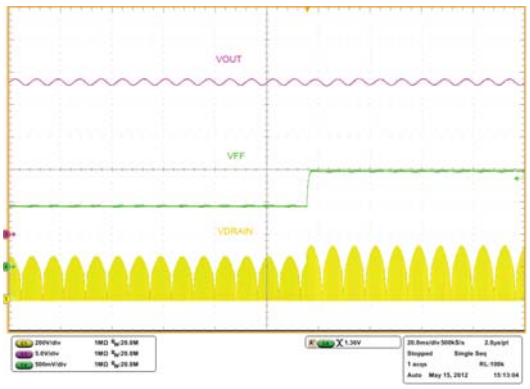
Figure 16. EVL6564-50WFLB input mains dip 140 V_{AC} to 90 V_{AC} @ full load



CH1: VDRAIN
CH3: VOUT
CH4: VFF

AM11653v1

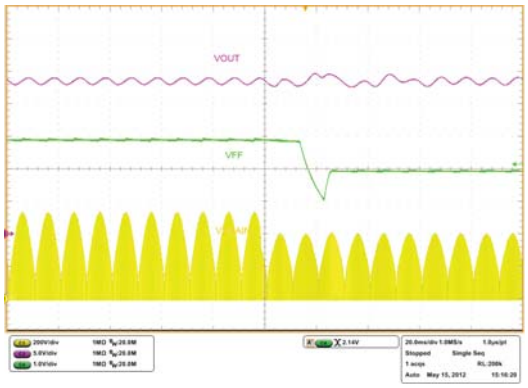
Figure 17. EVL6564-50WFLB input mains surge 90 V_{AC} to 140 V_{AC} @ full load



CH1: VDRAIN
CH3: VOUT
CH4: VFF

AM11654v1

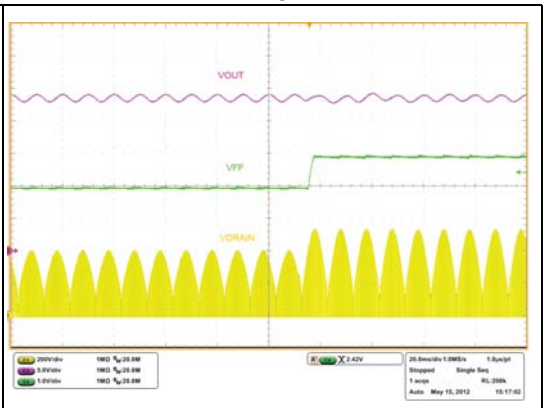
Figure 18. EVL6564-50WFLB input mains dip 265 V_{AC} to 185 V_{AC} @ full load



CH1: VDRAIN
CH3: VOUT
CH4: VFF

AM11655v1

Figure 19. EVL6564-50WFLB input mains surge 185 V_{AC} to 265 V_{AC} @ full load



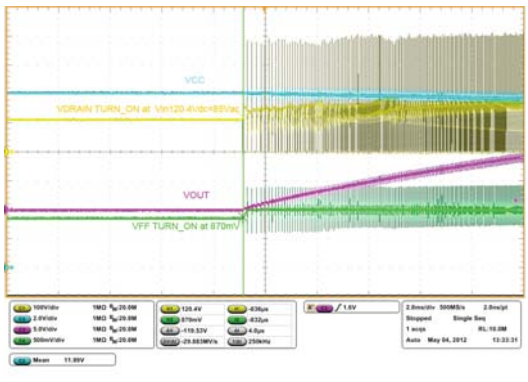
CH1: VDRAIN
CH3: VOUT
CH4: VFF

AM11656v1

Brownout thresholds are internally fixed at 0.88 V (typ.) for enabling operation and 0.8 V (typ.) for disabling the L6564. Sensing of the input mains condition is done by an internal comparator connected to pin VFF (#5) which delivers a voltage signal proportional to the peak input mains.

Figure 20 shows startup behavior and *Figure 21* shows the turn-off operation. In order to highlight a cleaner VFF brownout threshold behavior, DC input voltage has been used.

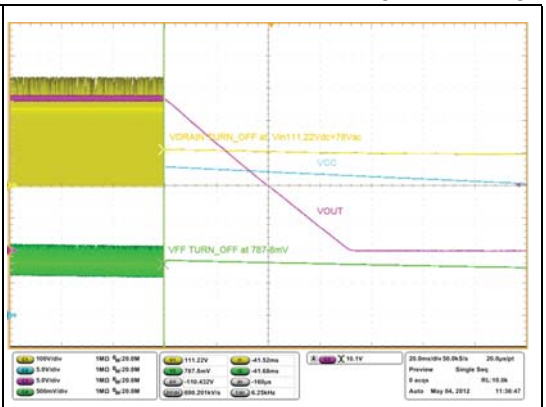
Figure 20. EVL6564-50WFLB brownout startup 120 V_{DC} = 85 V_{INAC}



CH1: VDRAIN
CH2: VCC
CH3: VOUT
CH4: VFF

AM11657v1

Figure 21. EVL6564-50WFLB brownout shutdown 111 V_{DC} = 78 V_{INAC}



CH1: VDRAIN
CH2: VCC
CH3: VOUT
CH4: VFF

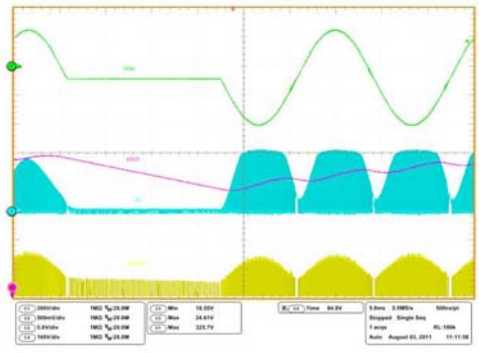
AM11658v1

3.8 Line sag

Figure 22 and *Figure 23* show the V_{INAC} line sag events. In this case, for 1 cycle during normal operations, V_{INAC} disappears. As seen, after a few cycles Vout rises and reaches its nominal voltage level (24 V).

.

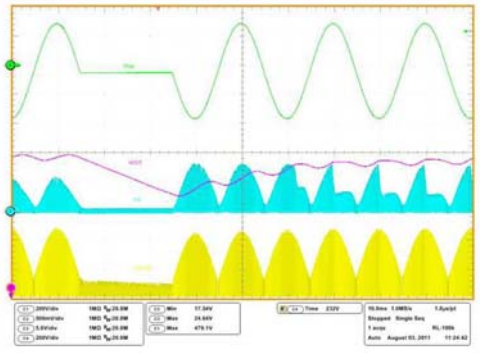
Figure 22. EVL6564-50WFLB line sag for 1 cycle @ 115 V_{INAC} full load



CH1: VDRAIN
CH2: VCS
CH3: VOUT
CH4: V_{INAC}

AM11659v1

Figure 23. EVL6564-50WFLB line sag for 1 cycle @ 230 V_{INAC} full load

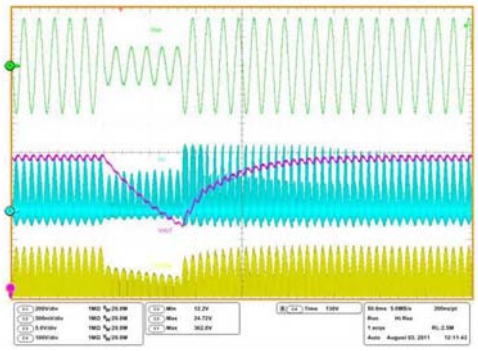


CH1: VDRAIN
CH2: VCS
CH3: VOUT
CH4: V_{INAC}

AM11660v1

Figure 24 and *Figure 25* show other line sag cases. During normal operations, for 5 cycles, V_{INAC} works at 60% of its nominal input voltage amplitude. Even in this case, Vout rises at 24 V (nominal output voltage) and the loop is again in steady-state condition.

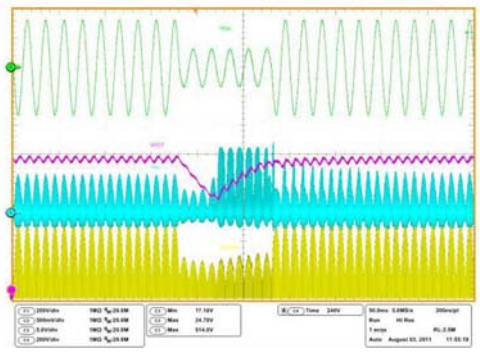
Figure 24. EVL6564-50WFLB line sag for 5 cycles at 60% @ 115 V_{INAC} full load



CH1: VDRAIN
CH2: VCS
CH3: VOUT
CH4: V_{INAC}

AM11661v1

Figure 25. EVL6564-50WFLB line sag for 5 cycles at 60% @ 230 V_{INAC} full load



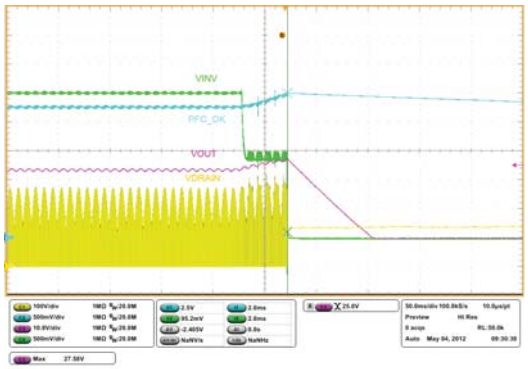
CH1: VDRAIN
CH2: VCS
CH3: VOUT
CH4: V_{INAC}

AM11662v1

3.9 Feedback failure (open loop) protection

Protection against the failure of the feedback circuitry is a must for any power supply. If this occurs, the output voltage can get high values, depending on the load and the transformer coupling between the windings. Here below, in *Figure 26* and *Figure 27*, as visible, when the voltage on the PFC_OK pin surpasses 2.5 V, and at the same time the VINV pin is below 1.66 V, the L6564 is latched off. Through the auxiliary transformer and via the diode D5, D6 and the divider made up of R32 and R12, the output overvoltage is triggered on the PFC_OK pin. The L6564 OVP is triggered on the voltage loop, offering a better immunity against external noise, as previously mentioned.

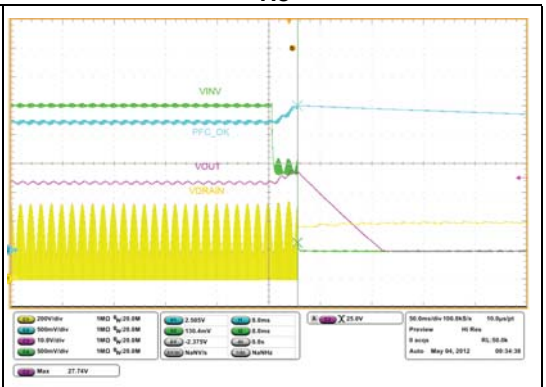
Figure 26. EVL6564-50WFLB feedback failure protection @ 90 V_{AC} - full load



CH1: VDRAIN
CH2: PFC_OK
CH3: VOUT
CH4: VINV

AM11663v1

Figure 27. EVL6564-50WFLB feedback failure protection @ 265 V_{AC} - full load



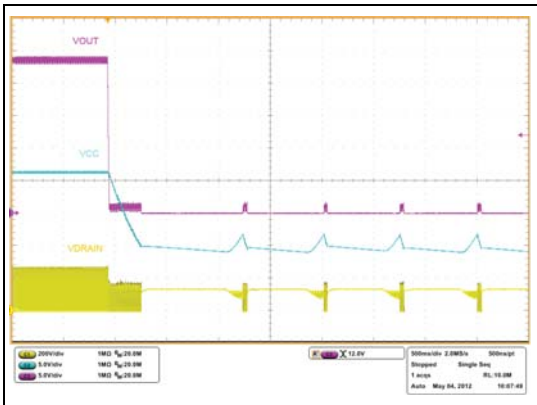
CH1: VDRAIN
CH2: PFC_OK
CH3: VOUT
CH4: VINV

AM11664v1

3.10 Short-circuit

An important function of any power supply is its ability to survive in the case of output overload or short-circuit, avoiding any consequent failure. Additionally, the power supply must be compliant with safety rules, requiring that, in the case of fault, no component can melt or burn out. *Figure 28* and *Figure 29* show the circuit behavior in the case of a short-circuit:

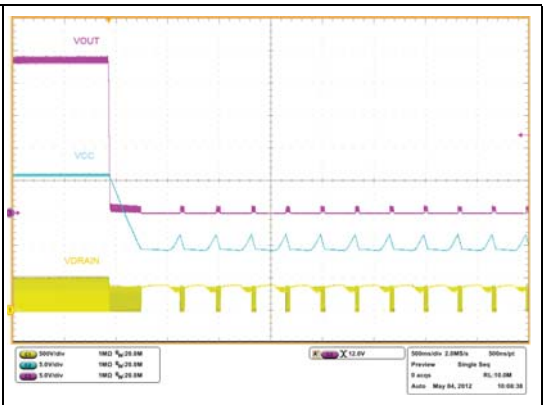
Figure 28. EVL6564-50WFLB short-circuit applied @ 90 V_{INAC} full load



CH1: VDRAIN
CH2: VCC
CH3: VOUT

AM11665v1

Figure 29. EVL6564-50WFLB short-circuit applied @ 265 V_{INAC} full load

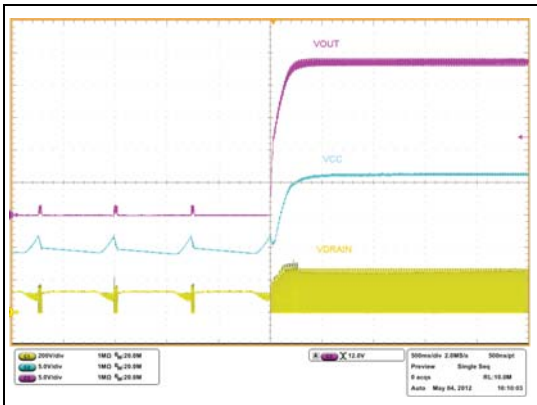


CH1: VDRAIN
CH2: VCC
CH3: VOUT

AM11666v1

In *Figure 30* and *Figure 31* the sequence of the operation in short-circuit when the short is removed is represented: as can be seen, a new startup sequence takes place and the circuit resumes normal operation.

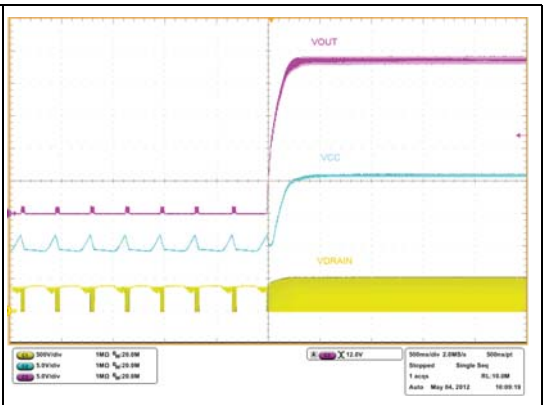
Figure 30. EVL6564-50WFLB short-circuit removed @ 90 V_{INAC} full load



CH1: VDRAIN
CH2: VCC
CH3: VOUT

AM11667v1

Figure 31. EVL6564-50WFLB short-circuit removed @ 265 V_{INAC} full load



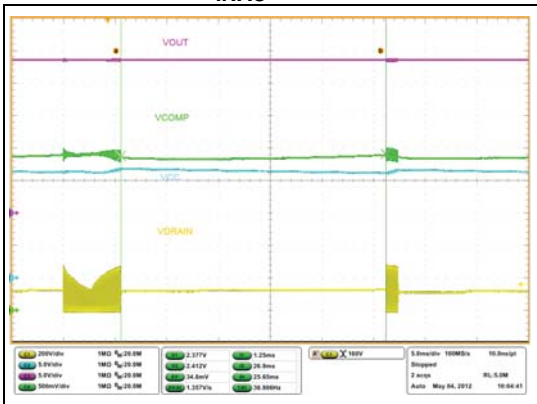
CH1: VDRAIN
CH2: VCC
CH3: VOUT

AM11668v1

3.11 No load

In *Figure 32* and *Figure 33*, some no load waveforms of the circuit are captured. When the control voltage on the COMP pin decreases below the Burst mode threshold of the L6564 (2.4V typ.), IC gate driver output is inhibited and its consumption reduced

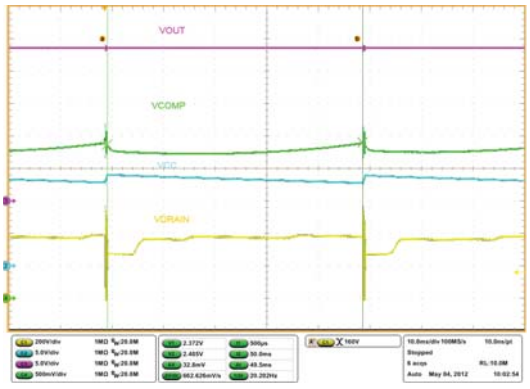
Figure 32. EVL6564-50WFLB 90 V_{INAC} @ no load



CH1: VDRAIN
CH2: VCC
CH3: VOUT
CH4: VCOMP

AM11669v1

Figure 33. EVL6564-50WFLB 265 V_{INAC} @ no load



CH1: VDRAIN
CH2: VCC
CH3: VOUT
CH4: VCOMP

AM11670v1

4 Thermal measurement

In order to check the design reliability, a thermal mapping by means of an IR camera was done. *Figure 34* and *Figure 35* show thermal measurements on the board component side at nominal input voltages and full load. Some pointers visible on the images placed across key components show the relevant temperature. The key component temperature is indicated in *Table 5* and *Table 6*.

Figure 34. Thermal map at 115 V_{AC} - full load

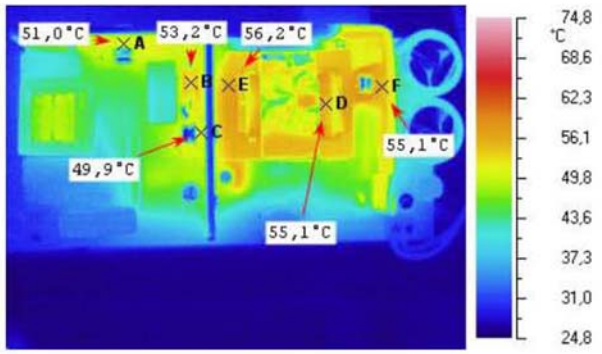


Table 5. Thermal temperature at 115 V_{AC} - full load

Point	Reference	Description	Temperature °C
A	BR1	Bridge rectifier	51
B	DZ1	Diode	53.2
C	Q1	MOSFET	49.9
D	T1	Trafo winding	55.1
E	T1	Trafo core	56.2
F	D1	Secondary diode	55.1

Figure 35. Thermal map at 230 V_{AC} - full load

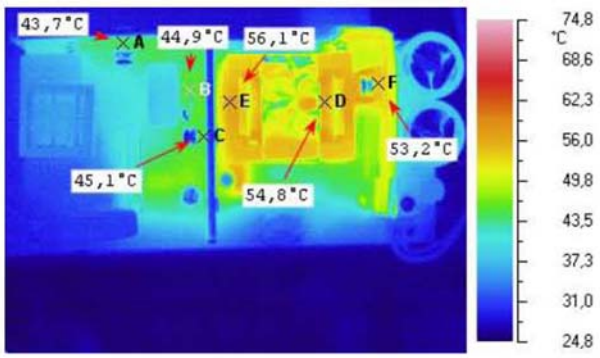


Table 6. Thermal temperature at 230 V_{AC} - full load

Point	Reference	Description	Temperature °C
A	BR1	Bridge rectifier	43.7
B	DZ1	Diode	44.9
C	Q1	MOSFET	45.1
D	T1	Trafo winding	54.8
E	T1	Trafo core	56.1
F	D1	Secondary diode	53.2

5 Conducted emission pre-compliance test

The following images are the quasi-peak measurement of the conducted noise at full load and nominal input mains voltages. The limits shown are the EN55022 Class-B ones, which is the most popular standard for domestic equipment. As seen in the diagrams, in all test conditions there is a good margin of the measurements with respect to the limits.

Figure 36. 115 V_{AC} at full load - phase

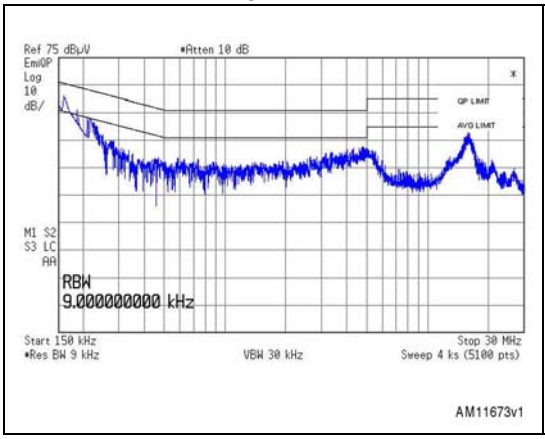


Figure 37. 115 V_{AC} at full load - neutral

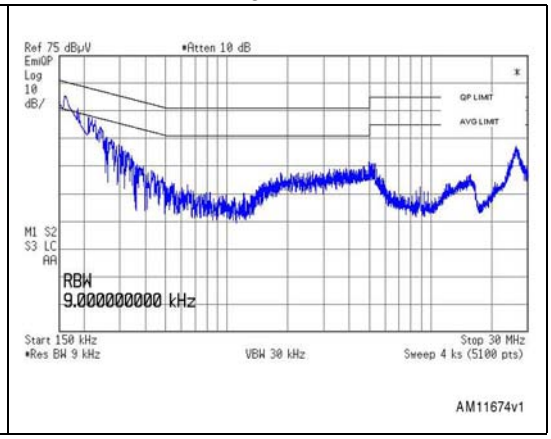


Figure 38. 230 V_{AC} at full load - phase

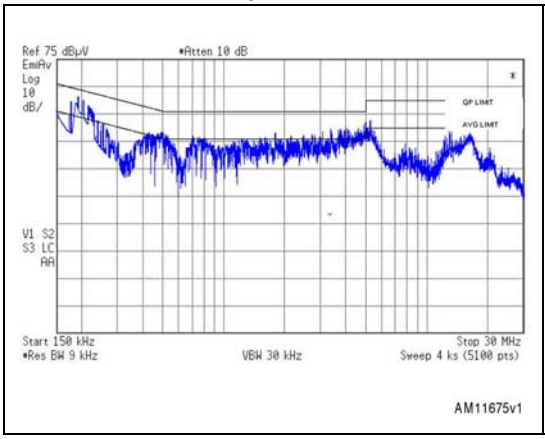
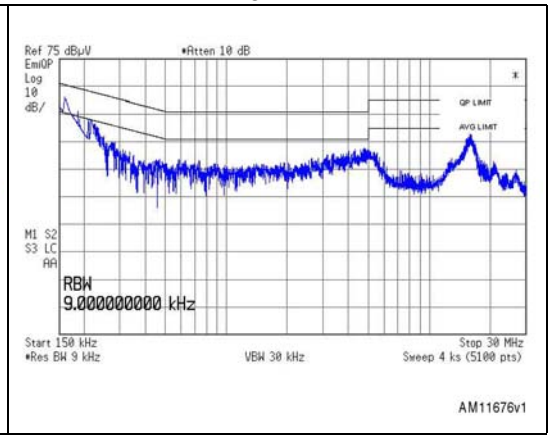


Figure 39. 230 V_{AC} at full load - neutral



6 Power transformer specification

6.1 General description and characteristics

- Application type: consumer, home appliance, lighting
- Transformer type: open
- Coil former: vertical type, 6+6 pins
- Mains insulation: 4kv
- Unit finishing: varnished

6.2 Electrical characteristics

- Converter topology: flyback TM
- Core type: ER28/17/11
- Operating freq.: 50Khz
- Primary inductance: 450 mH ±15% @1kHz-0.25V
- Leakage inductance: 0.9%
- Transformer ratio: -Pin 4-1/6-5: 6.85 ±5%; -Pin 4-1/10/11/12-7/8/9: 6 ±5%
- Primary peak current: 3.3 Apk

Figure 40. Electrical diagram

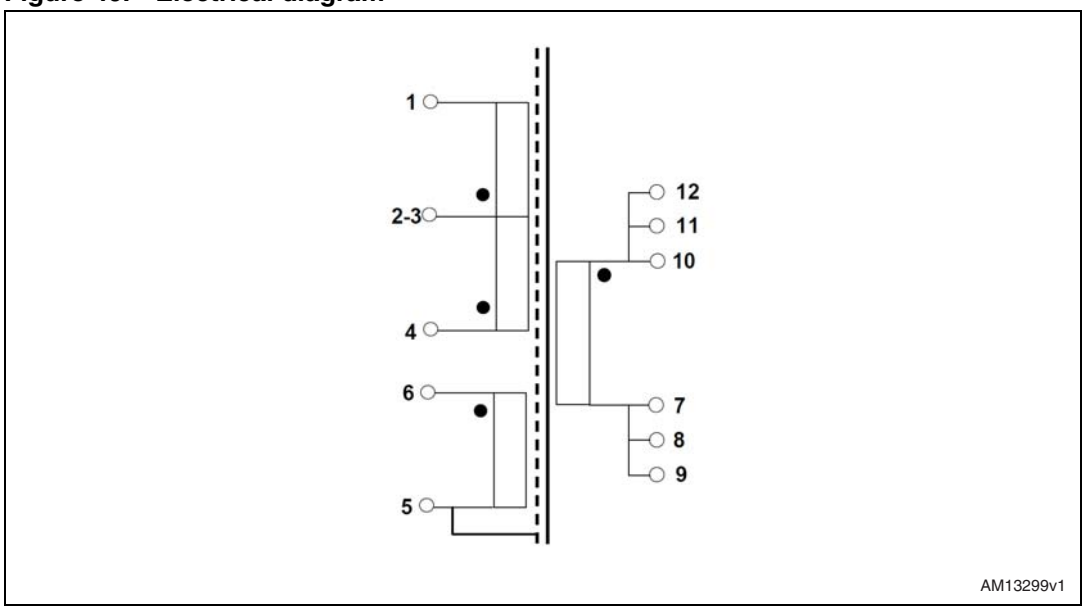


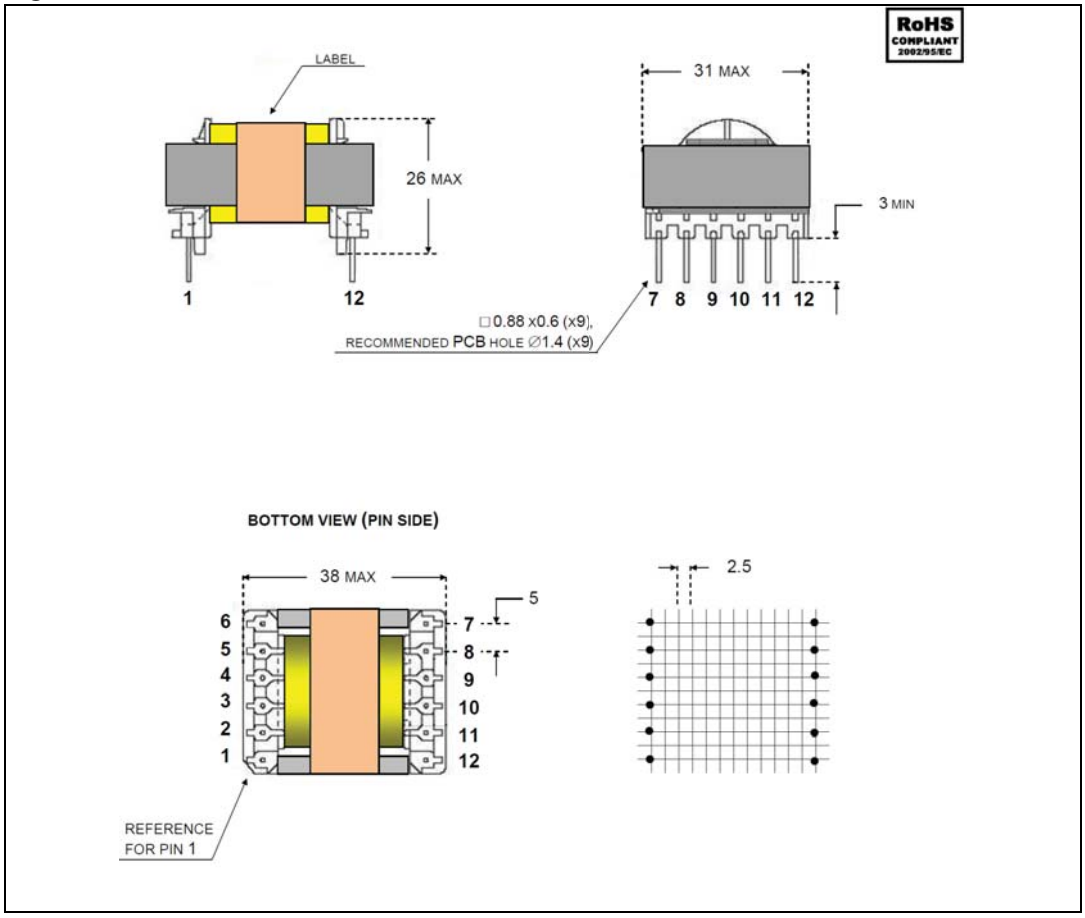
Table 7. Winding characterics tics

Windings	Start pins	End pins	Numberof turns
AUX	6	5	7
PRIM	1	2-3-4	48

6.3 Mechanical aspect and pin numbering

- Maximum Height from PCB: 26mm
- Coil former type: vertical, 6+6 pins
- Pin distance: 5 mm
- Row distance: 30 mm

Figure 41. Pin side view



Manufacturer:

- MAGNETICA di R. Volpini - Italy

7 References

1. L6564 datasheet
2. AN1059 application note
3. AN1060 application note
4. AN2838 application note.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
12-Sep-2012	1	Initial release.