UNITRODE

Design Note

## Controlling a –5V Rail Using the UCC3919, +3V to +8V Hot Swap Power Manager

By Dave Olson

This design note is intended to show the hot swap designer how to control a –5V rail using a UCC3919 Hot Swap Power Manager. The technique shown could also be applied using other positive Hot Swap Power Managers. Two circuit configurations are presented, one for systems with independent ground returns that will allow low side current sensing, and one for systems employing a common ground plane that require high side current sensing.

Fig. 1 shows the UCC3919 configured to control a –5V rail using low side (ground side) current sensing. As shown in fig 1, a positive 5V is established across the UCC3919 by connecting the IC's VDD pin to the interface ground or return lead, and the IC's GND pin to the –5V input. Using low side current sensing maintains the proper input common mode voltage range on the internal Linear Current Amplifier and Overcurrent comparators and therefore allows direct connection from the sense resistor to the CSP and CSN pins. The external n-channel MOSFET should be placed between the load and the input source (–5V) to provide adequate gate drive voltage when the load is switched on.

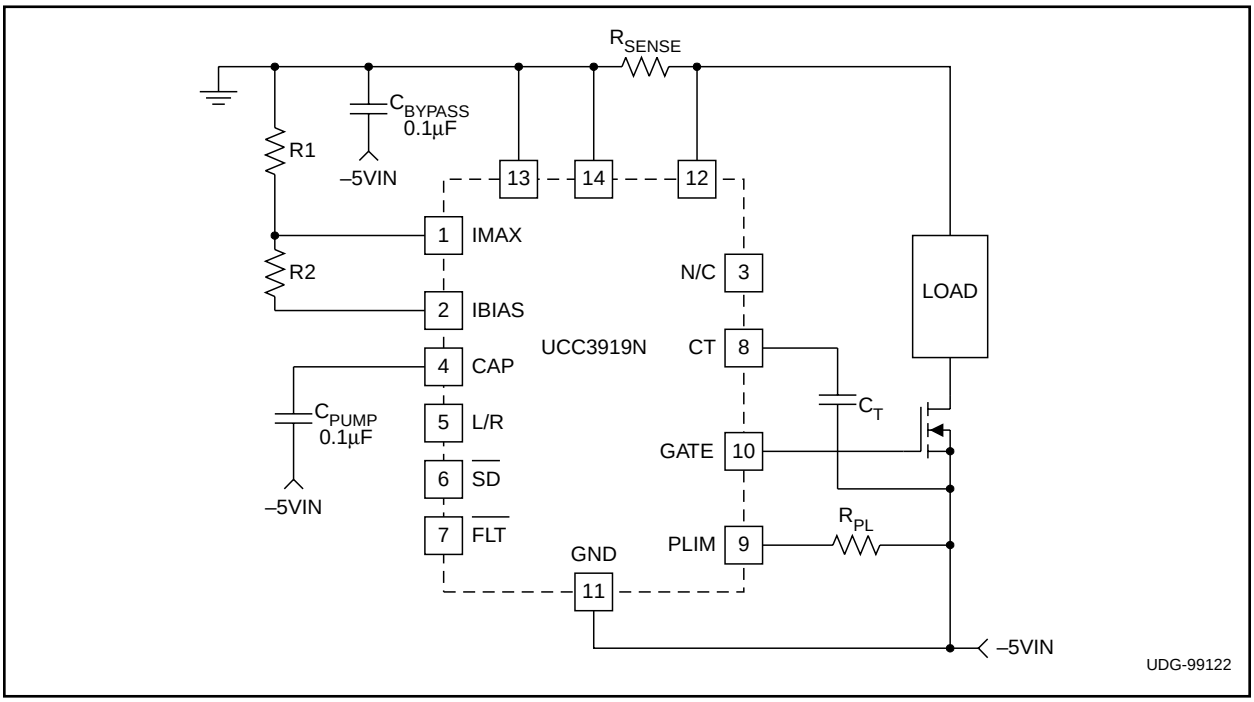


***Figure 1. Controlling a –5V Rail with the UCC3919 with low side current sensing.***

Fig. 2 shows the UCC3919 configured to control a –5V rail using high side (source side) current sensing. Because the voltage on the sense resistor is outside the acceptable common mode input range of the internal Linear Current Amplifier, level shift circuitry must be used. The current is sensed differentially using a low offset, rail-to rail input/output, op amp. The op amp translates the current sensed in the –5V rail to a voltage level in the common mode range of the internal Linear Current Amplifier for direct comparison to the IMAX pin. To minimize errors associated with the differential amplifier precision resistors should be used. Using 0.1% tolerance resistors provides a 9.5% $R_{SS}$ tolerance on the sensed current at $V_{SENSE}$ = 50mV.

It is important that the components and signal inputs which interface to the UCC3919 keep their correct voltage reference with respect to the IC. In other words, components referenced to the IC's GND pin should remain referenced to the IC's GND pin and components normally referenced to VDD should remain referenced to the VDD pin. Level shift circuitry will be required to interface the $\overline{SD}$, L/R and $\overline{FLT}$ pins to standard 5V logic. Possible level shift circuits for interfacing to the $\overline{SD}$, L/R, and $\overline{FLT}$ pins are shown in Fig. 3.

In either circuit configuration all IC or hot swap functions are maintained. However, operation of the power limit function changes slightly. Note that the voltage on $R_{PL}$ is fixed at –5V regardless of the voltage across the load. Therefore, the additional current injected into the fault timer capacitance will always be fixed at $I_{PL}$= VIN/$R_{PL}$. Equations (15) and (16) in the UCC3919 datasheet should use this value of $I_{PL}$ in place of $I_{PL}$(avg) listed on the datasheet. All other equations presented in the data sheet are valid.

***Please Note: The UCC3919 is not a floating Hot Swap Power Manager, absolute maximum voltage ratings must be adhered to.***

*For complete details about the operation of the UCC3919 Hot Swap Power Manager , please refer to the UCC3919 Data Sheet and the UCC3919 Application Note.*

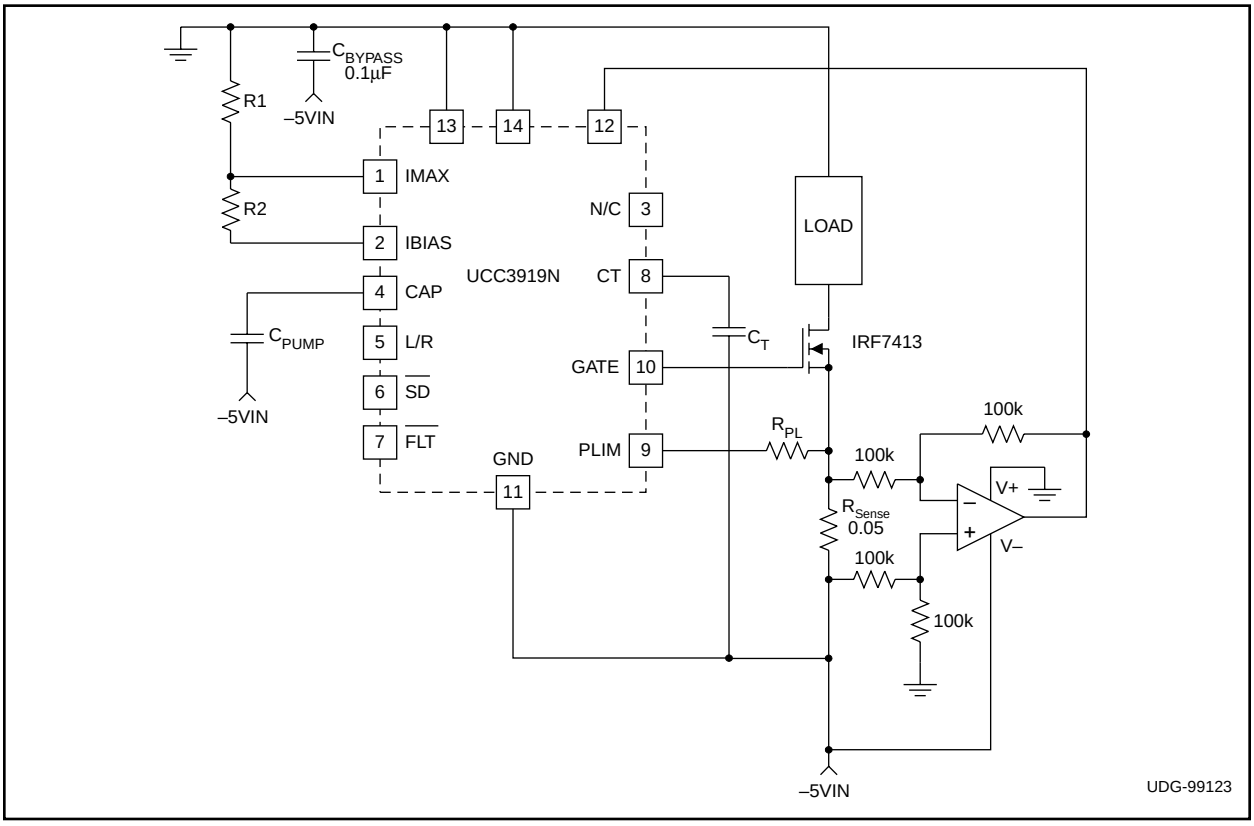


***Figure 2: Controlling a –5V rail using the UCC3919 with high side current sensing.***

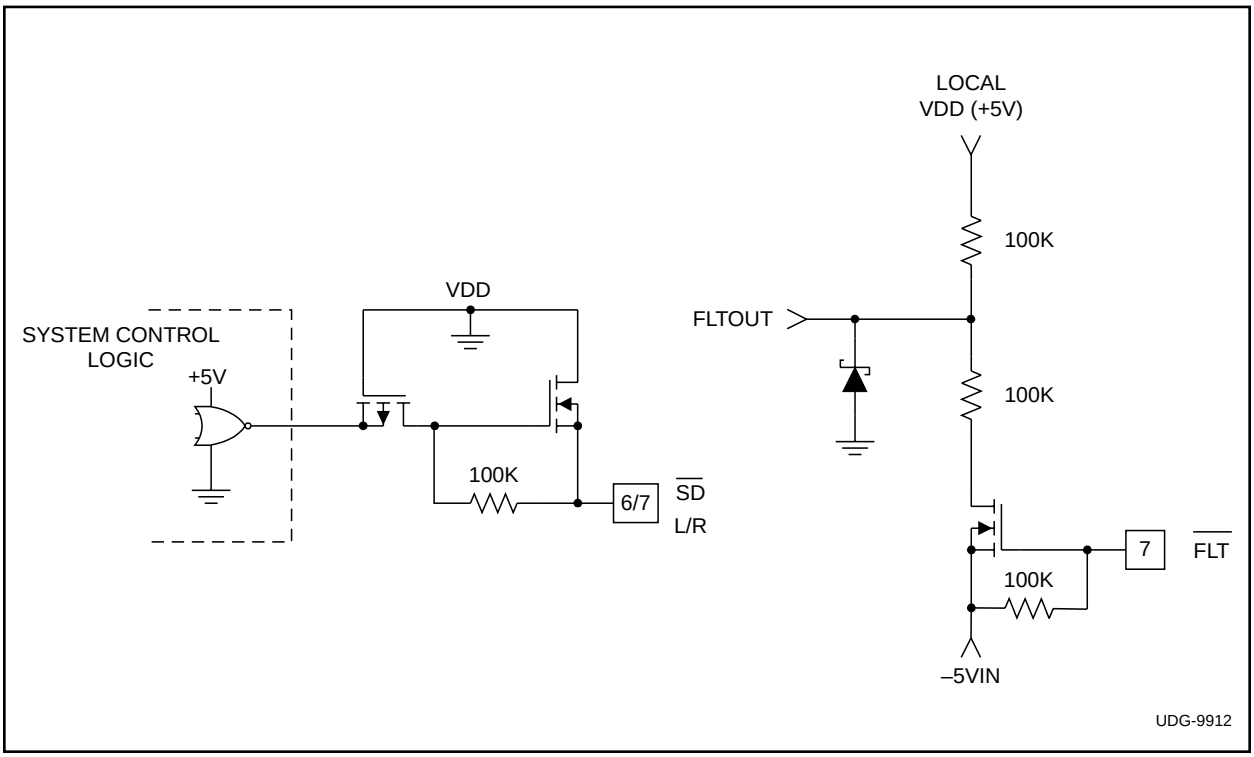


***Figure 3: Level shift circuitry for interfacing to the SD, FLT, and L/R pins.***

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