Application Report
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SIZING THE UCC3919 CHARGE-PUMP CAPACITOR

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ABSTRACT

The UCC3919 works in most hot-swap designs with the charge-pump capacitance recommended in the UCC3919 data sheet. However, this capacitance may be inadequate in high-current designs. This application report describes a method to size the charge-pump capacitance to ensure proper UCC3919 operation in any hot-swap design.

1 Introduction

An internal charge pump boosts the supply voltage to the UCC3919 linear current amplifier (LCA). This allows the LCA to drive a high-side, low-cost N-channel FET instead of a more expensive P-channel FET. Because of its high source impedance (i.e., 100 kΩ), the charge-pump output voltage droops when the LCA turns on the hot-swap FET. The amount of droop increases with the gate voltage slew rate and capacitance. If the droop is large enough to trip the charge-pump UVLO comparator, then the LCA shuts off, and it is not possible to turn on the FET. The UCC3919 data sheet recommends a 0.01-µF to 0.1-µF external charge-pump capacitor to provide adequate charge. This capacitance range is satisfactory for low-to-moderate current hot-swap designs. High-current hot-swap designs that use a larger FET require more capacitance. Instead of a *one size fits all* approach to selecting the charge-pump capacitance, an equation that customizes the charge-pump capacitance to the application is desirable. This application report presents a practical model of the UCC3919 and derives such an equation. This equation also applies to the UCC2919, an industrial-grade version of the UCC3919.

2 Turnon

Figure 1 is a simplified circuit model of the UCC3919 that shows only the LCA, charge pump, and charge-pump comparator. The turnon voltages are shown in Figure 2.

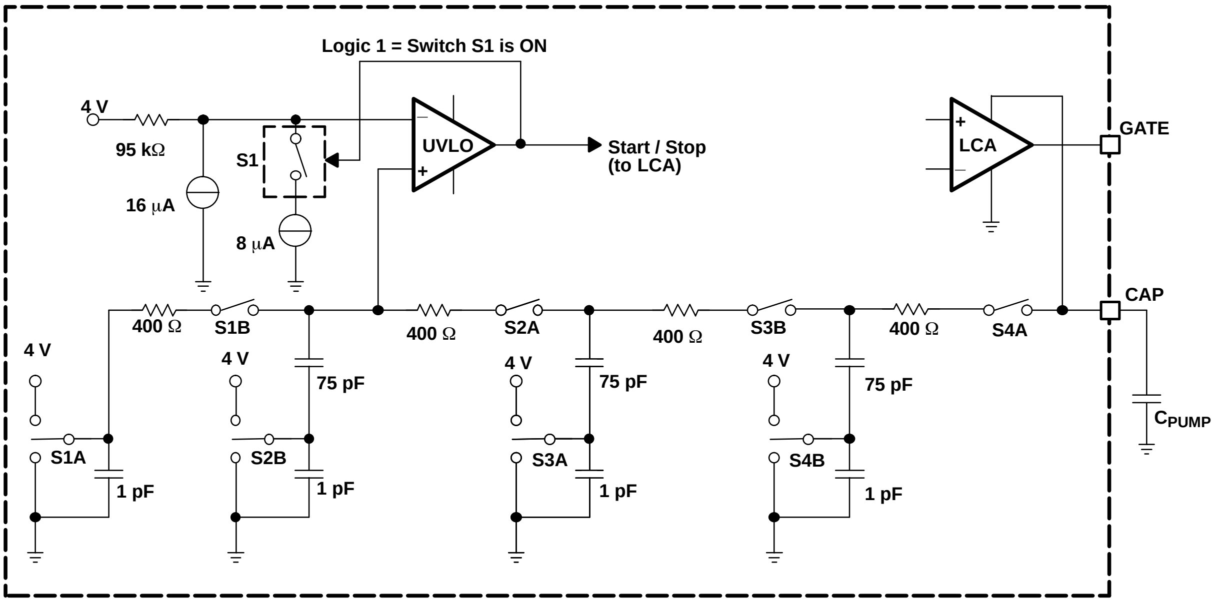

Figure 1. A Simplified UCC3919 Circuit Model

The UCC3919 charges capacitor C_{PUMP} when the $\overline{SD}$ input de-asserts. The UVLO comparator enables the LCA when the capacitor voltage rises to V_{START}, the charge-pump UVLO minimum voltage to start. For the UCC3919 example in Figure 2, V_{START} is approximately 9 V. Figure 2 shows the UCC3919 turning on with different C_{PUMP} capacitors. Note that the hot-swap FET turnon delay is proportional to C_{PUMP}.

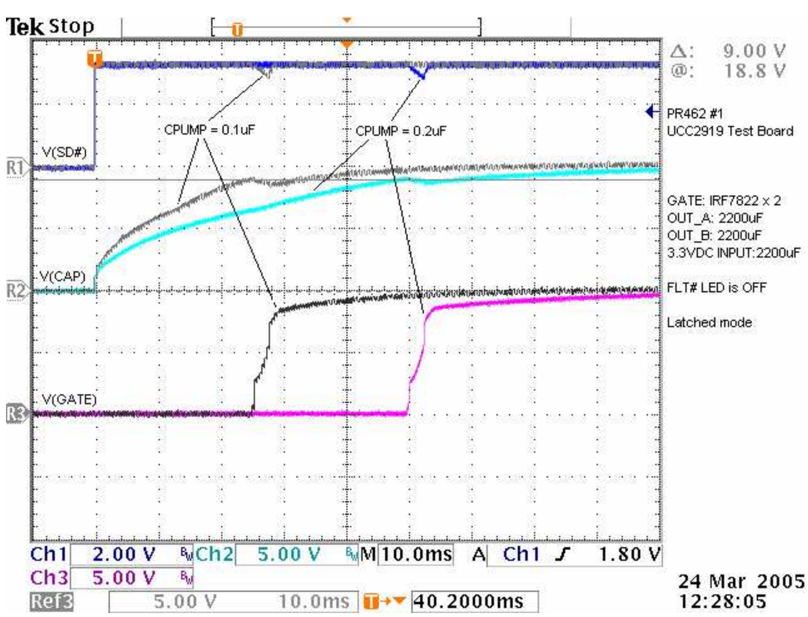

Figure 2. Typical UCC3919 Voltages at Turnon

3 SIZING C_{PUMP} FOR A PARTICULAR APPLICATION

Figure 3 shows a gate-drive circuit model that can be used to calculate the charge-pump capacitance.

The R_O represents the equivalent LCA output resistance, V_{CAP} represents the charge-pump output voltage, and C_g models the FET gate capacitance. The charge-pump voltage V_{CAP} rises to V_{START} just before switch SW1 closes. The closing of switch SW1 models the LCA turning on. The voltage source V_{OUT} represents the load voltage when the hot-swap FET is on.

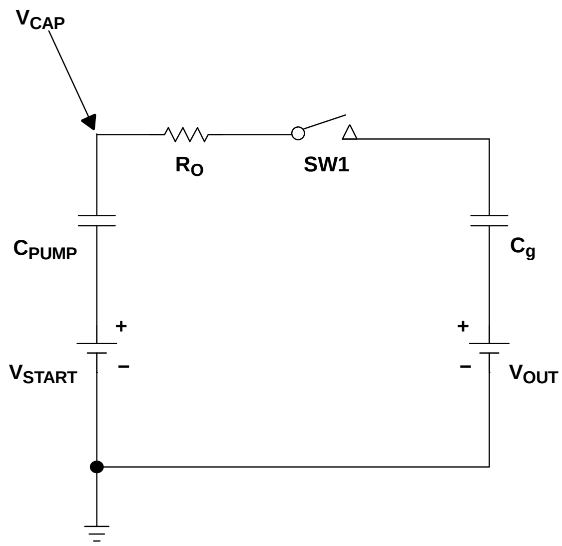

Figure 3. UCC3919 Gate-Drive Circuit Model.

When switch SW1 closes, charge from capacitor C_{PUMP} transfers to capacitor C_g causing the charge-pump voltage to drop by ΔV_{CAP}. Equation 1 describes this relationship.

$$C_{PUMP} \times \frac{\mu Q_{PUMP}}{\mu V_{CAP}} \qquad (1)$$

The charge lost by capacitor C_{PUMP} is gained by capacitor C_g.

$$\mu Q_{PUMP} \quad \mu Q_G \Big| \; V_{GS} \quad \geq V_{START} \times V_{OUT} \times V_{HYST}\Big) \qquad (2)$$

To ensure proper turnon, the charge-pump voltage droop must be less than the UVLO comparator hysteresis.

$$\mu V_{CAP} \times V_{HYST} \qquad (3)$$

Combine equations (1), (2), and (3) to get Equation 4.

$$C_{PUMP} \geq \frac{\mu Q_G}{V_{HYST}} \Big| \; V_{GS} \quad \Big) V_{START} \times V_{OUT} \times V_{HYST} \qquad (4)$$

For a worst-case calculation, use the maximum value for V_{START} and the minimum value for V_{HYST} in Equation 5.

UCC3919 production data over temperature and the V_{DD} supply voltage show that:

V_{START} (max) = 11 V
V_{HYST} (min) = 0.7 V

Therefore:

$$C_{PUMP} \geq \frac{\mu Q_G}{0.7\ V} \Bigg|\ V_{GS} \quad) 10.3\ V \times V_{OUT} \qquad (5)$$

As an example, consider a 3.3-V output hot-swap design that drives three IRF7822 FETs. The curve in Figure 4 shows 58.75 nC of gate charge for a gate-to-source voltage of 7 V. Thus, the required charge-pump capacitance is

$$C_{PUMP} \geq \frac{58.75\ nC \times 3}{0.7\ V} \quad 0.252\ \mu F \qquad (6)$$

A standard 0.33-µF ± 10% X7R dielectric capacitor works for this design. Note that 10% is the capacitor's initial tolerance. This tolerance is measured at room temperature and zero-bias voltage. The actual tolerance is higher when the capacitor's operating temperature and operating voltage are considered.

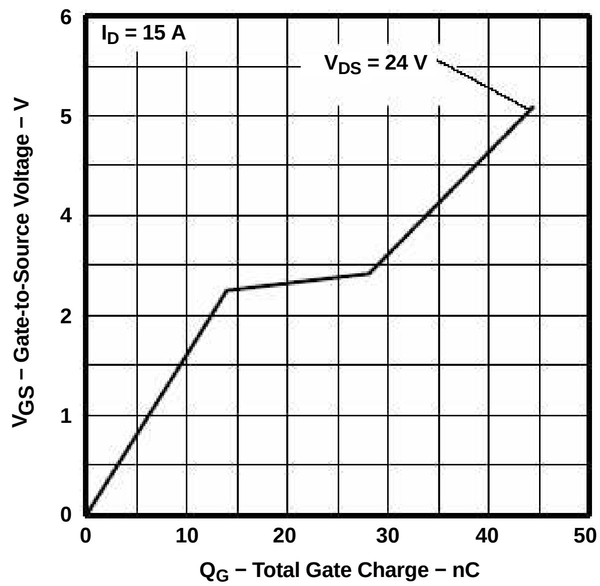

Figure 4. IRF7822 Gate Charge vs Gate-to-Source Voltage (1)

(1) Reprinted with permission from International Rectifier; Fig 2, page 3, International Rectifier IRF7822 datasheet.

4 SUMMARY

The UCC3919 works in a low-to-moderate current, hot-swap design with a 0.01-µF to 0.1-µF capacitance at the CAP pin as recommended in the data sheet (SLUS374). A high-current, hot-swap design that uses a larger FET requires more capacitance. This capacitance can be determined using the simple approach presented in this application report. The larger capacitance increases the hot-swap FET turnon delay but has no other effect on the UCC3919.

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