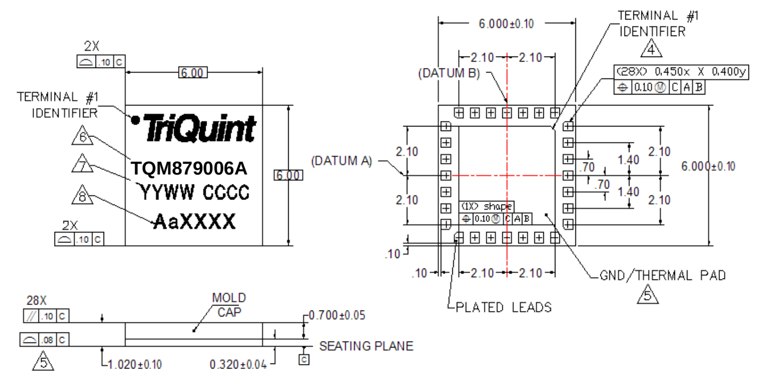
# Mechanical Information

## Package Information and Dimensions

This package is RoHS-compliant. The package bottom finish is electrolytic plated Au over Ni. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes. Also recommend adding active fluxes of 2% during solder reflow.

The component will be laser marked with “TQM879006A” product label with an alphanumeric lot code on the top surface of the package.



NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO–220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINEPITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M–1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

4 THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95–1 SPP–012.

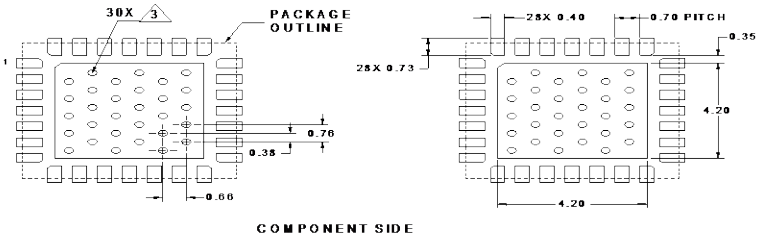
5 COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.

6 PRODUCT CODE.

7 ALPHA–NUMERIC LOT CODE.

8 VENDOR CODE AND TRIQUINT LOT NUMBER

## PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.