NM7010A-LF

1. Introduction

NM7010A-LF is the network module that includes W3100A-LF (TCP/IP hardwired chip), Ethernet PHY (RTL8201BL), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W3100A-LF and PHY chip. The NM7010A-LF is an ideal option for users who want to develop their Internet enabling systems rapidly.

NM7010A-LF consists of W3100A-LF, Ethernet PHY and MAG-JACK.

TCP/IP, MAC protocol layer: W3100A-LF

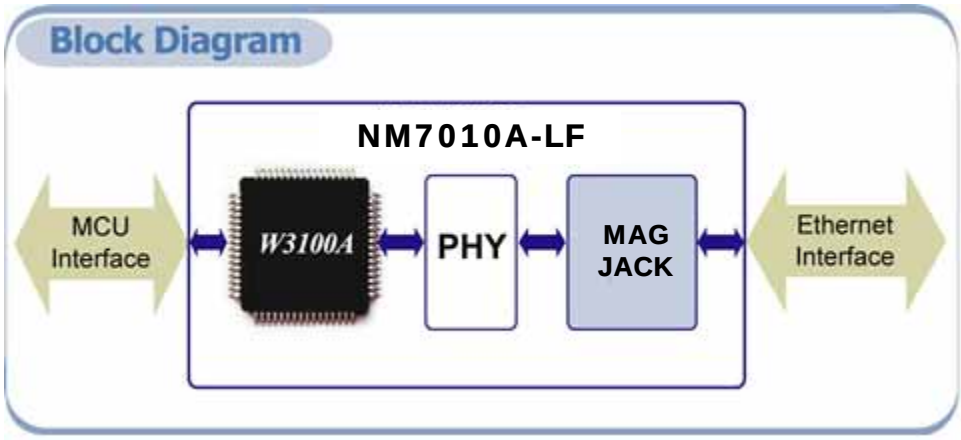
Physical layer: Ethernet PHY

Connector: MAG-JACK

1.1. Features

- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports auto-negotiation
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports Intel/Motorola MCU bus Interface
- Supports I^2C Interface
- Supports Direct/Indirect mode bus access
- Supports clocked mode, non-clocked mode, external clocked mode
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 14 header pin

1.2. Block Diagram



2. Pin Assignments & descriptions

I : Input O : Output

I/O : Bi-directional Input and output P : Power

2.1. Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP1 : 1 , JP2 : 24	**Power** : 3.3 V power supply
GND	P	JP1 : 8, JP1 : 13, JP1 : 24, JP2 : 1, JP2 :4, JP2 : 7, JP2 : 13, JP2 : 14, JP2 : 23	**Ground**

2.2. MCU Interfaces

Symbol	Type	Pin No.	Description
A14~A8	I	JP1 : 7, JP1 : 10 JP1 : 9, JP1 : 12 JP1 : 11, JP1 : 14 JP1 : 15	**Address / Device Address :**In Bus access mode is used as Address[14-8] pin In I^2C interface mode is used as device address[6-0] pin
A7~A0	I	JP1 : 16 ~ JP1 : 23	**Address :** In Bus access mode is used as Address[7-0] pin In I^2C interface mode, these pins are not used, so leave them NC or ground them.
D7~D0	I/O	JP2 : 21, JP2 : 22 JP2 : 19, JP2 : 20 JP2 : 17, JP2 : 18 JP2 : 15, JP2 : 16	**Data** : 8 bit-wide data bus
/CS	I	JP1 : 5	**Module Select** : Active low. /CS of W3100A
/RD	I	JP1 : 4	**Read Enable** : Active low. /RD of W3100A
/WR	I	JP1 : 3	**Write Enable** : Active low /WR of W3100A
/INT	O	JP1 : 2	**Interrupt** : Active low After reception or transmission it indicates that the W3100A requires MCU attention. By writing values to the Interrupt Status Register of W3100A the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W3100A(Interrupt Mask Register). For more details refer to the W3100A Datasheet
I_SCL	I	JP2 : 25	**SCL** :

			Used as clock by I^2C interface mode. Internally pull-down
I_SDA	I/O	JP2 : 26	**SDA** : Used as data by I^2C interface mode. Internally pull-down

2.3. Network status & LEDs

You can observe the network status using MAC-JACK LEDs. LED interface can be extended to the LED of the main board.

Symbol	Type	Pin No.	Description
L_COL	O	JP2 : 6	**Collision LED** : Active low when collisions occur.
L_100ACT	O	JP2 : 8	**Link 100/ACT LED** : Active low when linked by 100 Base TX, and blinking when transmitting or receiving data.
L_10ACT	O	JP2 : 10	**Link 10/ACT LED** : Active low when linked by 10 Base T, and blinking when transmitting or receiving data.
L_DUPX	O	JP2 : 11	**Full Duplex LED** : Active low when in full duplex operation. Active high when in half duplex operation.
L_LINK	O	JP2 : 12	**Link LED** : Active low when linked

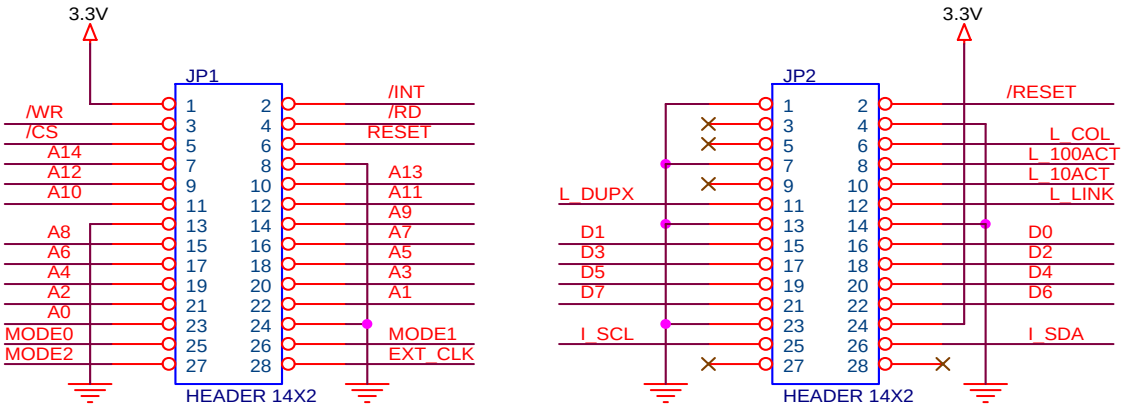
2.4. Miscellaneous Signals

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>RESET</td><td>I</td><td>JP1 : 6</td><td>Reset : Active high
Initializes or Reinitializes the W3100A. Asserting this pin will force a reset process to occur, which will result in all internal registers reinitializing to their default and all strapping options are reinitialized.
For complete reset function, this pin must be asserted low for at least 10us. Refer to W3100A datasheet for further detail regarding reset.</td></tr>
<tr><td>/RESET</td><td>I</td><td>JP2 : 2</td><td>Reset : Active low
Reset RTL8201BL chip. For complete reset function this pin must be asserted low for at least 10ms.</td></tr>
<tr><td>MODE1~0</td><td>I</td><td>JP1 : 26 ,
JP1 : 25</td><td>Mode Select : These pins select MCU interface and operating mode. Since each pin is pull-down internally, clocked mode (the default mode) is selected when these pins are not connected.
<table>
<tr><th>M1 M0</th><th>Mode</th></tr>
<tr><td>0 0</td><td>Clocked</td></tr>
<tr><td>0 1</td><td>External clocked</td></tr>
<tr><td>1 0</td><td>Non-clocked</td></tr>
<tr><td>1 1</td><td>I^{2}C interface</td></tr>
</table>
Refer to W3100A datasheet for further detail regarding mode select</td></tr>
</table>

EXT_CLK	I	JP1 : 28	**External clock** : supplementary clock used for external clocked mode. In external clocked mode, W3100A uses this clock to interface with MCU. Refer to W3100A datasheet for further detail regarding external clock.
NC	-	JP1 : 27, JP2 : 3 JP2 : 5, JP2 : 9 JP2 : 27, JP2 : 28	Not Connect

2.5. Pin Location & Schematic

Refer to “Chapter 4. Dimension”.



3. Timing Diagrams

NM7010A provides following interfaces of W3100A

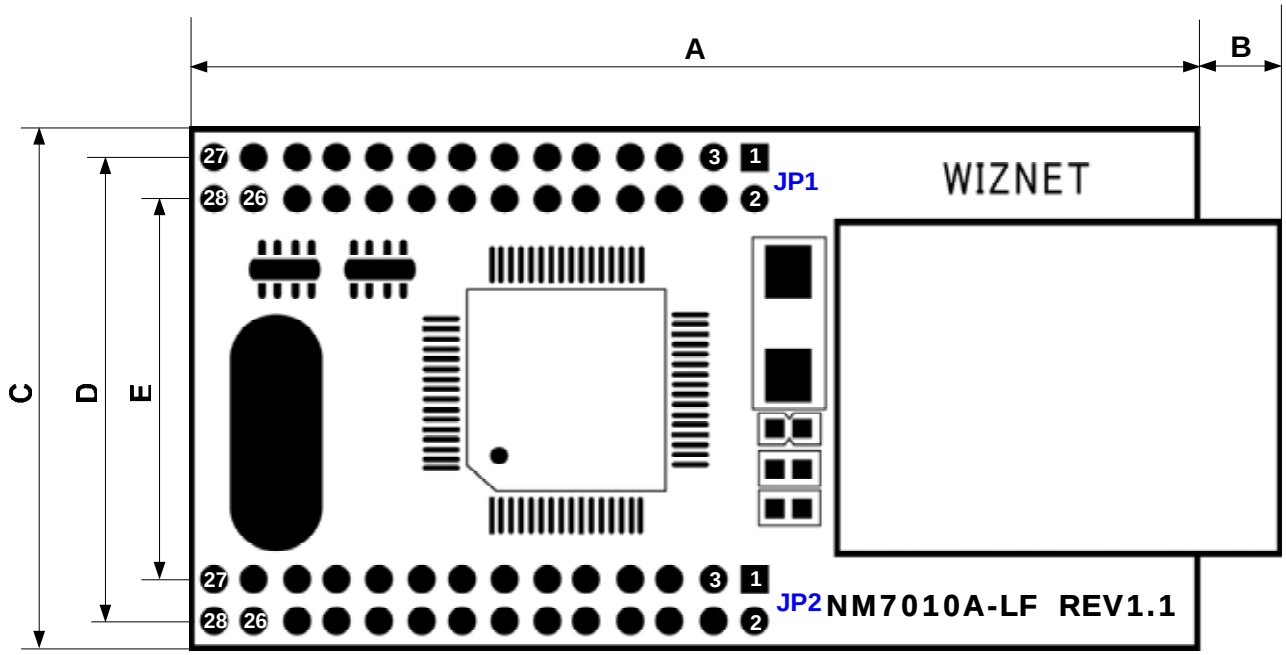
-. Direct/Indirect mode bus access

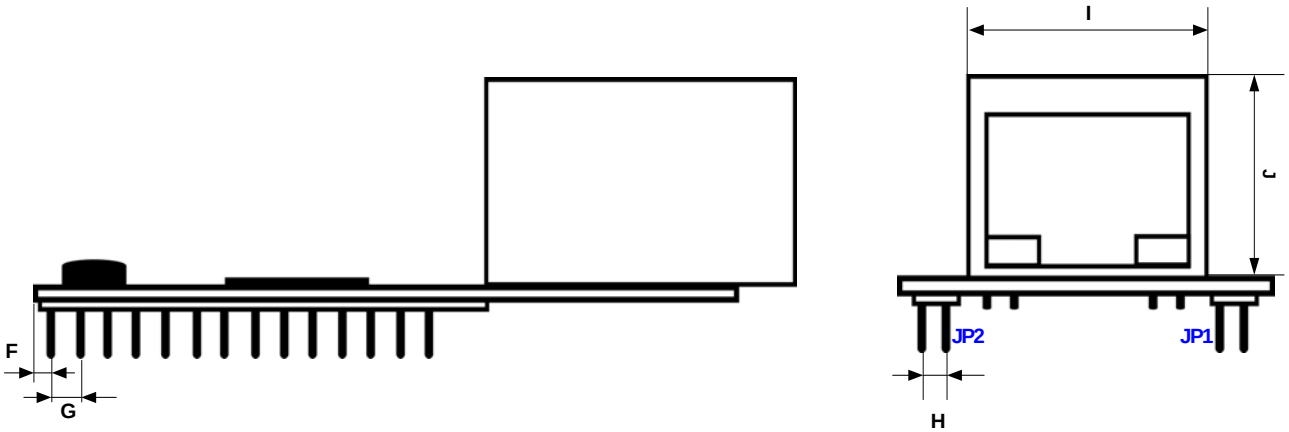
-. I^2C Interface

-. Clocked mode, Non-Clocked mode, External clocked mode

Refer to W3100A datasheet for timing of NM7010A

4. Dimensions





Symbols	Dimensions (mm)
A	48.0
B	4.0
C	25.0
D	22.4
E	18.4
F	1.0
G	2.0
H	2.0
I	16.0
J	13.4

5. Connector Specification

UNIT:mm