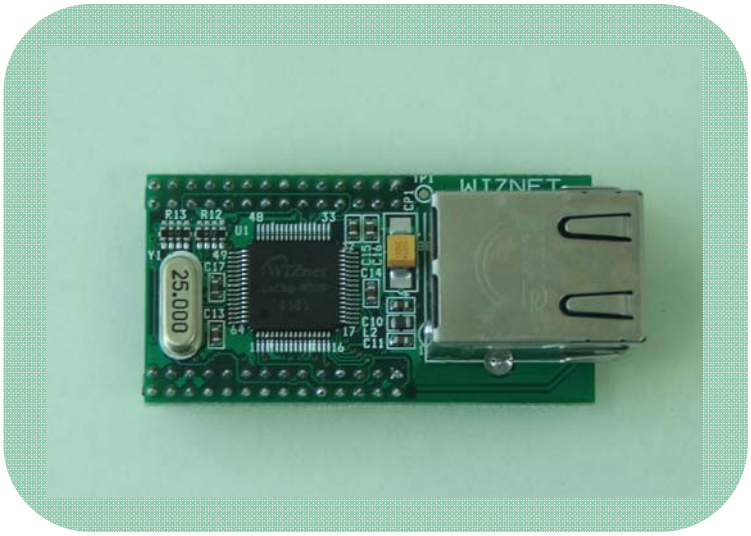
NM7010B+ Datasheet
(Ver. 1.1)



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Document History Information

Revision	Data	Description
Ver. 1.0	OCTOBER , 2006	Release with NM7010B+ Launching
Ver. 1.1	June 29, 2007	Add SPI signal Pin description(A14-A11)

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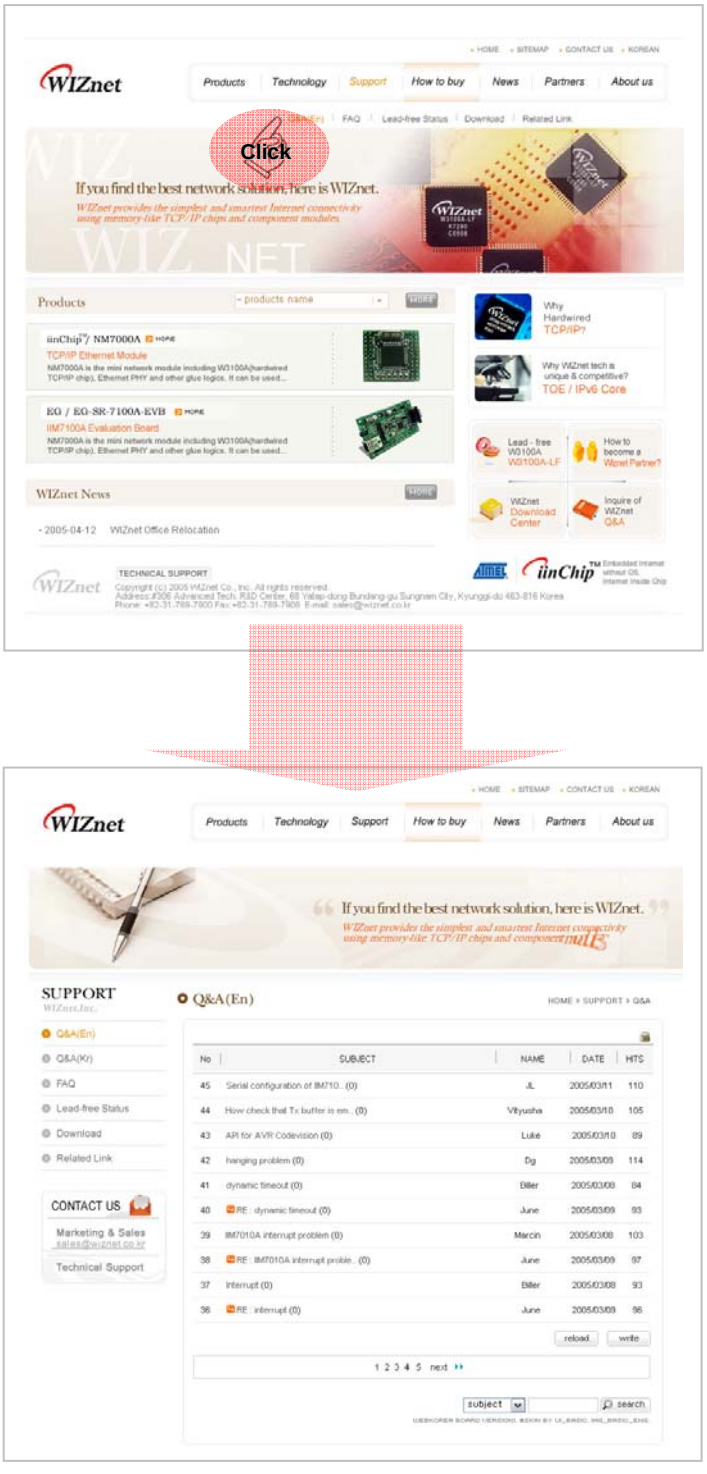


NM7010B+ Datasheet

<CONTENTS>

1. Introduction

NM7010B+ is the network module that includes W3150A+ (TCP/IP hardwired chip), Ethernet PHY (RTL8201CP), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W3150A+ and PHY chip. The NM7010B+ is an ideal option for users who want to develop their Internet enabling systems rapidly.

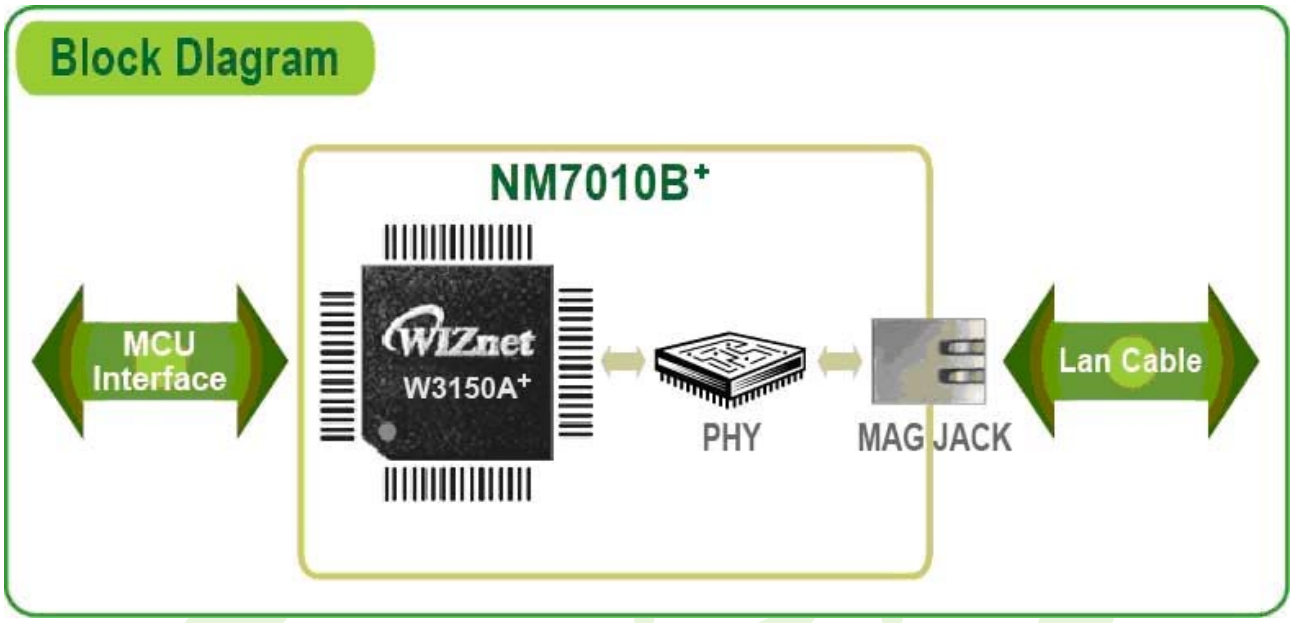
NM7010B+ consists of W3150A+, Ethernet PHY and MAG-JACK.

- TCP/IP, MAC protocol layer: W3150A+
- Physical layer: Ethernet PHY
- Connector: MAG-JACK

1.1. Features

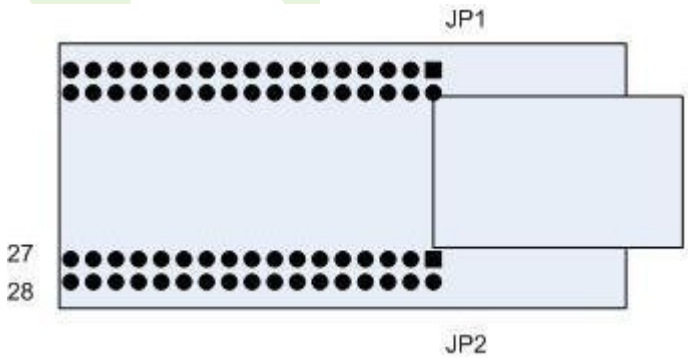
- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports auto-negotiation and auto crossover detection
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports MCU bus Interface and SPI Interface
- Supports Direct/Indirect mode bus access
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 14 header pin

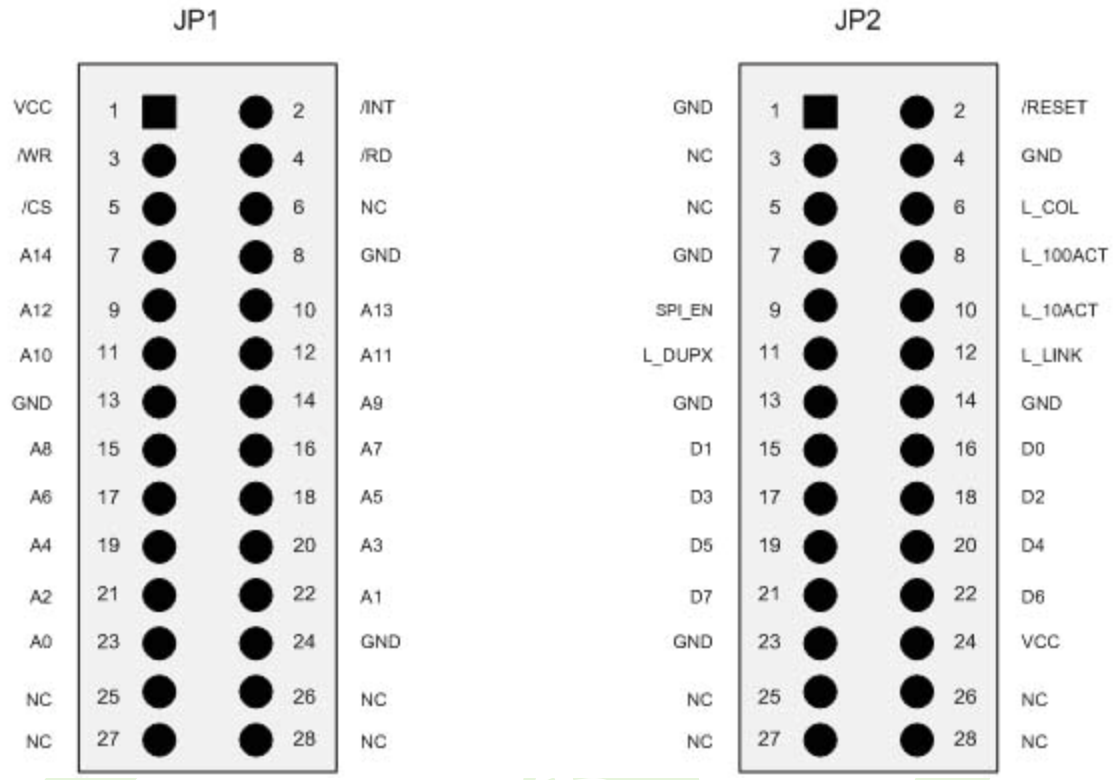
1.2. Block Diagram



2. Pin Assignments & descriptions

2.1. Pin Assignments





I : Input O : Output

I/O : Bi-directional Input and output P : Power

2.2. Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP1 : 1 , JP2 : 24	**Power** : 3.3 V power supply
GND	P	JP1 : 8, JP1 : 13, JP1 : 24, JP2 : 1 JP2 : 4, JP2 : 7 JP2 : 13, JP2 : 14 JP2 : 23	**Ground**

2.3. MCU Interfaces

Symbol	Type	Pin No.	Description
A14	I	JP1 : 7	**ADDRESS PIN OR SCLK(Serial Clock)** This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Clock signal Pin.
A13	I	JP1 : 10	**ADDRESS PIN or /SS (Slave Select)** * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Slave Select signal Pin. In only SPI Mode, this pin is active low
A12	I	JP1 : 9	**ADDRESS PIN or MOSI (Master Out Slave In)** * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MOSI signal pin.
A11	I/O	JP1 : 12	**ADDRESS PIN or MISO (Master In Slave Out)** * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MISO signal pin.
A10~A8	I	JP1 : 11, JP1 : 14 JP1 : 15	**Address** Used as Address[10-8] pin
A7~A0	I	JP1 : 16 ~ JP1 : 23	**Address** Used as Address[7-0] pin
D7~D0	I/O	JP2 : 21, JP2 : 22 JP2 : 19, JP2 : 20 JP2 : 17, JP2 : 18 JP2 : 15, JP2 : 16	**Data** 8 bit-wide data bus
/CS	I	JP1 : 5	**Module Select** : Active low. /CS of W3150A+
/RD	I	JP1 : 4	**Read Enable** : Active low. /RD of W3150A+
/WR	I	JP1 : 3	**Write Enable** : Active low /WR of W3150A+

/INT	O	JP1 : 2	**Interrupt** : Active low After reception or transmission it indicates that the W3150A+ requires MCU attention. By writing values to the Interrupt Status Register of W3150A+ the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W3150A+ (Interrupt Mask Register). For more details refer to the W3150A+ Datasheet

2.4. Network status & LEDs

You can observe the network status using MAC-JACK LEDs. LED interface can be extended to the LED of the main board.

Symbol	Type	Pin No.	Description
L_COL	O	JP2 : 6	**Collision LED** : Active low when collisions occur.
L_100ACT	O	JP2 : 8	**Link 100/ACT LED** : Active low when linked by 100 Base TX, and blinking when transmitting or receiving data.
L_10ACT	O	JP2 : 10	**Link 10/ACT LED** : Active low when linked by 10 Base T, and blinking when transmitting or receiving data.
L_DUPX	O	JP2 : 11	**Full Duplex LED** : Active low when in full duplex operation. Active high when in half duplex operation.
L_LINK	O	JP2 : 12	**Link LED** : Active low when linked

2.5. Miscellaneous Signals

Symbol	Type	Pin No.	Description
/RESET	I	JP2 : 2	**Reset :** Active low Reset W3150A, RTL8201BL chip. For complete reset function this pin must be asserted low for at least 10ms.
SPI_EN	I	JP2 : 9	**SPI Enable** This pin selects Enable/disable W3150A+ SPI Mode This pin is internally pulled low for previous W3150A users. Even if there is no signal connection to this pin, it asserts low internally. So change to new version W3150A+ including SPI interface, there is no effort to change previous board design. Low = Disable W3150A+ SPI Mode High = Enable W3150A+ SPI Mode
NC	-	JP1 : 6, 25, 26, 27, 28 JP2 : 3, 5, 9, 25, 26, 27, 28	Not Connect

3. Timing Diagrams

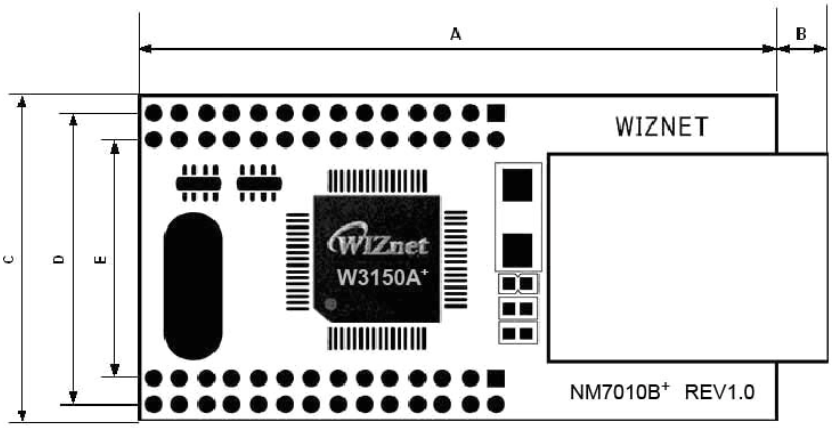
NM7010B+ provides following interfaces of W3150A+

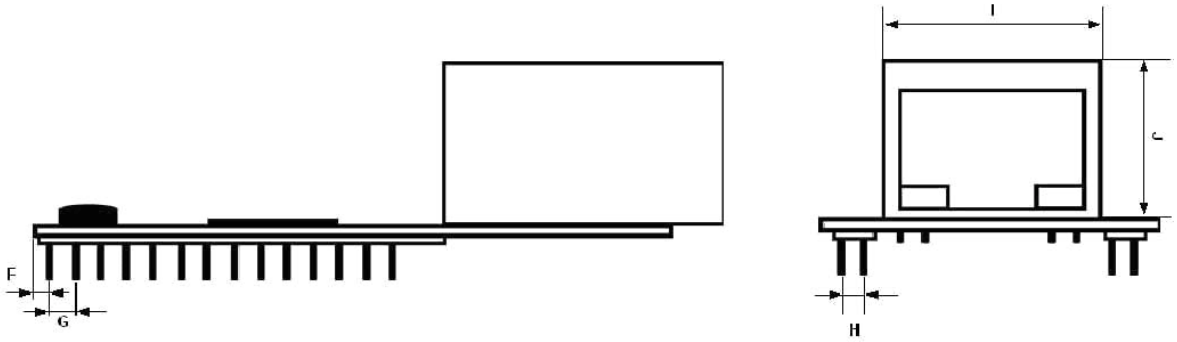
-. Direct/Indirect mode bus access

-. SPI access

Refer to W3150A+ datasheet for timing of NM7010B+

4. Dimensions





Symbols	Dimensions (mm)
A	48.0
B	4.0
C	25.0
D	22.4
E	18.4
F	1.0
G	2.0
H	2.0
I	16.0
J	13.4

5. Connector Specification

UNIT:mm