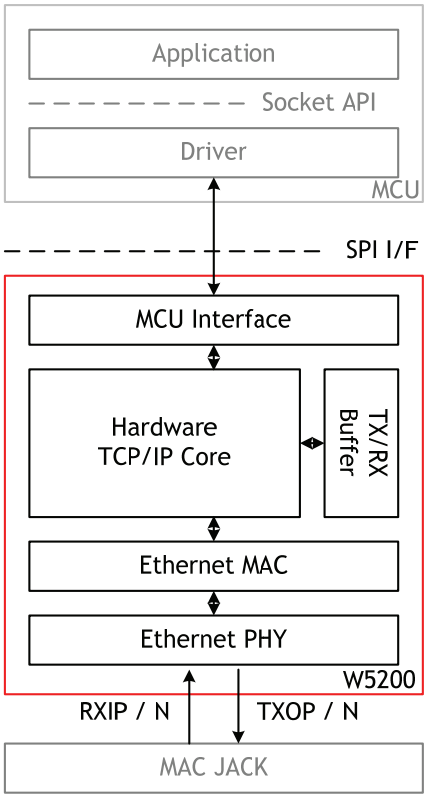
The W5200 chip is a Hardwired TCP/IP embedded Ethernet controller that enables easier internet connection for embedded systems using SPI Interface. By using SPI Interface, the decreased footprint size enables easier implementation for smaller embedded systems. The Hardware TCP/IP stack that is being used in W5200 has been certified throughout years in many applicable fields and provides network protocols such as, TCP, UDP, IPv4, ICMP, ARP, IGMP, PPPoE, and etc. The W5200 chip has both Ethernet MAC and PHY embedded inside; providing all necessary solutions for internet connection. Also, for energy related applicable fields, W5200 provides Power Down mode; minimizing energy consumption.

48 Pin QFN Package (7mm x 7mm)

Features

- Support Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4 ARP, IGMP, PPPoE, Ethernet
- Support high speed serial peripheral Interface(SPI MODE 0, 3)
- Supports 8 independent sockets simultaneously
- Support Power down mode
- Support Wake on LAN
- 10BaseT/100BaseTX Ethernet PHY embedded
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Support Auto MDI/MDIX
- Support ADSL connection (with support PPPoE Protocol with PAP/CHAP Authentication mode)
- Internal 32Kbytes Memory for Tx/Rx Buffers
- 3.3V operation with 5V I/O signal tolerance
- Lead-Free Package
- Multi-function LED outputs (Full/Half duplex, Link, Speed)



W5200 Block Diagram

http://www.wiznet.co.kr