

# Reset WizFi210

(WizFi 210 Application Notes)



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## 1. Reset WizFi210

EXT\_RESET pin is bidirectional.

EXT\_RESET pin is an output right at power-on, and kept it asserted while the 32KHz crystal is stabilizing. Once crystal is stabilized, RESET is de-assert and it becomes an input. Also at power up, WizFi210 don't require a reset, as it have a power-on-reset already built in. So MCU need not assert unless there is a real issue (E.g. hang).

Note: Minimum pulse width for reset is two 32KHz clock.



EXT\_RESET signal is active low signal (active or asserted state occurs when the signal is at a low voltage level).

It's an output during power up, indicating to the system when WizFi210 device is out of power-on-reset. After power-on-reset, this pin is an input. It's not necessary to assert reset to the WizFi210 after power on, since the WizFi210 has a built-in power on reset.

And, EXT\_RESET signal does not clear the RTC RAM or the SRAM.

But, be sure that <Led Blink during boot> is not progressed, if WizFi210 is reset by EXT\_RESET.