Spartan-6 FPGA LX16 CES Errata

EN113 (v1.5) March 18, 2011 **Errata Notification**

Introduction

Thank you for participating in the Spartan®-6 FPGA Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the device listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, this device is subject to the limitations described in the following errata.

Device

These errata apply to the Spartan-6 device shown in Table 1.

Table 1: **Device Affected by These Errata**

Device	JTAG ID (Revision Code)
XC6SLX16-2CSG324CES	1

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

IODELAY2

In the devices listed in Table 1, the IODELAY2 block can experience late data edge delays, early data edge delays, and single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

Late Data Edge Delay in IDELAY and ODELAY Modes

The IODELAY2 block can add up to 350 ps of delay on the rising or falling edge transitions when the IDELAY_VALUE or ODELAY_VALUE is 4 or higher for all IDELAY_TYPE settings or when used as output delay. This behavior can be present at all data rates and should be included in system timing margin analysis.

Early Data Edge Delay in ODELAY Mode

The IODELAY2 block used in the ODELAY mode can generate a data edge up to 350 ps early on the rising or falling edge transitions. This behavior can be present at data rates higher than 533 Mb/s and for all ODELAY_VALUE settings and should be included in system timing margin analysis.

Single Data Bit Corruption in IDELAY and ODELAY Modes

The IODELAY2 block can corrupt a single data bit for all IDELAY_TYPE settings or when used in ODELAY mode.

Work-arounds

IDELAY_TYPE=DEFAULT

The data rate must not exceed 250 Mb/s to avoid data corruption.

IDELAY_TYPE=FIXED or VARIABLE_FROM_ZERO or When Used in ODELAY Mode

The IDELAY_VALUE or ODELAY_VALUE must not exceed the values in Table 2 to avoid data corruption at the indicated data rate.

Table 2: **Maximum IDELAY_VALUE or ODELAY_VALUE**

Data Rate (Mb/s)	Bit Time (ps)	Maximum DELAY Value
945	1,058	9
800	1,250	14
667	1,499	20
625	1,600	22
533	1,876	28
400	2,500	43
333	3,003	54
266	3,759	72
200	5,000	101
188	5,319	107

IDELAY_TYPE=VARIABLE_FROM_HALF_MAX

The data rate must not exceed 400 Mb/s, the IODELAY2 IOCLK frequency must be equal to the data rate, and the positive increment must not exceed 5 to avoid data corruption.

IDELAY_TYPE=DIFF_PHASE_DETECTOR

The data rate must not exceed 400 Mb/s and data to clock skew, including package trace difference, must not exceed 0.15 UI to avoid data corruption.

See Answer Record 38408 for additional information.

Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) READ_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

Work-around

The recommended work-around to avoid memory array corruption issue is to configure the block RAM in WRITE_FIRST mode. WRITE_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.3 and later.

See Answer Record 34533.

9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWER in Simple Dual Port (SDP) mode (RAM_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA_WIDTH_A=36, DATA_WIDTH_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

Work-around

See Answer Record 34541.

9K Block RAM Initialization

Block RAM used in the 9K mode (RAMB8BWER) can fail to initialize user data or default values during configuration in the devices listed in Table 1.

This issue will not be fixed in the devices listed in Table 1.

Work-arounds

Either use 18K block RAM or write to the 9K block RAM to initialize it after configuration.

See Answer Record 39999.

Block RAM Byte-Write Enable Hold Time

The block RAM byte-write enable input can have a positive hold time in the device listed in Table 1.

Work-around

Adding additional delay to the write enable input on the block RAM is recommended. Do not place the write-enable source in the CLB adjacent to the block RAM.

Memory Controller Block (MCB)

MCB Calibration

In the device listed in Table 1, for designs using Calibrated Input Termination, use the following CSG324 pin locations for the RZQ reference resistor: MCB Bank 1 – pin M13, MCB Bank 3 – pin C2.

MCB and Suspend

In the device listed in Table 1, the MCB does not support the self-refresh mode of the external memory during FPGA Suspend.

MCB Address Bus Hold Time

In the device listed in Table 1, some bits of the MCB address bus (mcbx_dram_addr) can violate the input hold time (t_{IH}) specification of the memory device.

Work-around

See Answer Record 34089.

DCM Minimum Frequency

The Digital Clock Manager (DCM_SP or DCM_CLKGEN) minimum frequency does not meet the data sheet specifications in the device listed in Table 1. The following specifications deviate from the data sheet:

- CLKIN_FREQ_DLL Min: 50 MHz
- CLKOUT_FREQ_CLK0 Min: 50 MHz
- CLKOUT_FREQ_CLK90 Min: 50 MHz
- CLKOUT_FREQ_2X Min: 100 MHz
- CLKOUT_FREQ_DV Min: 3.125 MHz
- CLKIN_FREQ_FX Min: 1.6 MHz
- CLKOUT_FREQ_FX Min: 50 MHz
- CLKOUT_FREQ_FXDV: 1.6 MHz

BUFPLL LOCK Output

In the device listed in Table 1, the BUFPLL LOCK output might stay High when the PLL_BASE LOCKED signal is Low. As a result, the timing of the SERDESSTROBE signal might change after the PLL has been reset.

Work-around

Any application that performs a training, framing, or Bitslip function on the incoming data should be reinitialized following a PLL reset to ensure correct data reception.

Device DNA

Device DNA is not supported in the device listed in Table 1. Do not use this feature.

IOB DDR Mode

DDR mode is not supported in Banks 0 and 2 (top and bottom) in the device listed in Table 1.

Configuration Readback

Readback is not supported in the device listed in Table 1. Do not select the verify or readback options in the iMPACT tool or enable post-configuration CRC.

See Answer Record 35055 for more information.

Operational Guidelines

Design Software Requirements

The device listed in Table 1, unless otherwise specified, requires the following Xilinx development software installation.

Speed specification v1.01, Xilinx® ISE Design Suite 11.3, but no later than speed specification v1.12 and Xilinx ISE Design Suite 12.3 (see Answer Record 39545).

Operating Conditions Required when Using I/O Delay Variable Mode

In the device listed in Table 1, when using I/O Delay Variable Mode, the operating conditions must be:

- V_{CCINT} = 1.20V to 1.26V
- Junction temperature (T_j) = 25°C to 85°C

The I/O delay variable mode (also known as I/O delay calibration and reset) is used when the IODELAY2 CAL or RST are used or when IODELAY2 IDELAY_TYPE attribute is set to VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, or DIFF_PHASE_DETECTOR.

Traceability

The XC6SLX16 listed in Table 1 is marked as shown in Figure 1.

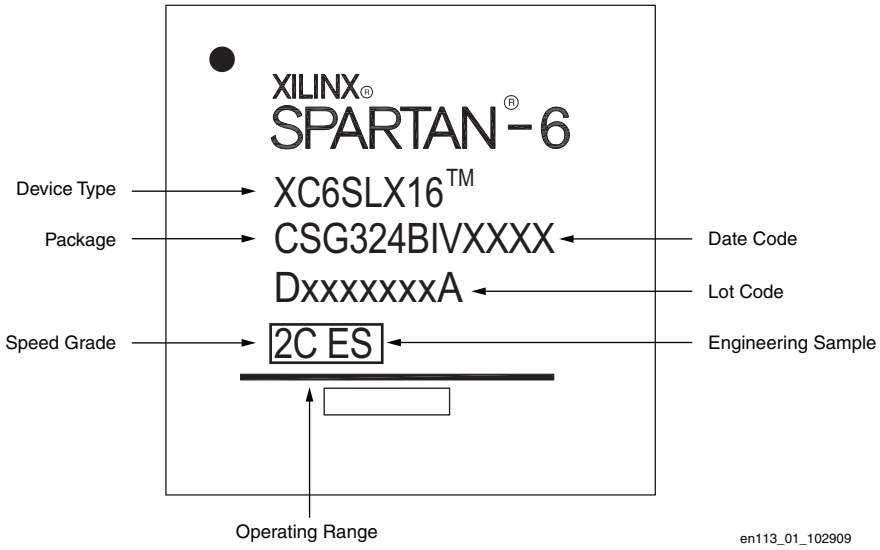

Figure 1: **XC6SLX16-2CSG324CES Marking**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
07/17/09	1.0	Initial Xilinx release.
09/10/09	1.1	Updated the Memory Controller Block (MCB) section and removed reference to software issues in Answer Record 33130. Removed MCB Auto-Precharge Instructions; this issue will be addressed in software.
10/29/09	1.2	Added MCB and Suspend. Updated Figure 1 marking.
02/11/10	1.3	Added MCB Address Bus Hold Time. Updated Design Software Requirements.
05/07/10	1.4	Created a Block RAM section: Added Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode and 9K Simple Dual Port Block RAM Width Restriction.
03/18/11	1.5	Added IODELAY2 and 9K Block RAM Initialization. Updated Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode and Design Software Requirements.

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