

## Introduction

Thank you for participating in the Spartan®-6 FPGA Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

## Devices

These errata apply to the Spartan-6 devices shown in [Table 1](#).

*Table 1: Devices Affected by These Errata*

Devices	JTAG ID (Revision Code)
XC6SLX45T-2FGG484CES	1
XC6SLX45T-3FGG484CES	1

## Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

### IODELAY2

In the devices listed in [Table 1](#), the IODELAY2 block can experience late data edge delays, early data edge delays, and single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

#### ***Late Data Edge Delay in IDELAY and ODELAY Modes***

The IODELAY2 block can add up to 350 ps of delay on the rising or falling edge transitions when the IDELAY\_VALUE or ODELAY\_VALUE is 4 or higher for all IDELAY\_TYPE settings or when used as output delay. This behavior can be present at all data rates and should be included in system timing margin analysis.

#### ***Early Data Edge Delay in ODELAY Mode***

The IODELAY2 block used in the ODELAY mode can generate a data edge up to 350 ps early on the rising or falling edge transitions. This behavior can be present at data rates higher than 533 Mb/s and for all ODELAY\_VALUE settings and should be included in system timing margin analysis.

#### ***Single Data Bit Corruption in IDELAY and ODELAY Modes***

The IODELAY2 block can corrupt a single data bit for all IDELAY\_TYPE settings or when used in ODELAY mode.

#### **Work-arounds**

##### **IDELAY\_TYPE=DEFAULT**

The data rate must not exceed 250 Mb/s to avoid data corruption.

##### **IDELAY\_TYPE=FIXED or VARIABLE\_FROM\_ZERO or When Used in ODELAY Mode**

The IDELAY\_VALUE or ODELAY\_VALUE must not exceed the values in [Table 2](#) to avoid data corruption at the indicated data rate.

Table 2: Maximum IDELAY\_VALUE or ODELAY\_VALUE

Data Rate (Mb/s)	Bit Time (ps)	Maximum DELAY Value
1,050	952	7
1,000	1,000	8
945	1,058	9
800	1,250	14
667	1,499	20
625	1,600	22
533	1,876	28
400	2,500	43
333	3,003	54
266	3,759	72
200	5,000	101
188	5,319	107

**IDELAY\_TYPE=VARIABLE\_FROM\_HALF\_MAX**

The data rate must not exceed 400 Mb/s, the IODELAY2 IOCLK frequency must be equal to the data rate, and the positive increment must not exceed 5 to avoid data corruption.

**IDELAY\_TYPE=DIFF\_PHASE\_DETECTOR**

The data rate must not exceed 400 Mb/s and data to clock skew, including package trace difference, must not exceed 0.15 UI to avoid data corruption.

See [Answer Record 38408](#) for additional information.

## Block RAM

### **Dual Port Block RAM Address Overlap in READ\_FIRST and Simple Dual Port Mode**

When using the block RAM in True Dual Port (TDP) READ\_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of [UG383](#), *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

**Work-around**

The recommended work-around to avoid memory array corruption issue is to configure the block RAM in WRITE\_FIRST mode. WRITE\_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE\_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.3 and later.

See [Answer Record 34533](#).

## 9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWER in Simple Dual Port (SDP) mode (RAM\_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA\_WIDTH\_A=36, DATA\_WIDTH\_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of [UG383](#), *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

### Work-around

See [Answer Record 34541](#).

## 9K Block RAM Initialization

Block RAM used in the 9K mode (RAMB8BWER) can fail to initialize user data or default values during configuration in the devices listed in [Table 1](#).

This issue will not be fixed in the devices listed in [Table 1](#).

### Work-arounds

Either use 18K block RAM or write to the 9K block RAM to initialize it after configuration.

See [Answer Record 39999](#).

## Configuration

### Configuration Readback When Using 9K Block RAM

Configuration readback can corrupt 9K block RAM (RAMB8BWER) data. Configuration readback (including iMPACT Verify) is not supported when 9K block RAM is used in the devices listed in [Table 1](#).

This issue will not be fixed in the devices listed in [Table 1](#).

### Work-around

Use 18K block RAM if configuration readback will be used.

See [Answer Record 39977](#).

### Readback CRC

Readback CRC for SEU detection (POST\_CRC) is not supported in the devices listed in [Table 1](#).

## GTP Transceivers

### JTAG Configuration

If using the iMPACT, ChipScope™, or System ACE™ tools, see [Answer Record 33575](#).

JTAG configuration outside of the iMPACT or ChipScope tools is not supported when a GTP transceiver is used in the devices listed in [Table 1](#).

#### Work-around

Instantiate the STARTUP\_SPARTAN6 primitive. Connect a free-running clock from an FPGA pin to the CLK input port of the STARTUP\_SPARTAN6 primitive. The clock must have a frequency between 50 MHz to 100 MHz. Select the bitstream generator option StartUpClk:UserClk. This work-around must only be used when configuring the FPGA via JTAG. See the [Configuration Start-Up](#) section.

### Configuration Start-Up

The bitstream generator option StartUpClk:UserClk is not supported when a GTP transceiver is used in the devices listed in [Table 1](#), except for the work-around noted in the [JTAG Configuration](#) section.

#### Work-around

Select the default bitstream generator option StartUpClk:CCLK.

### CHAN\_BOND\_KEEP\_ALIGN Attribute

The CHAN\_BOND\_KEEP\_ALIGN attribute is not supported by the devices listed in [Table 1](#). The CHAN\_BOND\_KEEP\_ALIGN attribute must always be set to FALSE.

## Endpoint Block for PCI Express

### Small TLPs and Packet Not Accepted DLLPs

For the devices listed in [Table 1](#), if the endpoint block for PCIe® receives multiple Packet Not Accepted DLLPs (NAKs) while also having small TLPs in the queue, the transmitter can lock up.

### CFGERRCPLRDYN Signal Inversion

For the devices listed in [Table 1](#), the signal CFGERRCPLRDYN, which corresponds to cfg\_err\_cpl\_rdy\_n on the PCIe wrapper, is the wrong polarity. Designs that use this signal need to be modified for compatibility with non-ES devices.

#### Work-around

An inverter can be added in the wrapper to correct the polarity.

### LCRC Errors on Received Power Management Message TLPs

For the devices listed in [Table 1](#), the endpoint block for PCIe will not detect LCRC errors on downstream Power Management Message TLPs.

### Packet Accepted DLLPs and Replay Timer Expiring

For the devices listed in [Table 1](#), Packet Accepted DLLPs that are received at the same time that the replay timer expires can cause the endpoint block for PCIe to indicate a fatal error.

## Memory Controller Block (MCB)

### *MCB Calibration*

In the devices listed in [Table 1](#), for designs using Calibrated Input Termination, use these FGG484 pin locations for the RZQ reference resistor: MCB Bank 1 – pin P19, MCB Bank 3 – pin K7.

### *MCB and Suspend*

In the devices listed in [Table 1](#), the MCB does not support self-refresh mode of the external memory during FPGA Suspend.

### *MCB Address Bus Hold Time*

In the devices listed in [Table 1](#), some bits of the MCB address bus (mcbx\_dram\_addr) can violate the input hold time ( $t_{IH}$ ) specification of the memory device.

#### **Work-around**

See [Answer Record 34089](#).

## DCM Minimum Frequency

The Digital Clock Manager (DCM\_SP or DCM\_CLKGEN) minimum frequency does not meet the data sheet specifications in the devices listed in [Table 1](#). The following specifications deviate from the data sheet:

- CLKIN\_FREQ\_DLL Min: 25 MHz
- CLKOUT\_FREQ\_CLK0 Min: 25 MHz
- CLKOUT\_FREQ\_CLK90 Min: 25 MHz
- CLKOUT\_FREQ\_2X Min: 50 MHz
- CLKOUT\_FREQ\_DV Min: 1.6 MHz
- CLKIN\_FREQ\_FX Min: 0.8 MHz
- CLKOUT\_FREQ\_FX Min: 25 MHz
- CLKOUT\_FREQ\_FXDV: 0.8 MHz

## BUFPLL LOCK Output

In the device listed in [Table 1](#), the BUFPLL LOCK output might stay High when the PLL\_BASE LOCKED signal is Low. As a result, the timing of the SERDESSTROBE signal might change after the PLL has been reset.

#### **Work-around**

Any application that performs a training, framing, or Bitflip function on the incoming data should be reinitialized following a PLL reset to ensure correct data reception.

## Device DNA

Device DNA is not supported in the devices listed in [Table 1](#). Do not use this feature.

## Operational Guidelines

### *Design Software Requirements*

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx development software installation:

- Speed specification v1.01, Xilinx ISE Design Suite 11.3, but no later than speed specification v1.12 and Xilinx ISE Design Suite 12.3 (see [Answer Record 39545](#)).

## Operating Conditions Required when Using I/O Delay Variable Mode

In the devices listed in Table 1, when using I/O Delay Variable Mode, the operating conditions must be:

- $V_{CCINT} = 1.20V$  to  $1.26V$
- Junction temperature ( $T_J$ ) =  $25^{\circ}C$  to  $85^{\circ}C$

The I/O delay variable mode (also known as I/O delay calibration and reset) is used when the IODELAY2 CAL or RST are used or when IODELAY2 IDELAY\_TYPE attribute is set to VARIABLE\_FROM\_ZERO, VARIABLE\_FROM\_HALF\_MAX, or DIFF\_PHASE\_DETECTOR.

## Notes and Recommendations

### Charged Device Model ESD Protection

The Charged Device Model (CDM) ESD for the GTP transceiver pins MGTRREF and MGTAVTTRCAL deviates from the qualification acceptance criteria of 250V in the devices listed in Table 1. These pins meet a CDM ESD level of 100V.

## Traceability

The XC6SLX45T is marked as shown in Figure 1. The other devices in Table 1 are marked similarly.

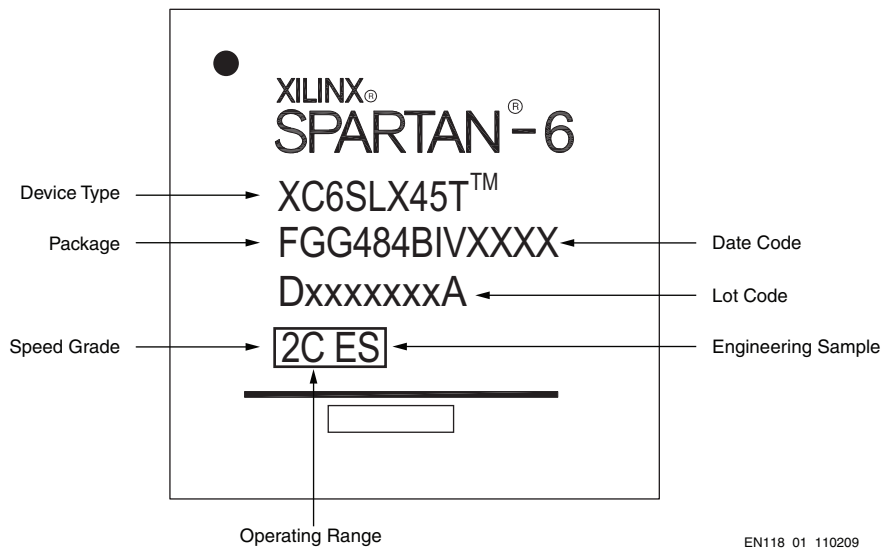


Figure 1: XC6SLX45T-2FGG484CES Marking

## Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact.htm>.

## Revision History

Date	Version	Description
09/28/09	1.0	Initial Xilinx release.
10/13/09	1.1	Improved <a href="#">DCM Minimum Frequency</a> with reduced specifications. Removed the Quiescent Current operational guideline because it is not a deviation from existing specifications; see <a href="#">Answer Record 33641</a> for more information on quiescent current.
11/02/09	1.2	Added <a href="#">MCB and Suspend</a> and <a href="#">Readback CRC</a> .
02/17/10	1.3	Added <a href="#">MCB Address Bus Hold Time</a> .
05/07/10	1.4	Added <a href="#">Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode</a> and <a href="#">9K Simple Dual Port Block RAM Width Restriction</a> sections. Added (or later) to software version.
03/18/11	1.5	Added <a href="#">IODELAY2</a> , <a href="#">9K Block RAM Initialization</a> , <a href="#">Configuration Readback When Using 9K Block RAM</a> , and <a href="#">BUFPLL LOCK Output</a> . Updated <a href="#">Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode</a> and <a href="#">Design Software Requirements</a> .

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