Spartan-6 FPGA LX9, LX16, LX25/T, LX45/T, LX75/T, LX100/T, and LX150/T CES9951 Errata

EN147 (v1.3) March 18, 2011 **Errata Notification**

Introduction

Thank you for participating in the Spartan®-6 FPGA Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the Spartan-6 devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	XC6SLX9 CES9951	JTAG ID (Revision Code): 0
	XC6SLX16 CES9951	JTAG ID (Revision Code): 3
	XC6SLX25 CES9951	JTAG ID (Revision Code): 0
	XC6SLX25T CES9951	JTAG ID (Revision Code): 0
	XC6SLX45 CES9951	JTAG ID (Revision Code): 3
	XC6SLX45T CES9951	JTAG ID (Revision Code): 3
	XC6SLX75 CES9951	JTAG ID (Revision Code): 0
	XC6SLX75T CES9951	JTAG ID (Revision Code): 0
	XC6SLX100 CES9951	JTAG ID (Revision Code): 0
	XC6SLX100T CES9951	JTAG ID (Revision Code): 0
	XC6SLX150 CES9951	JTAG ID (Revision Code): 3
	XC6SLX150T CES9951	JTAG ID (Revision Code): 3
Packages	All	
Speed Grades	-2, -3	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

IODELAY2

In the devices listed in Table 1, the IODELAY2 block can experience late data edge delays, early data edge delays, and single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

Late Data Edge Delay in IDELAY and ODELAY Modes

The IODELAY2 block can add up to 350 ps of delay on the rising or falling edge transitions when the IDELAY_VALUE or ODELAY_VALUE is 4 or higher for all IDELAY_TYPE settings or when used as output delay. This behavior can be present at all data rates and should be included in system timing margin analysis.

Early Data Edge Delay in ODELAY Mode

The IODELAY2 block used in the ODELAY mode can generate a data edge up to 350 ps early on the rising or falling edge transitions. This behavior can be present at data rates higher than 533 Mb/s and for all ODELAY_VALUE settings and should be included in system timing margin analysis.

Single Data Bit Corruption in IDELAY and ODELAY Modes

The IODELAY2 block can corrupt a single data bit for all IDELAY_TYPE settings or when used in ODELAY mode.

Work-arounds

IDELAY_TYPE=DEFAULT

The data rate must not exceed 250 Mb/s to avoid data corruption.

IDELAY_TYPE=FIXED or VARIABLE_FROM_ZERO or When Used in ODELAY Mode

The IDELAY_VALUE or ODELAY_VALUE must not exceed the values in Table 2 to avoid data corruption at the indicated data rate.

Table 2: **Maximum IDELAY_VALUE or ODELAY_VALUE**

Data Rate (Mb/s)	Bit Time (ps)	Maximum DELAY Value
1,050	952	7
1,000	1,000	8
945	1,058	9
800	1,250	14
667	1,499	20
625	1,600	22
533	1,876	28
400	2,500	43
333	3,003	54
266	3,759	72
200	5,000	101
188	5,319	107

IDELAY_TYPE=VARIABLE_FROM_HALF_MAX

The data rate must not exceed 400 Mb/s, the IODELAY2 IOCLK frequency must be equal to the data rate, and the positive increment must not exceed 5 to avoid data corruption.

IDELAY_TYPE=DIFF_PHASE_DETECTOR

The data rate must not exceed 400 Mb/s and data to clock skew, including package trace difference, must not exceed 0.15 UI to avoid data corruption.

See Answer Record 38408 for additional information.

Memory Controller Block (MCB)

MCB Not Supported

The memory controller block (MCB) is not supported in the devices listed in Table 1.

Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) READ_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

The recommended work-around to avoid memory array corruption issue is to configure the block RAM in WRITE_FIRST mode. WRITE_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.3 and later.

See Answer Record 34533.

9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWER in Simple Dual Port (SDP) mode (RAM_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA_WIDTH_A=36, DATA_WIDTH_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

See Answer Record 34541.

9K Block RAM Initialization

Block RAM used in the 9K mode (RAMB8BWER) can fail to initialize user data or default values during configuration in the devices listed in Table 1.

This issue will not be fixed in the devices listed in Table 1.

Work-arounds

Either use 18K block RAM or write to the 9K block RAM to initialize it after configuration.

See Answer Record 39999.

Configuration

BPI Configuration Not Supported in LX25/T Device

Master BPI mode for configuration is not supported in the XC6SLX25 and XC6SLX25T devices listed in Table 1. The other devices in Table 1 that support Master BPI configuration are not affected.

See Answer Record 36521 for additional information.

This issue will not be fixed in the XC6SLX25 and XC6SLX25T devices listed in Table 1.

Work-around

Alternative configuration modes include Master SelectMAP mode with a Xilinx Platform Flash PROM or Master SPI mode, including x4 mode with a quad SPI Flash.

16-Bit SelectMAP Configuration Maximum CCLK Frequency for LX100/T Devices

The maximum CCLK configuration frequency has been revised from 40 MHz to 35 MHz for 16-bit-wide SelectMAP mode for the XC6SLX100/T devices listed in Table 1. SelectMAP mode is also known as slave parallel or BPI mode. The parameters affected are F_{SMCCK} for slave mode (x16 only) and F_{MCCK} for master mode (SelectMAP/BPI x16 only). This change is included in DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*, v1.10, November 4, 2010. All designs using 16-bit SelectMAP in the XC6SLX100/T devices should use a configuration frequency of less than 35 MHz. No software changes are associated with this revision.

See Answer Record 38733 for additional information.

Configuration Readback When Using 9K Block RAM

Configuration readback can corrupt 9K block RAM (RAMB8BWER) data. Configuration readback (including iMPACT Verify) is not supported when 9K block RAM is used in the devices listed in Table 1. However, readback CRC (POST_CRC), which is typically used for SEU detection, is supported.

This issue will not be fixed in the devices listed in Table 1.

Work-around

Use 18K block RAM if configuration readback will be used.

See Answer Record 39977.

SCD9951 Test Conditions

The devices listed in Table 1 support the Industrial temperature range (T_j = –40°C to + 100°C), unless otherwise specified.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installation:

- Speed specification v1.08 (or later), Xilinx ISE Design Suite 12.1 (or later).

Traceability

The XC6SLX45T is marked as shown in Figure 1. The other devices in Table 1 are marked similarly.

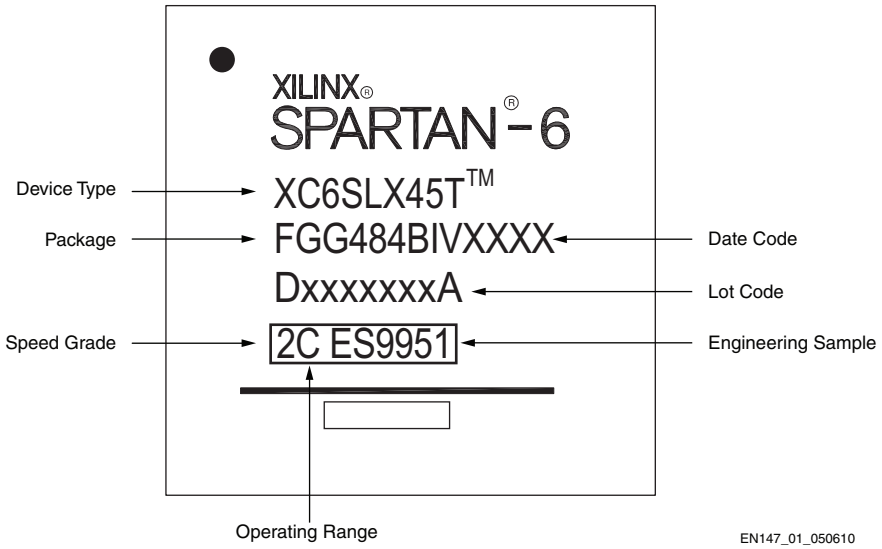

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
05/25/10	1.0	Initial Xilinx release under limited distribution.
06/16/10	1.0.1	Published to http://www.xilinx.com.
06/25/10	1.1	Removed the Spartan-6 LX4 device.
07/02/10	1.2	Added BPI Configuration Not Supported in LX25/T Device.
03/18/11	1.3	Added IODELAY2, 9K Block RAM Initialization, 16-Bit SelectMAP Configuration Maximum CCLK Frequency for LX100/T Devices, and Configuration Readback When Using 9K Block RAM. Updated Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode.

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