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How an FPGA Approach to Complex System Design Can Improve Profitability: Real Case Studies

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Large OEMs today are seeing their profit margins threatened by the need to adjust their products in the face of quickly changing market requirements. Each time a new market requirement surfaces, new products must be commissioned to meet this challenge. In addition, the cost of new System-on-a-Chip (SoC) designs at the current 28nm process node can run as high as $100M if all device parameters are maxed out (largest die, fastest part, highest pin count, etc.). Companies that fail to adjust quickly run the risk of losing market share to their competition and possibly never making back their investment in silicon design costs.

One of the ways to reduce risk is through the use of programmable logic in the form of FPGA (Field Programmable Gate Arrays). The conventional thinking is that FPGA solutions cannot provide the right cost structure to allow both a substantial reduction in cost and also meet volume production requirements. Semico Research has found data that counters this view and has detailed these findings in the following study.

This white paper quantifies the impact on profitability by using metrics developed by Advance Tech Marketing and Semico Research Corp. In the process of performing this analysis, real data points are used to produce a series of curves that depict the impact of silicon costs and differences in time to market have on profitability.

This white paper captures and uses hard data points in the following manner:

1. Design costs, silicon prices and board prices are based on surveys and industry benchmark information.
2. Silicon unit shipments are based on a classic product market life cycle curve (from introduction and ramp to market saturation)
3. Methodology used for data calculations:
   - Board Cost = Silicon Unit Cost * Number of Board Sales
   - Board Revenue = Board Price * Number of Board Sales
   - Board Profit = Board Revenue – Board Cost – Design Cost

   (Note: Design Cost is amortized monthly through the lifetime of the product)
4. The same methodology is used to calculate the monthly and cumulative board profits for an FPGA / EasyPath design approach, an FPGA-only design approach and for a SoC design approach.
5. This methodology is repeated for both profiled applications in the white paper.

We have profiled two separate applications in this white paper:

- A Remote Radio Head board for use in a Cellular Base Station application
- A Server processor blade for use in a Data Center Application.

In each profiled case study, an early market entrant using FPGAs is followed by a late market entry from a competitor using a SoC or ASIC solution. The difference between an early market entry and a late entry has an impact on market share and extends to adversely affect the profitability of the late market entrant.

The following case studies, complete with graphs and tables, detail the Board Profits of both companies for each of the profiled applications.

Remote Radio Head Board Application

In this application, Company #1 does their initial design using FPGAs and enters its market on time and with a relatively low design cost. Company #2 enters the market 6 months late using a SoC approach which carries a much higher design cost and the added problem of being late to market compared to their competition. The following table details the data points used for both companies and both silicon design solutions.

Table 1: Remote Radio Head Board Application

FPGA Design Cost	$1,000K
FPGA Unit Price	$100
FPGA / EasyPath yearly reduction	8%
FPGA to EasyPath Design Cost	$ 300K
EasyPath Unit Price Reduction from FPGA	35%
ASIC Design Cost	$20,000K
ASIC Starting Unit Price	$20
ASIC yearly reduction in first year	20%
ASIC yearly reduction after first year	8%
TAM units	4,000,000
System Board Price (1st year)	$1,000
System Board Price (2nd year)	$900
System Board Price (3rd year)	$800
Early Entry % TAM volume	49%
Initial Late Entry % TAM volume	38%
Other Late Entrants % TAM volume	13%

Source: Semico Research Corp. and Advance Tech Marketing

Notes:

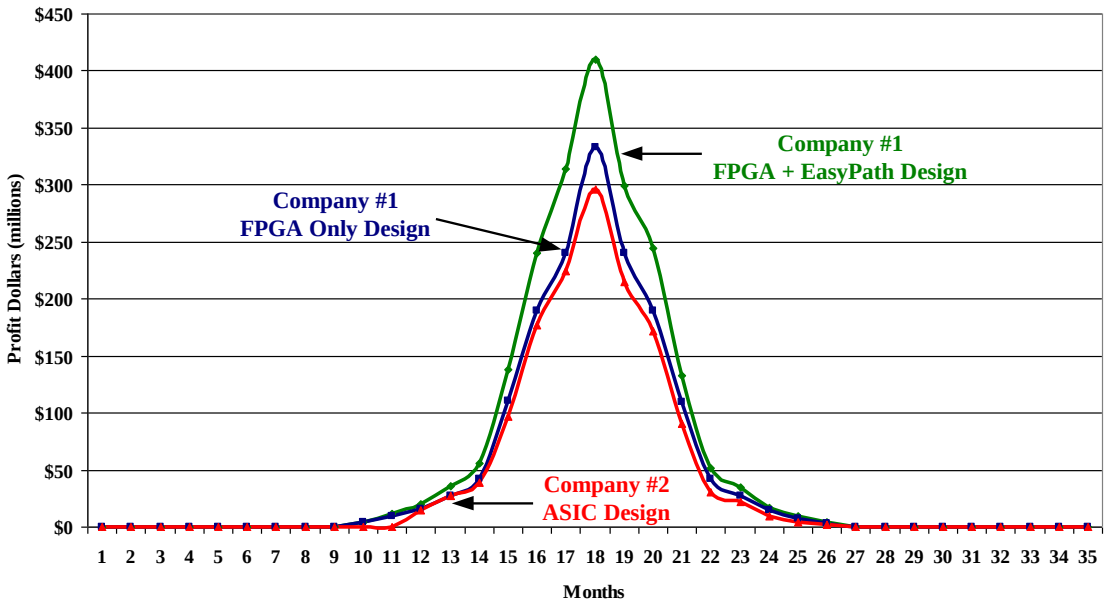
FPGA Unit Price: 1 FPGA per board. ASP $100 (1 x $100= $100)
FPGA Design Cost: $200K / person year, 5PY = $1M (6-7 engineers for 9 months)
ASIC Design Cost: Labor + NRE (mask, packaging, prototype cost and testing)

In this application, Company #2 has opted to do a low-to-medium-scale SoC costing approximately $20M. The FPGA application from Company #1 costs only $1M to design and is completed on time, allowing an early market entry. The SoC is late to market by 6 months due to timing closure and signal integrity issues and respins.

For this scenario, the market ramp is fairly aggressive as cellular base station OEMs tend to deploy new solutions into the market quickly to meet changing market requirements. Once initial deployment is under way, this application usually sees a 'long tail' where the new boards continue to be deployed, but with much lower volumes.

Figure 1 shows the impact on Company #2's profits caused by their late entry. This figure also shows a comparison between an FPGA + Easy Path solution, an FPGA only solution and the ASIC Solution.

Figure 1: Early and Late Market Entry Board Profits: Remote Radio Head Application



Source: Semico Research Corp. and Advanced Tech Marketing

A late entry also impacts Company #2's market share since they now need to displace Company #1 from sockets gained through an early market entry.

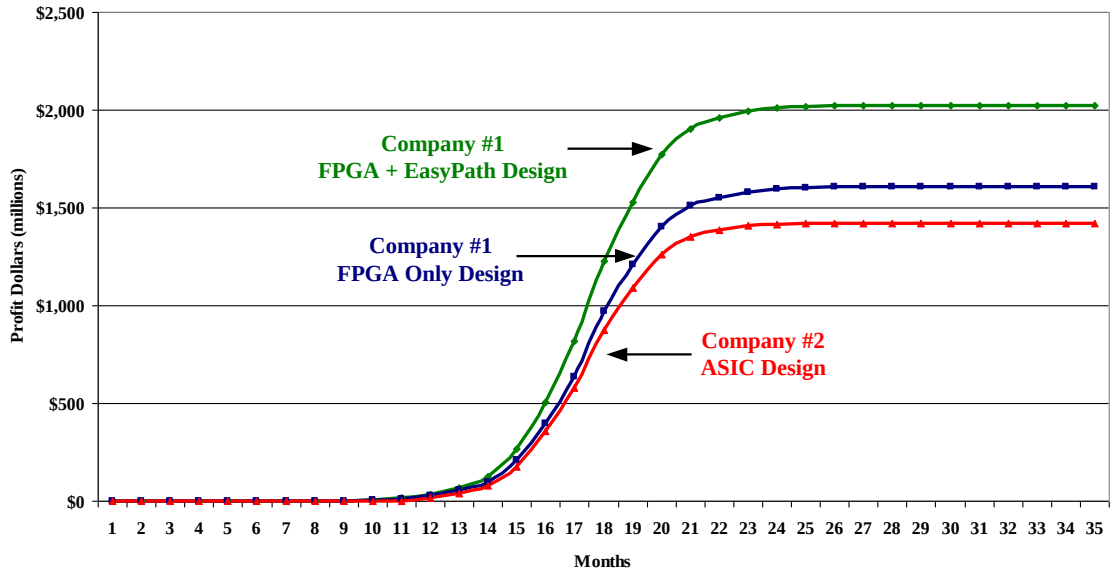
However, this is not the whole story. As Company #1 enjoys success with their product, they need both additional volumes and a lower device cost to meet their profitability targets over the life of their product. Company #1 employed a strategy of moving their FPGA design to a lower cost design option at a predetermined point in their production ramp. EasyPath™ is a lower-cost option for FPGAs provided by Xilinx® to help reduce the BOM cost once the design no longer needs programmability. EasyPath devices are FPGAs custom tested to a design, and can deliver as much as 35% lower cost compared to standard FPGAs. There is an additional design cost to convert to an EasyPath solution, but, at only $300K, it is minimal compared to the SoC design costs. This strategy by

Customer #1 ensured access to the lower unit price at the right time in the production ramp to capture additional market share.

This application has a limited number of competitors in the market at any one time. Company #1, because of its early market entry, captures the majority of available boards. Company #2, due to their late market entry, captures fewer boards. Even though they are late to market, Company #2 does capture a reasonable amount of market share since there are fewer competitors, but at a lower ASP compared to Company #1, resulting in lower profitability and market share over time.

Company #2 also was able to cost reduce their SoC through working with their foundry partner to achieve better yields, but cannot make up for their late market entry and the lost profits due to lower unit shipments. Company #2 must also reduce the ASP of their board solution almost right from introduction because they were late to market and must 'buy' market share to displace their competitor. This also has an adverse effect on profitability.

Figure 2: Early and Late Market Entry Cumulative Board Profits: Remote Radio Head Application



Source: **Semico Research Corp. and Advanced Tech Marketing**

As Figure 2 shows, the combination of an FPGA design with a switchover to an EasyPath solution at a predetermined point in the production ramp produces a significant increase in the profits Company #1 has generated compared to Company #2 with their SoC approach. Since the SoC design cost is appreciably more than the combined FPGA and EasyPath solution, it takes Company #2 longer to recoup their design investment. In addition, since the SoC solution is new and just ramping into production, the yields at the

beginning of the silicon production ramp can fluctuate or be unstable. This can put additional pressure on Company #2's final market share for this application since they may not have the units available to meet market demand as and when it occurs.

Conclusions for Remote Radio Head Application

The combined FPGA and EasyPath solution helped Company #1 enter the market early. This head start on the competition resulted in Company #1 generating $286M more in board profits and in shipping 49% of the total available units in this market. In addition, the use of an EasyPath solution helped Company #1 stabilize their profits at a time in the production ramp when the market demand was peaking. Without the EasyPath cost reduction solution, Company #1 might have missed their profitability targets altogether and suffered substantially lower profits.

Data Center Server Processor Blade Application

This application is substantially different from the Remote Radio Head application because it follows a much different product roadmap. In large part, processor blades for server applications are driven by the introduction of new X86 processors from Intel. This causes the production ramp of new products to be much sharper and shorter than the Remote Radio Ahead application. In addition, this market has a much larger unit TAM and holds many more competitors than does the first market profiled. This results in greater competition and downward ASP pressure.

In this application, Company #1 does their initial design using FPGAs and enters its market on time and with a relatively low design cost and no yield issues because the FPGA is an 'off-the-shelf" solution. Company #2 enters the market 3 months late using a SoC approach which carries a much higher design cost and the added problem of unstable yield compared to their competition. The following table details the data points used for both companies and both silicon design solutions.

Table 2: Data Center Server Processor Blade Application

FPGA Design Cost	$3,200K
FPGA Starting Unit Price	$1,500
FPGA / EasyPath yearly reduction	8%
FPGA to EasyPath Design Cost	$ 300K
EasyPath Unit Price Reduction from FPGA	35%
ASIC Starting Unit Price	$400
ASIC Yearly reduction in first year	20%
ASIC yearly reduction after first year	8%
ASIC Design Cost	$85,000K
TAM units	2,000,000
System Board Price (1st year)	$4,000
System Board Price (2nd year)	$3,200
System Board Price (3rd year)	$2,750
Early Entry % TAM volume	46%
Initial Late Entry % TAM volume	28%
Other Late Entrants % TAM volume	26%

Source: Semico Research Corp. and Advance Tech Marketing

Notes:

FPGA Unit Price: 4 FPGAs per board. ASP $375 (4 x $375 = $1,500)
FPGA Design Cost: $200K / person year, $3.2M = 16 (5-6 engineers for 9 months per FPGA design)
ASIC Design Cost: Labor + NRE (mask, packaging, prototype cost and testing)

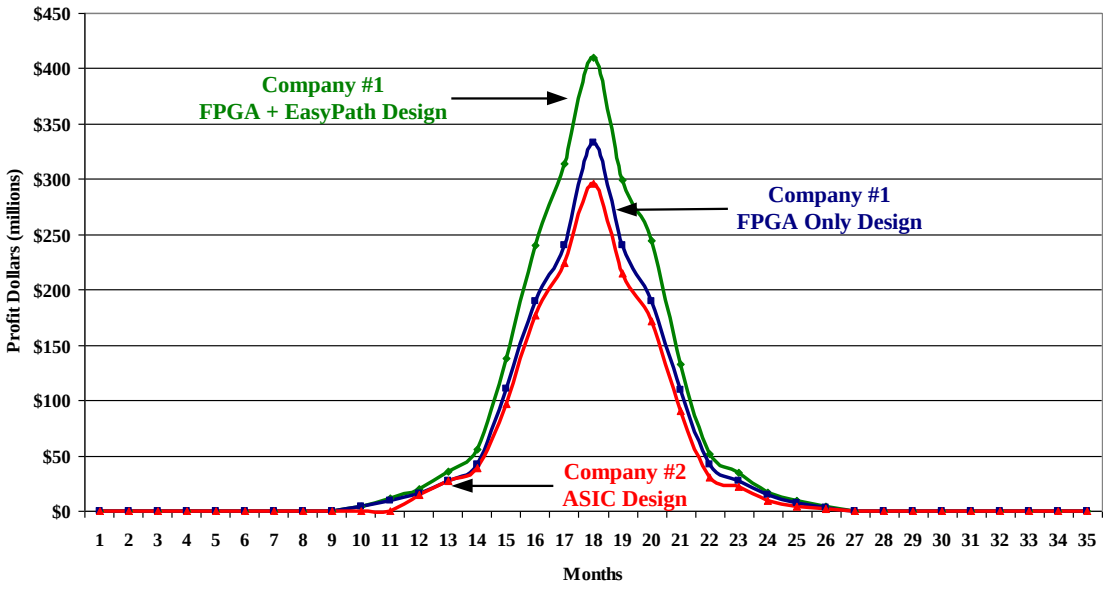
For this application, Company #2 has opted to do a medium-to-high-scale SoC costing approximately $85M. The FPGA application from Company #1 costs $3.2M to design and is completed on time, allowing an early market entry. The SoC is late to market by 3 months. Also, 4 FPGAs are being used by Company #2 in this example to mirror a 60M gate SoC. This results in a substantially higher silicon cost compared to the first application.

For this scenario, the market ramp is aggressive as Data Center managers need to use the highest performing products as quickly as possible to meet dramatically rising market requirements for bandwidth. Once initial deployment is under way, this application usually sees a rapid increase in units to reach a peak approximately one year after introduction. Then, there can be a rapid falloff of shipments since the Intel product roadmap tends to follow a two year cycle.

In addition, since this market has a great many competitors, regular reductions in the board ASP are a requirement to participate. A ‘mid-life’ cost reduction generated by using the EasyPath program offered by Xilinx meets this requirement.

Figure 3 shows the impact on Company #2’s profits caused by their late entry.

Figure 3: Early and Late Market Entry Board Profits: Data Center Application



Source: Semico Research Corp. and Advanced Tech Marketing

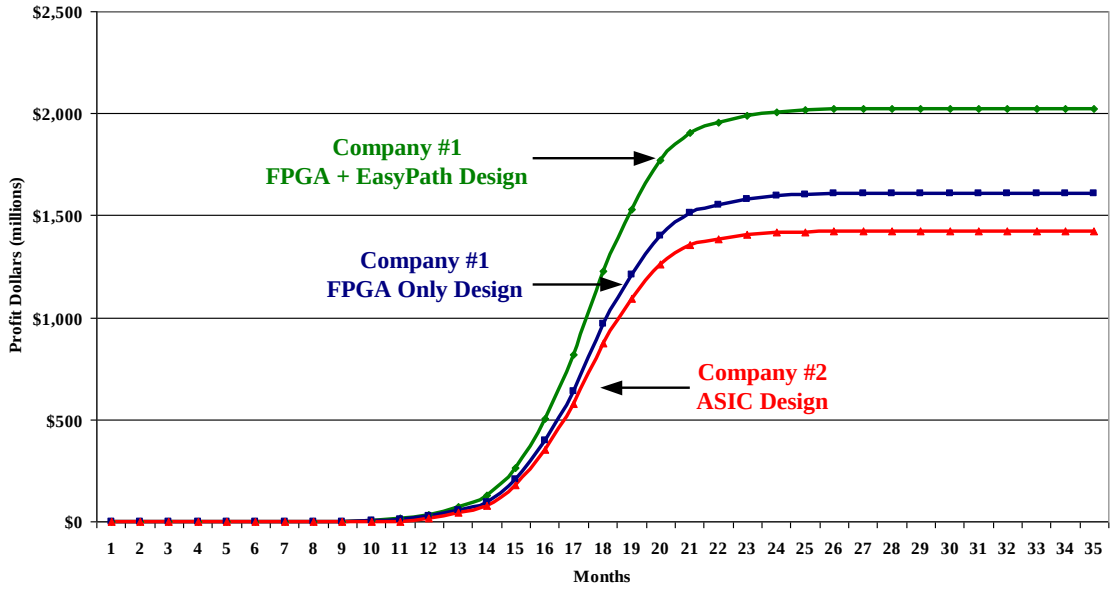
Please Note: Due to the very low unit volumes shipping at the beginning of market entry by Company #1 and Company #2, it appears as though both companies started shipments at the same time even though Company #2 was late to market by 3 months. This is due to the scale on the graph being used. Company #1 actually started their shipments in month 10 with the FPGA solution and by month 12 had generated $35.6M in profits. Company #2 started shipments in month 12 with the ASIC solution and generated only $14.9M in profits. Later, Company #2 generates higher profits, but is unable to catch up to Company #1 over the life of the product.

Company #1 generates higher profits over the life of the product compared to Company #2. A late entry also impacts Company #2's market share since they now need to displace Company #1 from sockets gained through an early market entry. Because this is a larger market, there are more competitors and Company #2, with its late market entry, can only generate around a 28% market share. The other late entrants split the remaining 26% of market share, and have even less success than Company #1 and Company #2.

As Company #1 enjoys success with their product, they need additional volumes and a lower device cost to meet their profitability targets over the life of their product. Company #1 employed a strategy of moving their FPGA design to an EasyPath design at a predetermined point in their production ramp. This ensured access to the right unit volumes at the right time and also gave them a cost reduction of 35% compared to the initial FPGA cost.

Company #2 also was able to cost reduce their SoC, but cannot make up for their late market entry and the lost profits resulting from lower unit shipments.

Figure 4: Early and Late Market Entry Cumulative Board Profits: Data Center Application



Source: **Semico Research Corp. and Advanced Tech Marketing**

As Figure 4 shows, the combination of an FPGA design with a switchover to an EasyPath solution at a predetermined point in the production ramp produces a significant increase in the profits Company #1 has generated compared to Company #2 with their SoC approach. Since the SoC design cost is significantly more than the combined FPGA and EasyPath solution, Company #2 will take longer to recoup their design investment and must retarget their silicon solution at other similar applications to generate more sales and profits.

Even though the unit cost per board for the FPGA / EasyPath solution was higher than the SoC solution over time, Company #1 generated an additional $600M in profits compared to Company #2 by being first to market. In addition Company #1 shipped 363K more units than Company #2.

Conclusions for Data Center Application

An early entry using a combination of an FPGA / EasyPath solution will generate higher profits and unit shipments than taking a SoC approach. The flexibility of the FPGA / EasyPath solution allowed Company #1 to pick the point in time to switch over to the EasyPath design to both increase their unit volumes and reduce their parts costs. Xilinx

has removed the Memorandum on Quantity (MOQ) requirement for customers using the EasyPath solution for the Virtex 6 and Virtex 7 product families, relieving inventory and reschedule pressures. Changes in production volume requirements are more easily accommodated than for a SoC solution that may be just ramping production and where yields might not yet be stable. There is also greatly reduced pressure to recover the FPGA design costs since the design effort is so much less than for the SoC, providing additional, long term benefits to Company #1's bottom line.

Summary

1. Two real case studies demonstrate that the FPGA and EasyPath approach enables greater total profit for applications >1M units (compared to SoC or ASIC).
2. The compression of the FPGA design cycle compared to the SoC design cycle allows for a much faster time to market.
3. Even though FPGA silicon is relatively more expensive compared to most SoC silicon, the reduction in the amount of design cost incurred by the customer is significant.
4. The lower design costs associated with an FPGA and EasyPath solution allows customers taking this approach to recoup their design costs much more readily than by pursuing a SoC design approach.
5. Fluctuations in yield during production ramp up of the SoC solution may become an issue for Company #2. By using the FPGA / EasyPath solution, Company #1 avoids these problems.
6. Early market entry by an OEM can produce substantially larger profits than by entering a market later even with a much better product,
7. The reason for this is that by the time a company enters the market some months after their competitor's initial entry, in order to gain market share, that initial market entrant must be displaced from the sockets he already possesses. This puts ASP and margin pressure on the late entrant's product, reducing his profitability by a substantial amount.
8. The ability to pick the point in time to switch over to an EasyPath solution provides a customer with greater production ramp flexibility than with the SoC solution.

Semico believes that the combination of an FPGA / EasyPath design approach can produce higher and more stable profits and allow companies taking this path to ship more product over time. This ensures both end customer satisfaction, by having access to the right solution at the right time in the market cycle, and better market share for the board vendor over the life of the end product.