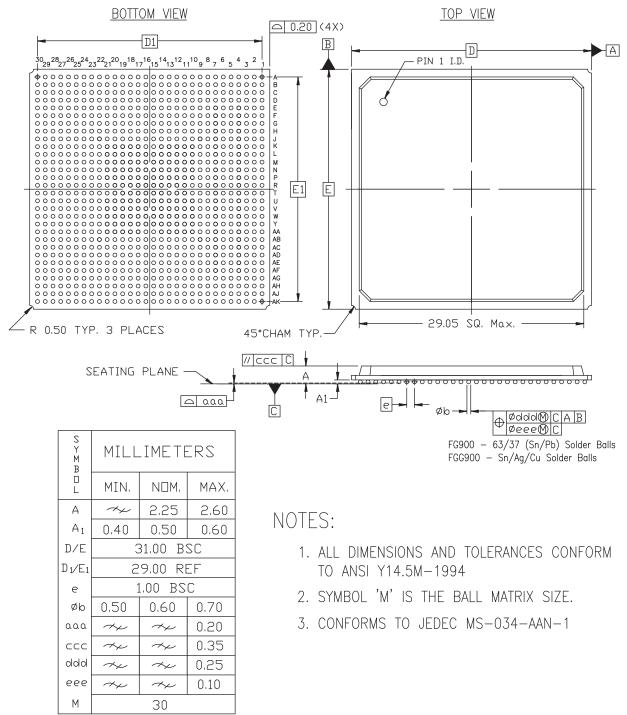


Fine-Pitch BGA (FG900/FGG900) Package

PK038 (v1.4) November 12, 2009



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Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
03/12/09	1.3	Removed note 3 regarding component land diameter. This dimension is specified in <u>UG112</u> , Device Package User Guide under Recommended PCB Design Rules.
11/12/09	1.4	Changed symbol ddd value from 0.30 to 0.25 to conform to JEDEC MS-034.

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