

Virtex-5 GTP Transceiver Interoperability: Virtex-II Pro RocketIO MGT

Characterization Test Report

RPT074 (v1.0) September 27, 2007



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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/27/07	1.0	Initial Xilinx release.

Virtex-5 GTP Transceiver Interoperability: Virtex-II Pro RocketIO MGT

Introduction

The purpose of this report is to communicate the conditions, results, and procedural methods used to achieve a quantified test of interoperation between a Virtex™-5 GTP transceiver and a Virtex-II Pro RocketIO™ MGT.

The scope of this testing covers electrical compatibility between the PMA layers of the devices under test (DUT A and DUT B). The TX and RX interfaces provided by the development platforms described below were used to facilitate the collection and generation of test results and test data, but were not considered as part of the test results.

This document briefly describes the DUTs and their associated development platforms. Eye diagrams captured at the test points shown in the block schematic diagram ([Figure 2](#)) are presented, along with the test setup and conditions. The results of a bit error ratio (BER) test are presented to demonstrate the high reliability of the communications link.

Test Description

Eye diagrams are commonly used to evaluate the quality of signals at different points along a serial link. A specific test pattern is used to produce a worst-case scenario for potential data distortion through the test medium.

Characterization Test Platforms

Virtex-II Pro Platform (DUT A)

Device:

Virtex-II Pro XC2VP7-FF672 FPGA

Test Platform:

ML321 Virtex-II Pro RocketIO Transceiver Characterization Board, Rev. F

Virtex-5 Platform (DUT B)

Device:

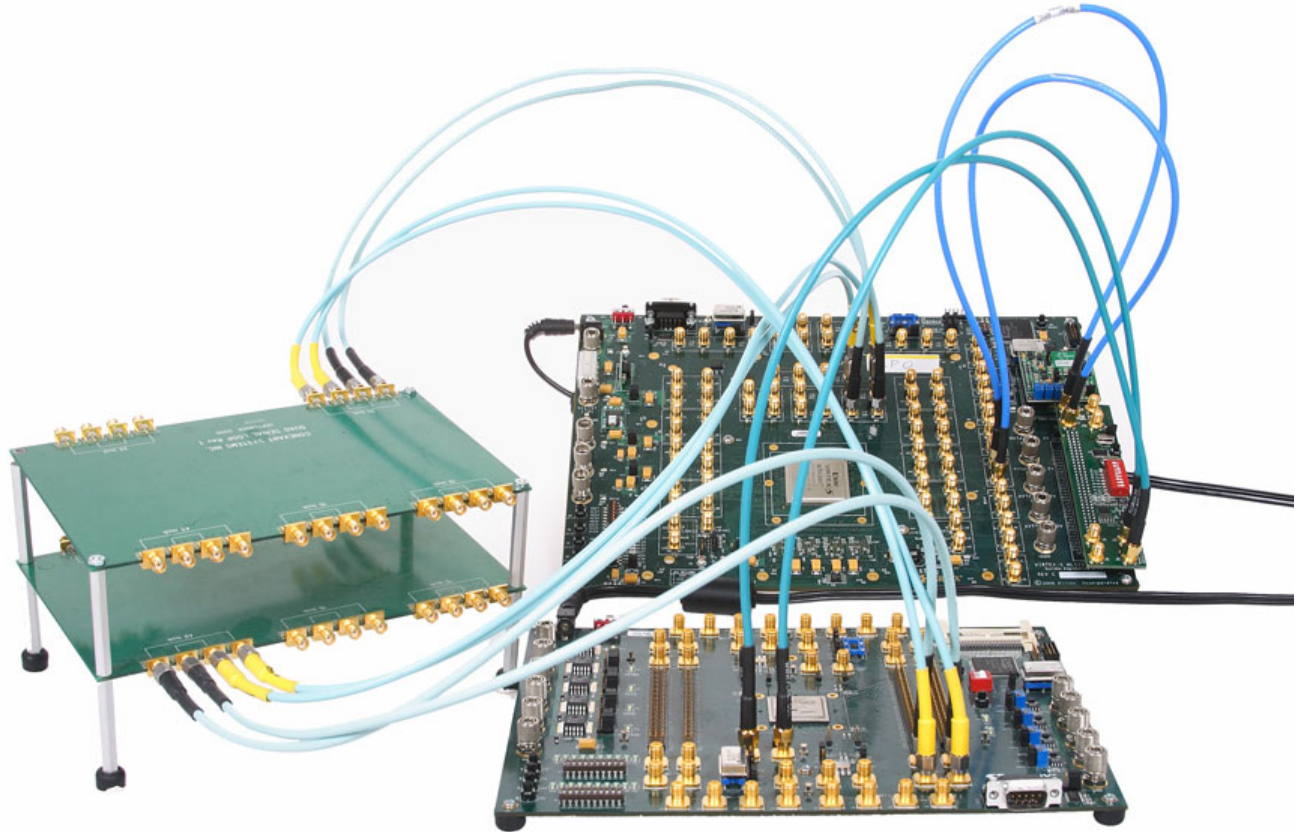
Virtex-5 XC5VLX50T-FF1136 FPGA

Test Platform:

ML523 Virtex-5 GTP Transceiver Characterization Board, Rev. C

Test Platforms and Interconnection

Figure 1 (photographically) and Figure 2 (schematically) show the test setup used for the transceiver interoperability characterization testing. External AC Coupling caps must be used for successful interoperability between transceivers of different families.



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Figure 1: Test Setup for Transceiver Interoperability Characterization

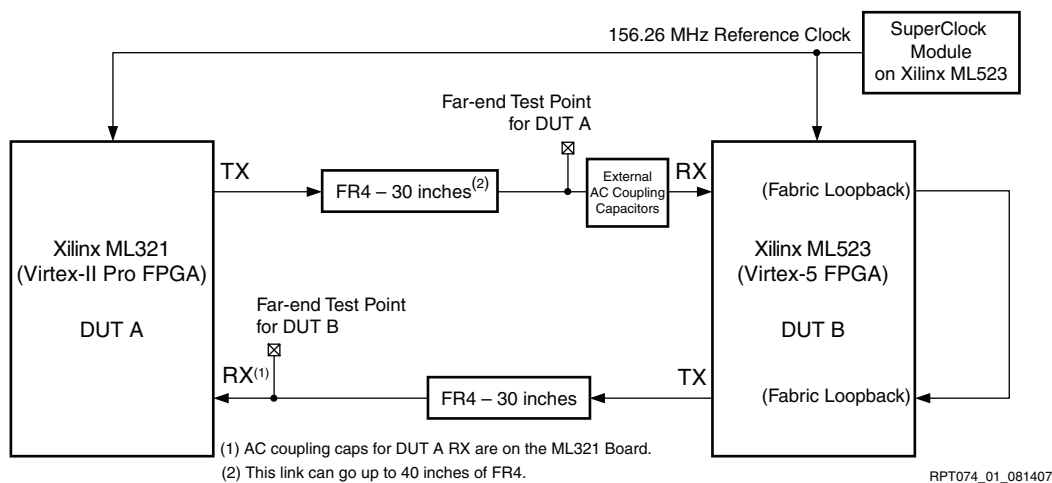


Figure 2: Test Setup for Transceiver Interoperability Characterization Block Diagram

Table 1 shows the transceiver PLL settings for the Virtex-II Pro Platform (DUT A).

Table 1: Transceiver Interoperability PLL Settings for Virtex-II Pro Platform (DUT A)

Data Rate	PLL Frequency (GHz)	REFCLK Frequency (MHz)	REFCLK_V_SEL	SERDES_10B
3.125 Gb/s	1.5625	156.25	1	FALSE

Table 2 shows the transceiver PLL settings for the Virtex-5 Platform (DUT B).

Table 2: Transceiver Interoperability PLL Settings for Virtex-5 Platform (DUT B)

Data Rate	PLL Frequency (GHz)	REFCLK Frequency (MHz)	PLL_DIVSEL_REF	PLL_DIVSEL_FB and DIV	PLL_TXDIVSEL_OUT, PLL_TXDIVSEL_COMM_OUT, PLL_RXDIVSEL_OUT	Over-sample
3.125 Gb/s	1.5625	156.25	1	2*5=10	1	1X

Table 3 lists the interoperability test setting for the Virtex-II Pro Platform (DUT A). Table 4 lists the interoperability test setting for the Virtex-5 Platform (DUT B). Table 5 lists the interoperability test conditions.

Table 3: Transceiver Interoperability Test Settings for Virtex-II Pro Platform (DUT A)

Attribute	Description	Set Value
TX_DIFF_CTRL	Controls the differential output swing.	800 (mV)
TX_PREEMPHASIS	Controls the output driver pre-emphasis to improve output waveform shaping for various load conditions.	3

Table 4: Transceiver Interoperability Test Settings for Virtex-5 Platform (DUT B)

Attribute/Port	Description	Set Value
TXBUFDIFFCTRL[2:0]	Controls the strength of the pre-drivers.	000
TXDIFFCTRL[2:0]	Controls the transmitter differential output swing.	000
TXPREEMPHASIS[2:0]	Controls the relative strength of the main drive and pre-emphasis.	011
RXENEQB	Active-Low port for enabling linear receive equalization. Receiver equalization is disabled when set to 1.	1

Table 4: Transceiver Interoperability Test Settings for Virtex-5 Platform (DUT B)

Attribute/Port	Description	Set Value
CHAN_BOND_1_MAX_SKEW	Sets the maximum amount of lane skew allowed when using channel bonding. Must be set less than 1/2 the minimum distance between channel bonding sequences.	Default
CHAN_BOND_2_MAX_SKEW		
AC_CAP_DIS	Disables built-in AC coupling capacitors on receiver inputs when set to TRUE.	TRUE
CLK25_DIVIDER	Sets the divider used to divide CLKIN down to an internal rate close to 25 MHz.	REFCLK/6
CLKINDC_B	Must be set to TRUE. Oscillators driving the dedicated reference clock inputs must be AC coupled.	TRUE
OOB_CLK_DIVIDER	Sets the squelch clock rate based on CLKIN.	3
OOBDETECT_THRESHOLD	Sets the minimum differential voltage between RXN and RXP before a signal is considered an electrical idle or a SATA OOB signal for a PCI™ design.	000
OVERSAMPLE_MODE	Enables 5X oversampling.	FALSE
PLL_SATA	Tie to FALSE. When FALSE, allows TX SATA operations to work at the SATA1 or SATA2 rate.	FALSE
PMA_RX_CFG	Adjusts CDR operation for oversampling and PLL_RXDIVSEL_OUT settings. This value enables the second-order loop filter.	0DCE089
RCV_TERM_GND	Sets the RX termination voltage to GND. Used with internal and external AC coupling to support TXDETECTRX for PCI EXPRESS® functionality.	FALSE
RCV_TERM_MID	Activates the internal RX termination voltage. Set to TRUE when RX built-in AC coupling is used.	FALSE

Table 4: Transceiver Interoperability Test Settings for Virtex-5 Platform (DUT B)

Attribute/Port	Description	Set Value
RCV_TERM_VTTRX	Sets RX termination voltage to VTTRX.	FALSE
TX_DIFF_BOOST	Changes the strength of the TX driver and pre-emphasis buffers. When set to TRUE, the pre-emphasis percentage is boosted or increased. Overall differential swing is reduced when TX_DIFF_BOOST is TRUE.	TRUE

Table 5: Transceiver Interoperability Test Conditions

Test Parameter	Test Value for the Virtex-II Pro Platform (DUT A)	Test Value for Virtex-5 Platform (DUT B)
Loopback Mode	N/A	Fabric Loopback
Pattern	PRBS-7	N/A (Fabric Loopback)
Silicon Corner Used	TT	TT
Transceiver Location	MGT 21	GTP 112_0
Ambient Temperature	25°C	25°C
Power Supplies	±2%	±2%
Test Board	ML321 Virtex-II Pro XC2VP7-FF672 Rev F	ML523 Virtex-5 XC5VLX50T-FF1136 Rev C
FR4 Length	30 inches	30 inches
REFCLK and PLL Rates	See Table 1	See Table 2

Results

[Figure 3](#) and [Figure 4](#) show the far-end eye diagrams for both DUT A and DUT B. The far-end eye for each device was measured closest to the remote receiver after going through (for DUT A) 40 inches of FR4, or (for DUT B) 30 inches of FR4. Refer to the test setup diagram in [Figure 2](#).

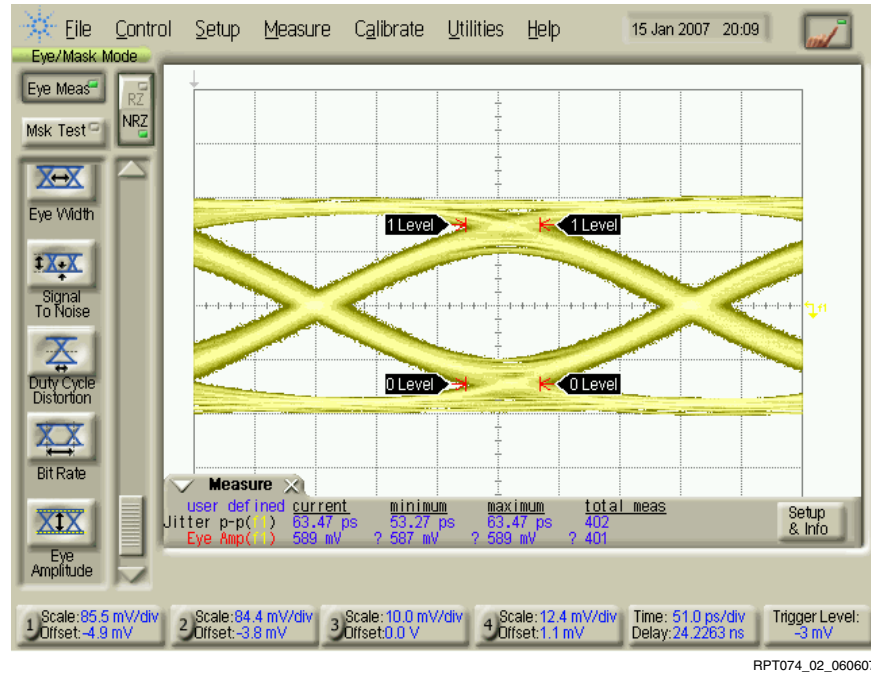


Figure 3: Far-End Eye at Virtex-5 Transceiver (DUT B) RX Input (40 in. FR4)

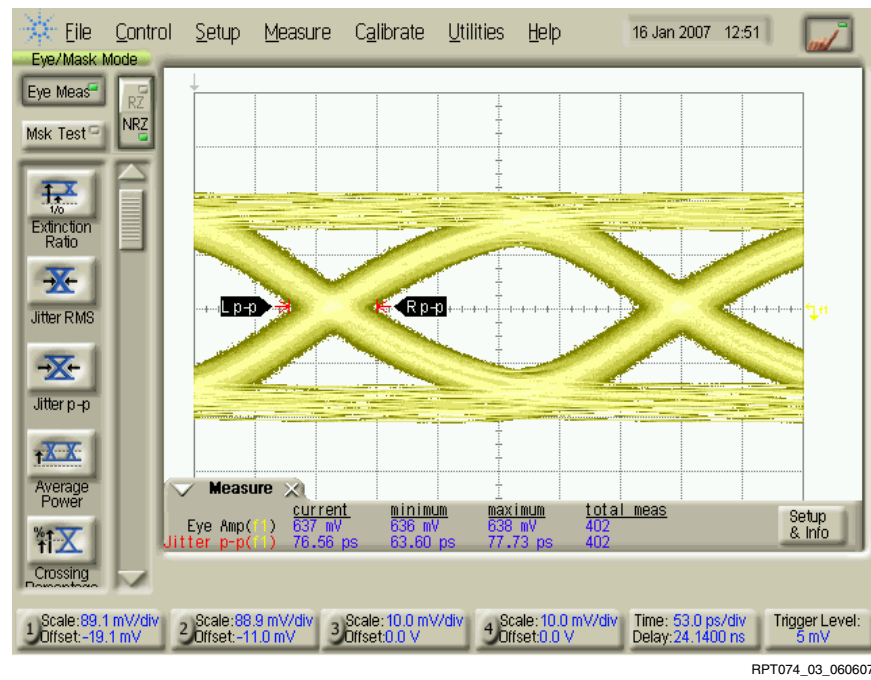


Figure 4: Far-End Eye at Virtex-II Pro Transceiver (DUT A) RX Input (30 in. FR4)

Conclusion

The test results (Table 6) were measured as observed on the receive counters of the Virtex-II Pro transceiver board (DUT A).

Table 6: Bit Error Ratio Test Results

Parameter	Value
Test Time	15 min
Received Bits	2.70E+012
Error Bits	0.00E+000
Calculated BER (assuming 1 bit in error)	0.37E-012

