Virtex-5 GTP Transceiver Interoperability: Virtex-4 RocketIO MGT

Characterization Test Report

RPT075 (v1.0.1) October 24, 2007

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/27/07	1.0	Initial Xilinx release.
10/24/07	1.0.1	Corrected typographical error, sentence above Table 6.

Virtex-5 GTP Transceiver Interoperability: Virtex-4 RocketIO MGT

Introduction

The purpose of this report is to communicate the conditions, results, and procedural methods used to achieve a quantified test of interoperation between a Virtex™-5 GTP transceiver and a Virtex-4 RocketIO™ transceiver.

The scope of this testing covers electrical compatibility between the PMA layers of the devices under test (DUT A and DUT B). The TX and RX interfaces provided by the development platforms described below were used to facilitate the collection and generation of test results and test data, but were not considered as part of the test results.

This document briefly describes the DUTs and their associated development platforms. Eye diagrams captured at the test points shown in the block schematic diagram (Figure 2) are presented, along with the test setup and conditions. The results of a bit error ratio (BER) test are presented to demonstrate the high reliability of the communications link.

Test Description

Eye diagrams are commonly used to evaluate the quality of signals at different points along a serial link. A specific test pattern is used to produce a worst-case scenario for potential data distortion through the test medium.

Characterization Test Platforms

Virtex-5 Platform (DUT A)

Device:
Virtex-5 XC5VLX50T-FF1136 FPGA

Test Platform:
ML523 Virtex-5 GTP Transceiver Characterization Board, Rev. C

Virtex-4 Platform (DUT B)

Device:
Virtex-4 XC4VFX60-FF1152 FPGA (CES4)

Test Platform:
ML423 Virtex-4 RocketIO Transceiver Characterization Board, Rev. C

Test Platforms and Interconnection

Figure 1 (photographically) and Figure 2 (schematically) show the test setup used for the transceiver interoperability characterization testing. External AC Coupling caps must be used for successful interoperability between transceivers of different families.
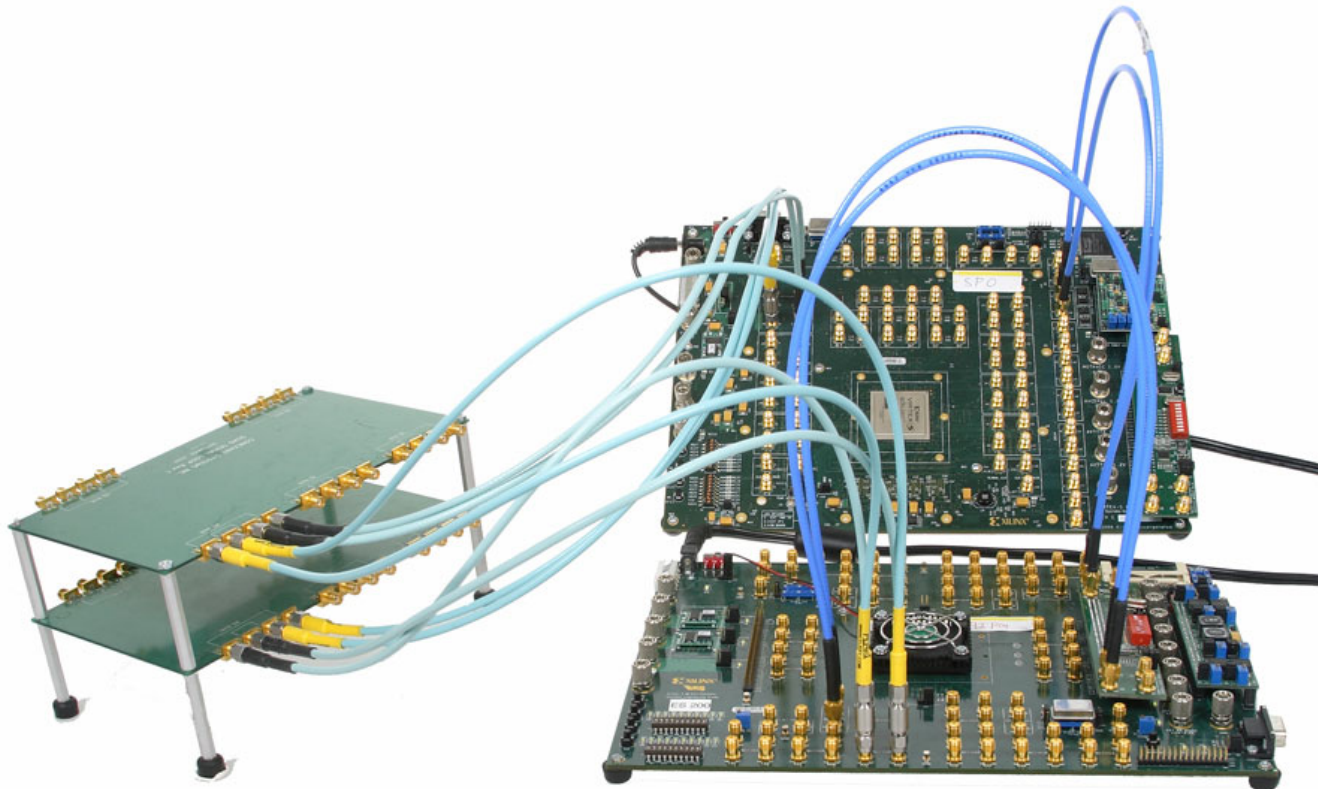
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Figure 1: **Test Setup for Transceiver Interoperability Characterization**
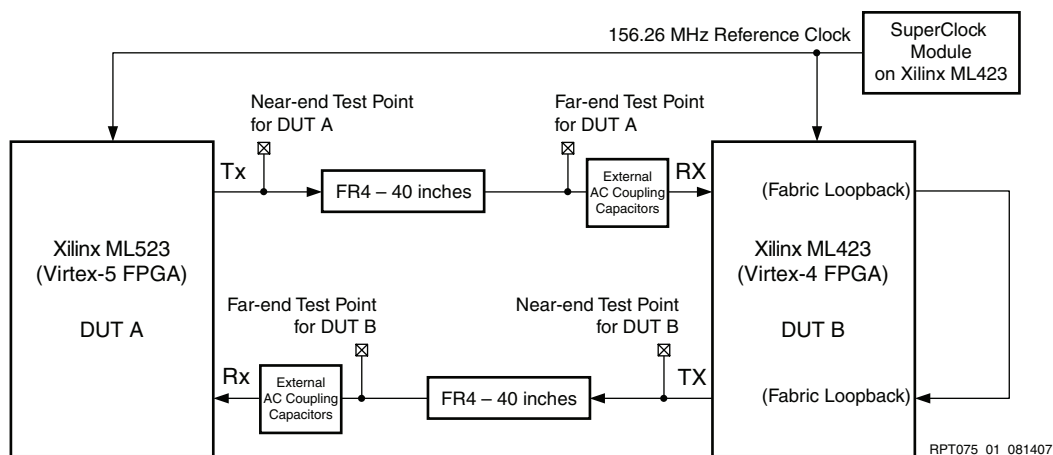
RPT075_01_081407

Figure 2: **Test Setup for Transceiver Interoperability Characterization—Block Diagram**

Table 1 shows the transceiver PLL settings for the Virtex-5 Platform (DUT A).

Table 1: **Transceiver Interoperability PLL Settings for Virtex-5 Platform (DUT A)**

Data Rate	PLL Frequency (GHz)	REFCLK Frequency (MHz)	PLL_DIVSEL_REF	PLL_DIVSEL_FB and DIV	PLL_TXDIVSEL_OUT, PLL_TXDIVSEL_COMM_OUT, PLL_RXDIVSEL_OUT	Over-sample
3.125 Gb/s	1.5625	156.25	1	2*5=10	1	1X

Table 2 shows the transceiver PLL settings for the Virtex-4 Platform (DUT B).

Table 2: **Transceiver Interoperability PLL Settings for Virtex-4 Platform (DUT B)**

Data Rate	PLL Frequency (GHz)	REFCLK Frequency (MHz)	TXPLLNDIVSEL, RXPLLNDIVSEL[3:0]	TXOUTDIV2SEL, RXOUTDIV2SEL[3:0]
3.125 Gb/s	1.5625	156.25	0110	0010

Table 3 lists the interoperability test setting for the Virtex-5 Platform (DUT A). Table 4 lists the interoperability test setting for the Virtex-4 Platform (DUT B). Table 5 lists the interoperability test conditions.

Table 3: **Transceiver Interoperability Test Settings for Virtex-5 Platform (DUT A)**

Attribute/Port	Description	Set Value
TXBUFDIFFCTRL[2:0]	Controls the strength of the pre-drivers.	000
TXDIFFCTRL[2:0]	Controls the transmitter differential output swing.	000
TXPREEMPHASIS[2:0]	Controls the relative strength of the main drive and pre-emphasis.	000
RXENEQB	Active-Low port for enabling linear receive equalization. Receiver equalization is disabled when set to 1.	0
RXEQMIX[1:0]	Controls the wideband/high-pass mix ratio for the RX equalization circuit.	00
RXEQPOLE[3:0]	Controls the location of the pole in the RX equalizer high-pass filter.	0000
CHAN_BOND_1_MAX_SKEW	Sets the maximum amount of lane skew allowed when using channel bonding. Must be set less than 1/2 the minimum distance between channel bonding sequences.	Default
CHAN_BOND_2_MAX_SKEW		
AC_CAP_DIS	Disables built-in AC coupling capacitors on receiver inputs when set to TRUE.	TRUE
CLK25_DIVIDER	Sets the divider used to divide CLKIN down to an internal rate close to 25 MHz.	REFCLK/6

Table 3: **Transceiver Interoperability Test Settings for Virtex-5 Platform (DUT A)**

Attribute/Port	Description	Set Value
CLKINDC_B	Must be set to TRUE. Oscillators driving the dedicated reference clock inputs must be AC coupled.	TRUE
OOB_CLK_DIVIDER	Sets the squelch clock rate based on CLKIN.	3
OOBDETECT_THRESHOLD	Sets the minimum differential voltage between RXN and RXP before a signal is considered an electrical idle or a SATA OOB signal for a PCI™ design.	000
OVERSAMPLE_MODE	Enables 5X oversampling.	FALSE
PLL_SATA	Tie to FALSE. When FALSE, allows TX SATA operations to work at the SATA1 or SATA2 rate.	FALSE
PMA_RX_CFG	Adjusts CDR operation for oversampling and PLL_RXDIVSEL_OUT settings. This value enables the second-order loop filter.	0DCE089
RCV_TERM_GND	Sets the RX termination voltage to GND. Used with internal and external AC coupling to support TXDETECTRX for PCI EXPRESS® functionality.	FALSE
RCV_TERM_MID	Activates the internal RX termination voltage. Set to TRUE when RX built-in AC coupling is used.	FALSE
RCV_TERM_VTTRX	Sets RX termination voltage to VTTRX.	FALSE
TX_DIFF_BOOST	Changes the strength of the TX driver and pre-emphasis buffers. When set to TRUE, the pre-emphasis percentage is boosted or increased. Overall differential swing is reduced when TX_DIFF_BOOST is TRUE.	TRUE

Table 4: **Transceiver Interoperability Test Setting for Virtex-4 Platform (DUT B)**

| Attribute	Description	Set Value
TXDAT_TAP_DAC[4:0]	Controls the drive strength of the data driver.	10110
TXPRE_TAP_PD	Disables the PRE driver, which disables the pre-emphasis.	1
TXPOST_TAP_PD	Disables the POST driver, which disables the pre-emphasis.	1
RXAFEEQ[2:0]	Controls the gain setting for the receive equalizer.	111
RXSELDACFIX[4:0]	Co-controls the CDR phase along with RXSELDACTRAN.	10000
RXSELDACTRAN[4:0]	Co-controls the CDR phase along with RXSELDACFIX.	10000
RXDCCOUPLE	Disables internal RX AC coupling caps.	1

Table 5: **Transceiver Interoperability Test Conditions**

Test Parameter	Test Value for Virtex-5 Platform (DUT A)	Test Value for Virtex-4 Platform (DUT B)
Loopback Mode	N/A	Fabric Loopback
Pattern	PRBS-7	N/A (Fabric Loopback)
Silicon Corner Used	TT	TT
Transceiver Location	GTP 122_0	MGT 109B
Ambient Temperature	25°C	25°C
Power Supplies	±2%	±2%
Test Board	ML523 Virtex-5 XC5VLX50T-FF1136 Rev C	ML423 Virtex-4 XC4VFX60-FF1152 Rev C
FR4 Length	40 inches	40 inches
REFCLK and PLL Rates	See Table 1	See Table 2

Results

Figure 3 and Figure 4 show the near-end and far-end eye diagrams for DUT A; Figure 5 and Figure 6 show the near-end and far-end eye diagrams for DUT B.

The near-end eye for each device was measured closest to its transmitter before going through 40 inches of FR4. The far-end eye for each device was measured closest to the remote receiver after going through 40 inches of FR4.
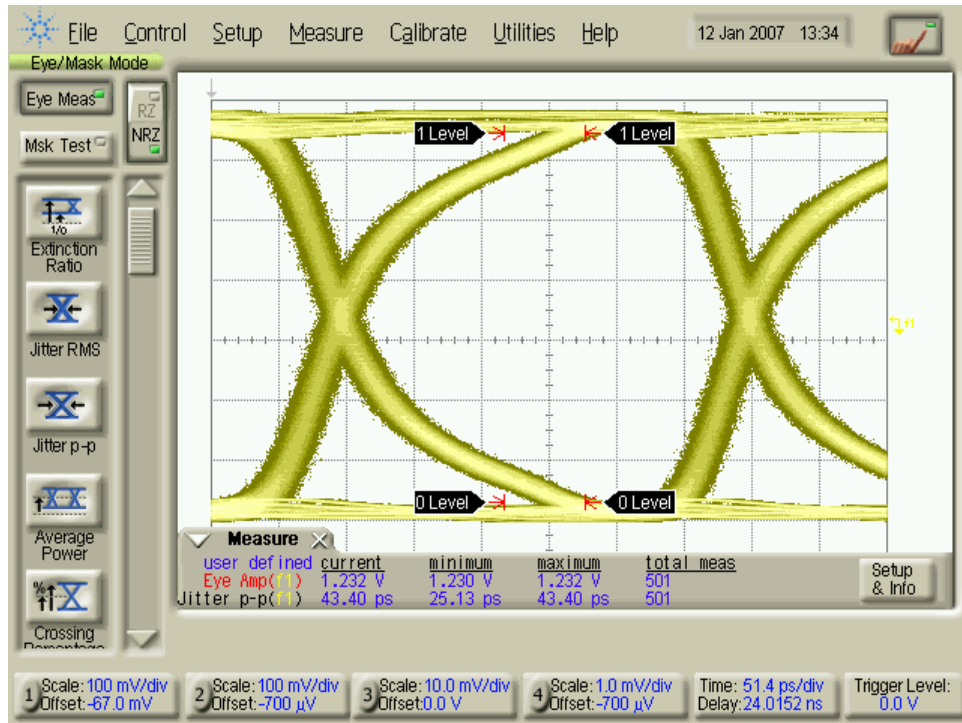
Figure 3: **Near-End Eye Diagram at Virtex-5 Transceiver (DUT A) TX Output**
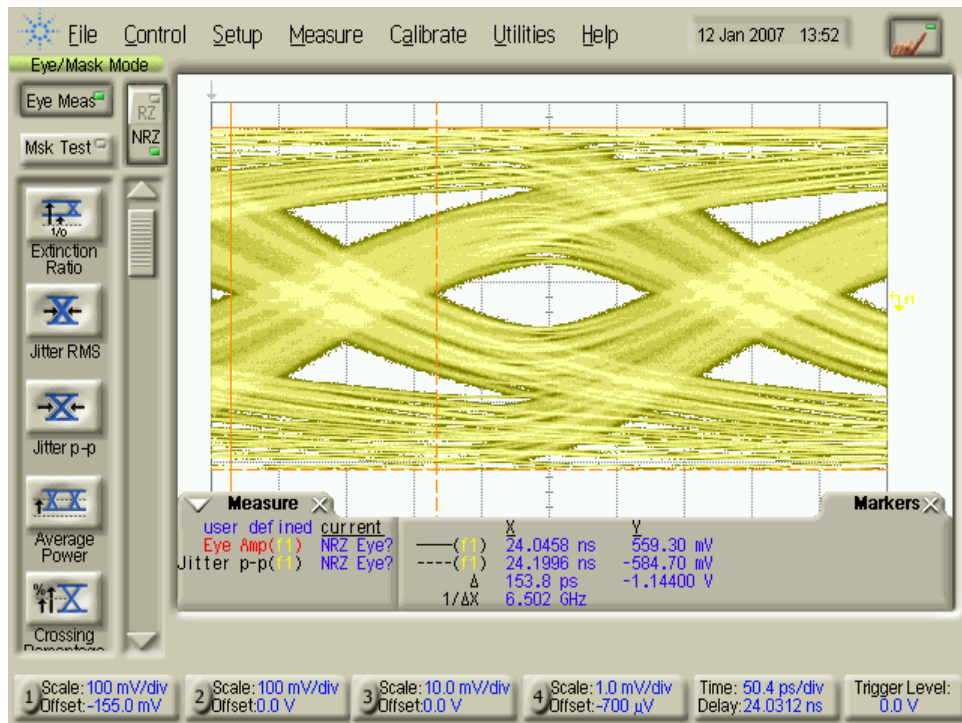
Figure 4: **Far-End Eye Diagram at Virtex-4 Transceiver (DUT B) RX Input (40 In. FR4)**
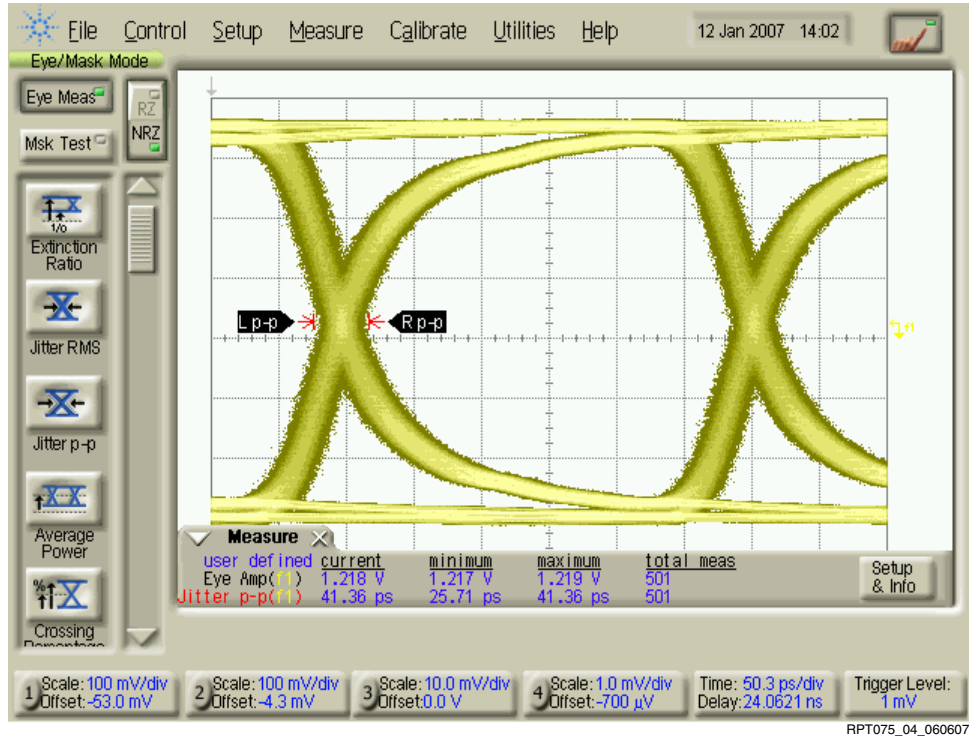
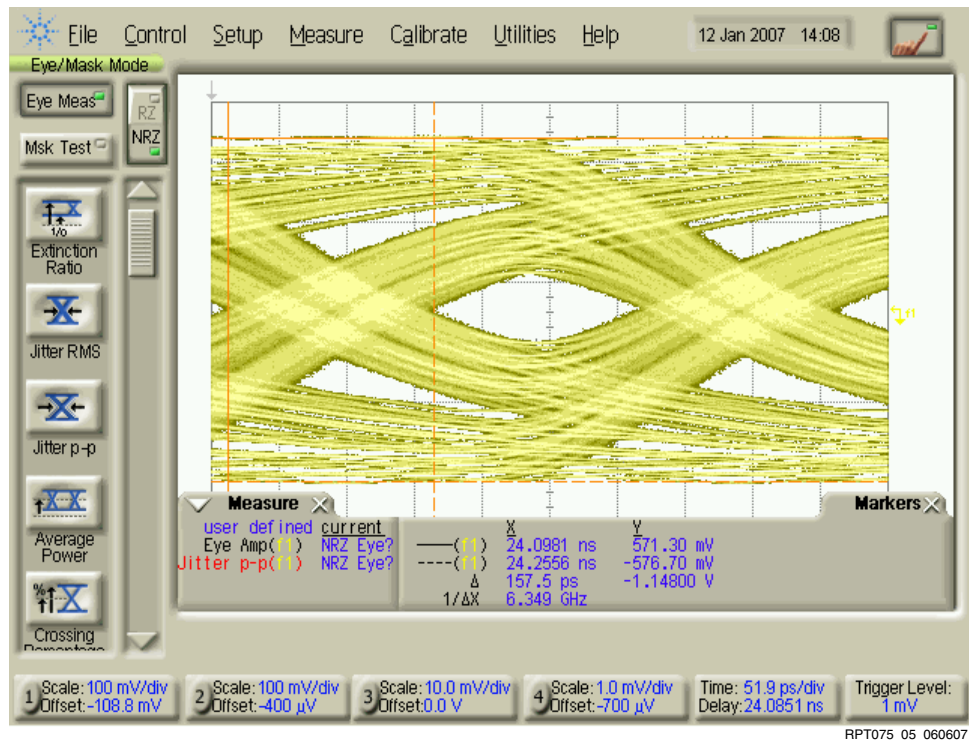Figure 5: **Near-End Eye Diagram at Virtex-4 Transceiver (DUT B) TX Output**

Figure 6: **Far-End Eye Diagram at Virtex-5 Transceiver (DUT A) RX Input (40 In. FR4)**

Conclusion

The test results (Table 6) were measured as observed on the receive counters of the Virtex-5 transceiver board (DUT A).

Table 6: **Bit Error Ratio Test Results**

Parameter	Value
Test Time	15 min
Received Bits	1.60E+012
Error Bits	0.00E+000
Calculated BER (assuming 1 bit in error)	0.63E–012