Virtex-6 FPGA GTX Transceiver XAUI Protocol

Characterization Summary Report

RPT124 (v1.0) November 3, 2010

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/03/10	1.0	Initial Xilinx release.

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Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report

Introduction

This protocol characterization summary report compares the electrical performance of the Virtex®-6 FPGA GTX transceiver against the 10 Gb Attachment Unit Interface (XAUI) specifications. Unless otherwise noted, the data presented in this report is extracted from the volume generic transceiver characterization across process, voltage, and temperature. The transmitter and receiver electrical characteristics are measured using a combination of lab bench setups and a high volume characterization (HVC) system. The methods used to characterize the transceiver are based on the standard specifications and also follow the best-practice methods for some parameters.

These test results are included in this report:

Test Conditions

Table 1 and Table 2 indicate the supply voltage and temperature conditions, respectively.

Table 1: **Supply Voltage Test Conditions**

Condition	MGTAVTT (V)	MGTAVCC (V)
V_{MIN}	Note(1)	1.14
V_{MAX}	Note(1)	1.26

Notes:

1. Depends on speed grade and PLL frequency. Refer to DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*, for the MGTAVCC values.

Table 2: **Temperature Test Conditions**

Condition	Temperature (°C)
T_{-40}	–40
T_{100}	100

Summary of Results

Table 3 indicates the tested Virtex-6 FPGA GTX transceiver performance results against the IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements (IEEE Std 802.3-2008), clause 47 specifications. The data reported in this table represents the values obtained under the worst-case voltage, temperature, and performance corner conditions.

Table 3: **Characterization Summary of Results**

Test	Parameter	Specification	Worst-Case Test Result	Units	Compatible
Transmitter Deterministic Jitter	DJ	0.17	0.15	UI	Yes
Transmitter Total Jitter	TJ	0.35	0.26	UI	Yes
Transmitter Output Differential Amplitude(1)	Min	800	Programmable(2)	mV	Yes
	Max	1600	Programmable(2)	mV	Yes
Transmitter Output Rise Time(1)	Min	60	115.1	ps	Yes
	Max	130	131.3		Note(3)
Transmitter Output Fall Time(1)	Min	60	122.5	ps	Yes
	Max	130	137.3		Note(3)
Transmitter Differential Output Return Loss	Frequency Profile	See Figure 4, page 13		dB	Yes
Transmitter Common Mode Output Return Loss	Frequency Profile	See Figure 5, page 14		dB	Yes
Receiver Deterministic Jitter	DJ	0.37	0.464	UI	Yes
Receiver Sinusoidal Jitter	SJ	0.1	0.219	UI	Yes

Table 3: **Characterization Summary of Results *(Cont'd)***

Test	Parameter	Specification	Worst-Case Test Result	Units	Compatible
Receiver Total Input Jitter Tolerance	TJ	0.65	0.864	UI	Yes
Receiver Differential Input Return Loss	Frequency Profile	See Figure 8, page 18		dB	Yes
Receiver Common Mode Input Loss	Frequency Profile	See Figure 9, page 18		dB	Yes

Notes:

1. These tests are performed at 2.5 Gb/s with a clock pattern of five `1`s and five `0`s (...`11000001111100`...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of UG366, *Virtex-6 FPGA GTX Transceivers User Guide*.
3. Measurement is taken with approximately 4.5 inches of channel between the TXP/TXN FPGA device pins and the SMA connectors on the ML623 Virtex-6 FPGA GTX Transceiver Characterization Board. De-embedding the channel effect shows approximately 20 to 30 ps improvement in the rise time and fall time measurements.

Electrical Characterization Details

This section describes the test methodology and test results for each test summarized in Table 3. The GTX transceiver is configured using the Virtex-6 FPGA GTX Transceiver Wizard, v1.6. GTX transceiver attribute settings that differ from the Wizard default settings are identified in the "Test Setup and Conditions" table for each test. Table 4 indicates the PLL settings used in the characterization.

Table 4: **3.125 Gb/s Line Rate PLL Settings**

Data Rate (Gb/s)	PLL Frequency (GHz)	REFCLK Frequency (MHz)	TXPLL_DIVSEL_REF/ RXPLL_DIVSEL_REF	TXPLL_DIVSEL45_FB/ RXPLL_DIVSEL45_FB* TXPLL_DIVSEL_FB/ RXPLL_DIVSEL_FB	PLL_TXDIVSEL_OUT/ PLL_RXDIVSEL_OUT
3.125	1.5625	156.25	1	5 x 2 = 10	1

Transmitter Near-End Output Eye

Test Methodology

The device is configured to transmit a PRBS7 pattern on each of the TX data pins, and the resulting eye is captured using an Agilent 86100C Infiniium DCA-J wideband oscilloscope for 1000 samples at nominal voltage and room temperature conditions. The test setup and conditions are defined in Table 5.

Table 5: **Transmitter Near-End Output Eye Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope with an Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	Nominal
Temperature	Room temperature

Table 5: **Transmitter Near-End Output Eye Test Setup and Conditions *(Cont'd)***

Parameter	Value
Pattern	PRBS7
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)(1)
TX Amplitude	Maximum amplitude, TXDIFFCTRL = `4'b1111`
REFCLK	156.25 MHz sourced from an Agilent 81133A pulse generator

Notes:

1. Refer to UG724, *ML623 Virtex-6 FPGA GTX Transceiver Characterization Board User Guide*, for additional information on the ML623 board.

Test Results

Figure 1 shows the transmitter near-end output eye at 3.125 Gb/s. Figure 1 is provided as a representative diagram, and does not quantify device performance.

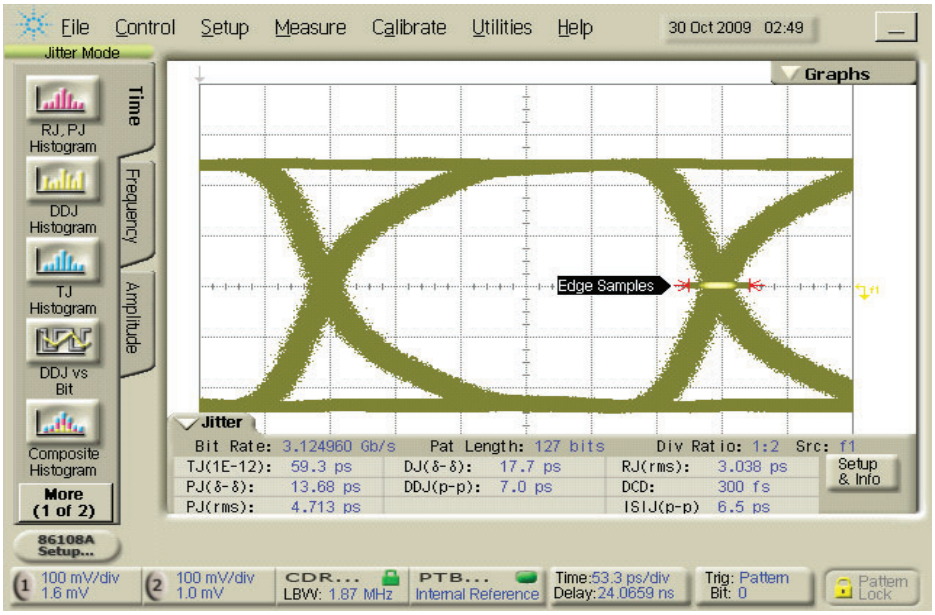

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Figure 1: **Transmitter Near-End Output Eye (3.125 Gb/s with a 156.25 MHz REFCLK)**

Transmitter Output Jitter

Test Methodology

TX jitter data is collected using the HVC system. Data for 12 serial transceiver channels is collected simultaneously. The primary instrument used to collect the data is an Agilent Parallel BERT (ParBERT) analyzer. This instrument determines the BER at various sample points across the TX eye. The data is analyzed in the ParBERT analyzer, and the resulting TJ, DJ, and RJ are reported back to the controlling test program. The test setup and conditions are defined in Table 6.

Table 6: **Transmitter Output Jitter Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HVC ParBERT Analyzer
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_{100}
Pattern	PRBS7
BER	10^{-12}
Load Board	Custom HVC Test Fixture (FF1156)
TX Amplitude/Post Emphasis	GTX transceiver attributes: • TXDIFFCTRL = `4'b1111` • TXBUFDIFFCTRL = `3'b100` • TXPREEMPHASIS = `4'b0000` • TXPOSTEMPHASIS = `5'b00000`
REFCLK	160 MHz sourced from an Agilent ParBERT E4862B module

Test Results

Figure 2 shows the output jitter test results with a PRBS7 pattern (BER of 10^{-12}) at 3.2 Gb/s. A PRBS7 data pattern is used for the output jitter measurements instead of the required CJPAT test patterns. The transmitter behavior is similar for PRBS7 and CJPAT. The measured output jitter was not filtered, and represents a pessimistic broadband jitter.

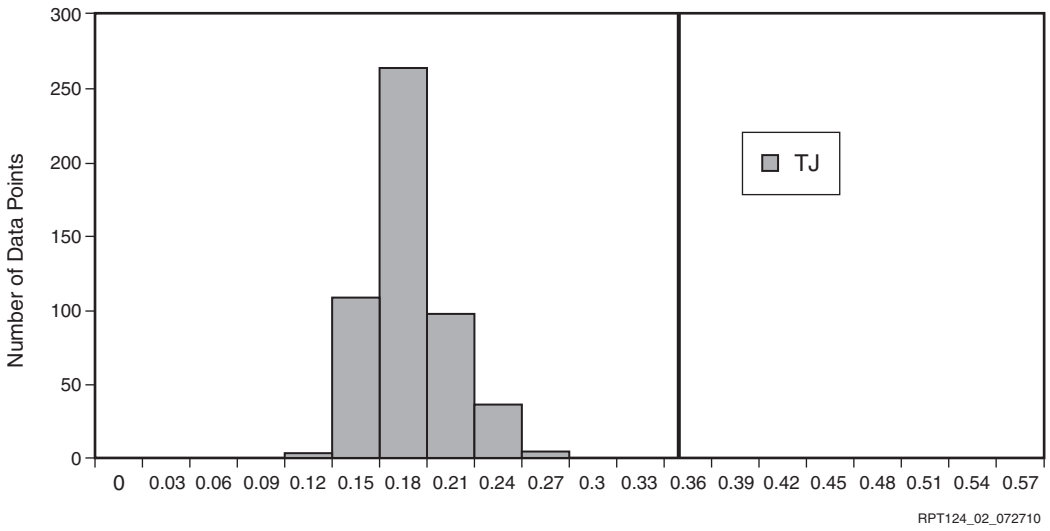

Figure 2: **Transmitter Output Jitter Test Results Targeted for 3.125 Gb/s**

Table 7 indicates the maximum transmitter output jitter test result at a 3.2 Gb/s line rate with a 160 MHz reference clock, a PRBS7 pattern, and a BER of 10^{-12}.

Table 7: **Transmitter Output Jitter Test Results Targeted for 3.125 Gb/s**

Parameter	Pattern	BER	TJ (UI)	DJ (UI)	RJ (UI)
Maximum Transmitter Output Jitter	PRBS7	10^{-12}	0.26	0.15	0.23

Transmitter Output Differential Amplitude

Test Methodology

The IEEE Std 802.3-2008 (clause 47) specification defines the transmitter differential amplitude as:

Output amplitude = 800 to 1600 mV

The transmitter output differential amplitudes are measured using the transmitter characterization bench setup as specified in RPT120, *Virtex-6 FPGA GTX Transceiver Characterization Report*. Data is measured at a TX data rate of 2.5 Gb/s with a clock pattern of five `1`s and five `0`s. This is a typical representation of GTX transceiver behavior at 3.125 Gb/s. The test setup and conditions are defined in Table 8.

Table 8: **Transmitter Output Differential Amplitude Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_{100}
Pattern	A clock pattern of five `1`s and five `0`s (...`11000001111100`...) generated internally in the FPGA logic
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
TX Amplitude/Post Emphasis	GTX transceiver attributes: • TXDIFFCTRL = `4'b1111` • TXBUFDIFFCTRL = `3'b100` • TXPREEMPHASIS = `4'b0000` • TXPOSTEMPHASIS = `5'b00000`
REFCLK	125 MHz sourced from Agilent 8133A pulse generator

Test Results

The transmitter output differential amplitude test results are indicated in Table 9.

Table 9: **Transmitter Output Differential Amplitude Test Results**

Parameter	Min	Max	Units
Output differential amplitude (TXDIFFCTRL = `4'b1111`)	1003	1250	mV

Transmitter Output Rise and Fall Times

Test Methodology

The IEEE Std 802.3-2008 (clause 47) specification defines the transmitter rise and fall times as:

Output rise and fall time = 60 to 130 ps

The transmitter output rise and fall times are measured using the transmitter characterization bench setup as specified in RPT120, *Virtex-6 FPGA GTX Transceiver Characterization Report*. Because of board limitations, the measurement is taken with approximately 4.5 inches of channel length between the TXP/TXN FPGA pins and the SMA connectors on the ML623 board.

De-embedding the channel effect shows approximately 20 to 30 ps improvement in the rise time and fall time measurements. Data is measured at a TX data rate of 2.5 Gb/s with a clock pattern of five `1`s and five `0`s. This is a typical representation of GTX transceiver behavior at 3.125 Gb/s. The test setup and conditions are defined in Table 10.

Table 10: **Transmitter Output Rise and Fall Times Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_{100}
Pattern	A clock pattern of five `1`s and five `0`s (...`11000001111100`...) generated internally in the FPGA logic
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
TX Amplitude/Post Emphasis	GTX transceiver attributes: • TXDIFFCTRL = `4'b1111` • TXBUFDIFFCTRL = `3'b100` • TXPREEMPHASIS = `4'b0000` • TXPOSTEMPHASIS = `5'b00000`
REFCLK	125 MHz sourced from Agilent 8133A pulse generator

Test Results

The transmitter output rise and fall time test results are indicated in Table 11 and Table 12, respectively.

Table 11: **Transmitter Output Rise Time Test Results**

Parameter	Min	Max	Units
Output Rise Time (TXDIFFCTRL = `4'b1111`)	115.1	131.3	ps

Table 12: **Transmitter Output Fall Time Test Results**

Parameter	Min	Max	Units
Output Fall Time (TXDIFFCTRL = `4'b1111`)	122.5	137.3	ps

Transmitter Differential and Common Mode Output Return Loss

Test Methodology

The setup for the return loss measurement is shown in Figure 3. For frequencies from 312.5 MHz to 3.125 GHz, the differential return loss of the driver must exceed the limits shown in Figure 4. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

The Vector Network Analyzer (VNA) interfaces to the host PC through the general purpose interface bus (GPIB). After the measurement parameters are set, calibration begins. Four cables are included in the calibration process. VNA measurements are independent of voltage and are accurate up to 11 GHz. A digital voltmeter (DVM) confirms that the differential resistance is 100Ωbefore the measurement. The test setup and conditions are defined in Table 13.

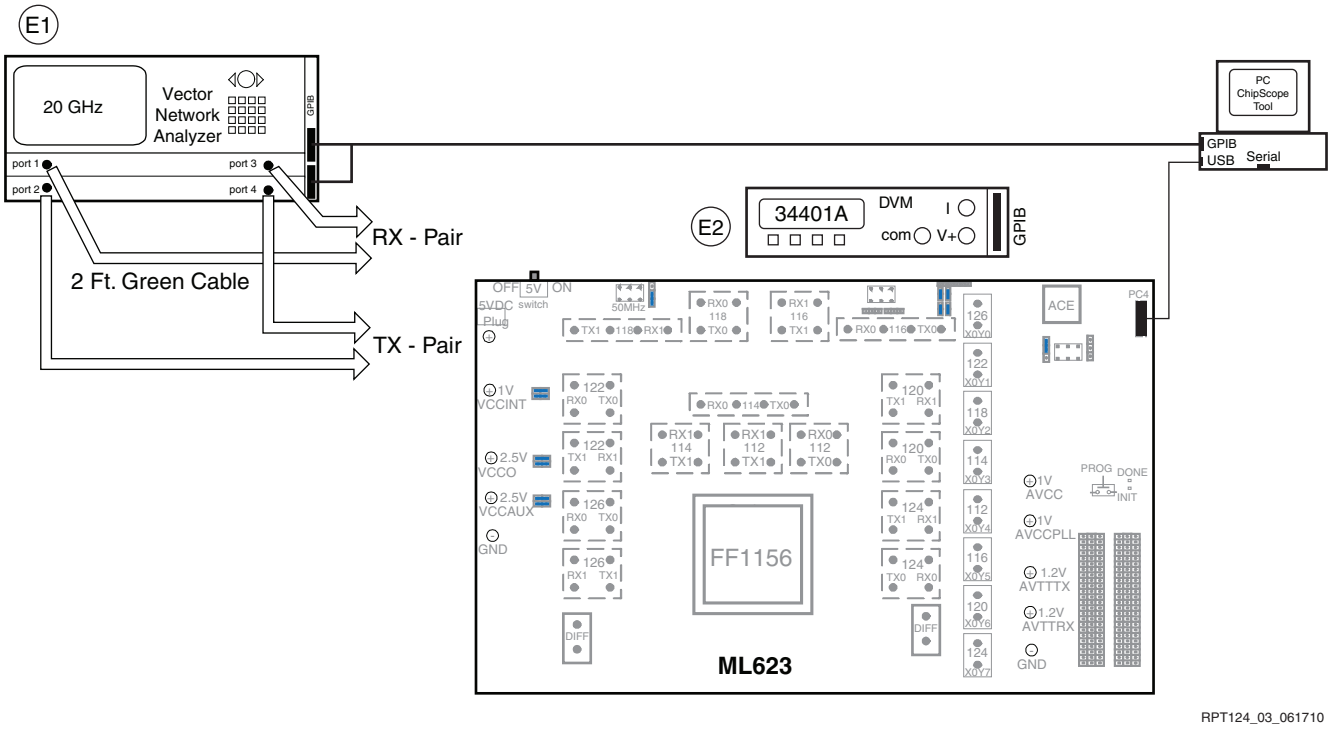

Figure 3: **Return Loss Test Setup Diagram**

Table 13: **Transmitter Differential and Common Mode Output Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES Vector Network Analyzer
TX Coupling	AC coupled using DC blocks
Voltage	Typical voltage
Temperature	Room temperature

Table 13: **Transmitter Differential and Common Mode Output Return Loss Test Setup and Conditions *(Cont'd)***

Parameter	Value
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency	100 Hz

Test Results

Figure 4 shows the transmitter differential output return loss measurement.

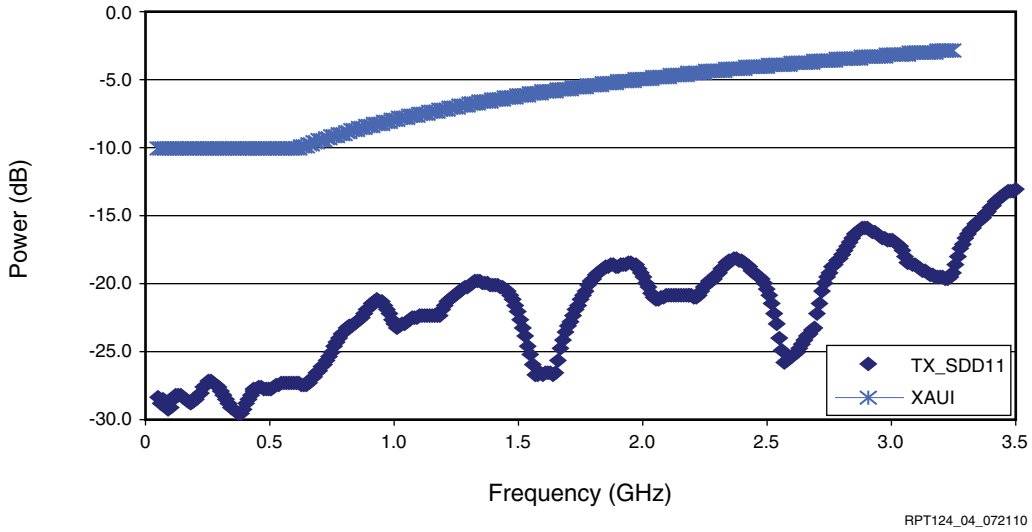

Figure 4: **Transmitter Differential Output Return Loss Measurement**

Figure 5 shows the transmitter common mode output return loss measurement.

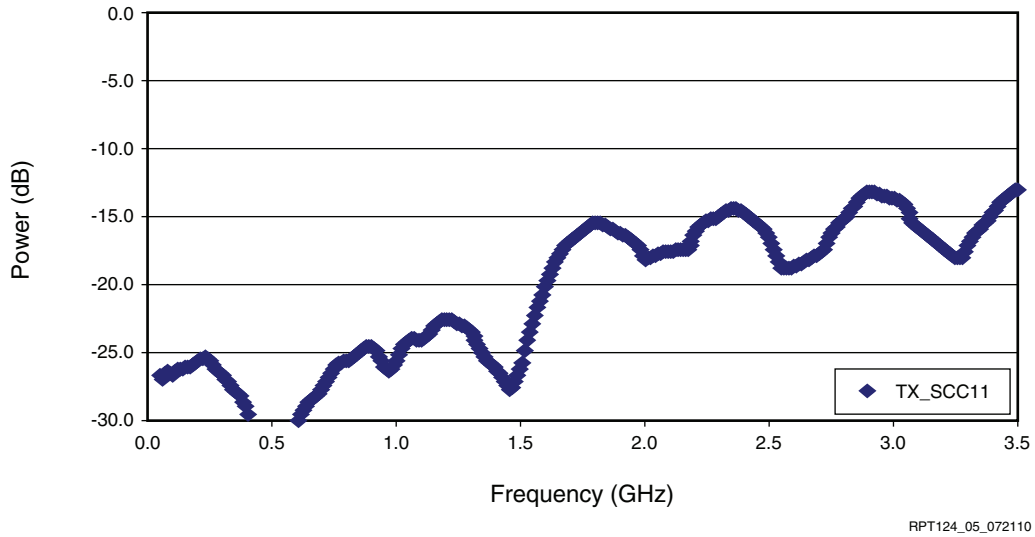

Figure 5: **Transmitter Common Mode Output Return Loss Measurement (Informative)**

Receiver Input Jitter Tolerance

Test Methodology

The setup for the receiver jitter tolerance measurement is shown in Figure 6. Medium and worst performance transceivers are used for the measurements. The Agilent N4903B J-BERT generates a CJPAT pattern with random jitter (RJ) and deterministic jitter (DJ) designated by the IEEE Std 802.3-2008 (clause 47) specification. DJ in the form of intersymbol interference (ISI) and bounded uncorrelated jitter (BUJ) are added with the Agilent built-in features. ISI is added by using the Agilent J-BERT interference channel feature (option J20) by selecting the 24 inches of board trace (Nelco 4000-6). Sinusoidal jitter (SJ) is swept from 1 KHz to 80 MHz. The GTX transceiver under test recovers the data and transmits the pattern back to the Error Detector input of the J-BERT, where bit errors are measured. The test is performed with a +200 and –200 ppm offset between the J-BERT data generator and the reference clock provided to the GTX transceiver under test. The test setup and conditions are defined in Table 14.

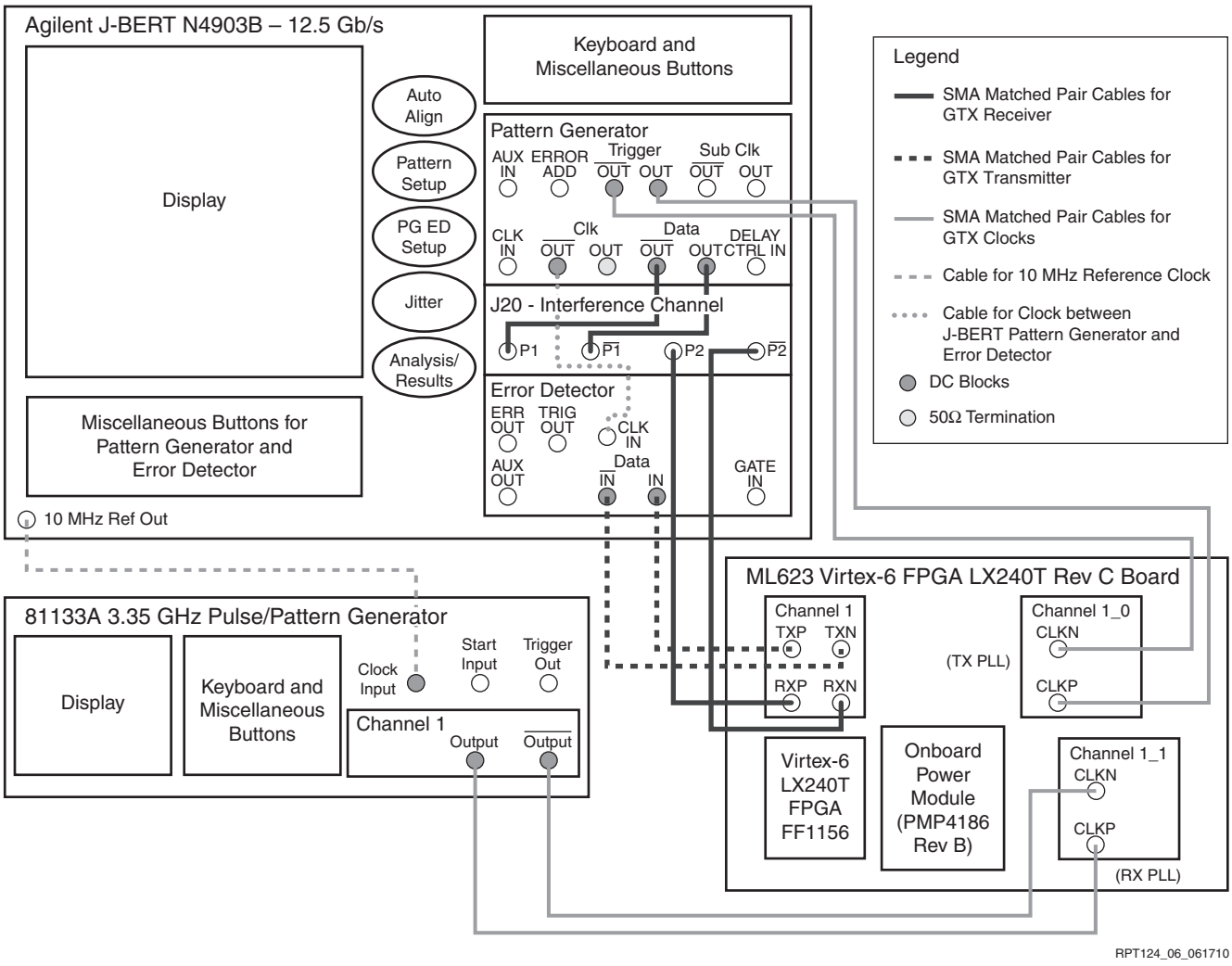

Figure 6: **Receiver Jitter Tolerance Setup Diagram**

Table 14: **Transmitter Differential and Common Mode Output Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent N4903B J-BERT
RX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_{100}
Pattern	CJPAT
Injected Jitter	Sum of: • RJ = 0.1806 UI_{P-P} • DJ = 0.2740 UI_{P-P} (24 inches of interference channel) • BUJ = 0.1900 UI_{P-P} • SJ = Tested to failure; Frequency sweep = {1 KHz — 80 MHz}

Table 14: **Transmitter Differential and Common Mode Output Return Loss Test Setup and Conditions *(Cont'd)***

Parameter	Value
BER	10^{-12} (measured at 10^{-9}, extrapolated to 10^{-12})
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)

Attributes	GTX transceiver attributes:
	• PMA_RX_CFG = `25'h05ce049`
	• RXEQMIX = `3'b110`
	• DFE Disabled
	  • DFETAP1[4:0] = `5'b00000`
	  • DFETAP2[4:0] = `5'b00000`
	  • DFETAP3[4:0] = `5'b00000`
	  • DFETAP4[4:0] = `5'b00000`

REFCLK	• 156.25 MHz sourced from the J-BERT • 156.25 MHz ± 200 ppm offset from the Agilent 81133A pulse generator

Test Results

Figure 7 shows the receiver jitter tolerance SJ sweep for the receiver jitter tolerance test. SJ is applied in addition to RJ, BUJ, and DJ, as defined in Table 14. The minimum total receiver jitter tolerance performance is indicated in Table 14.

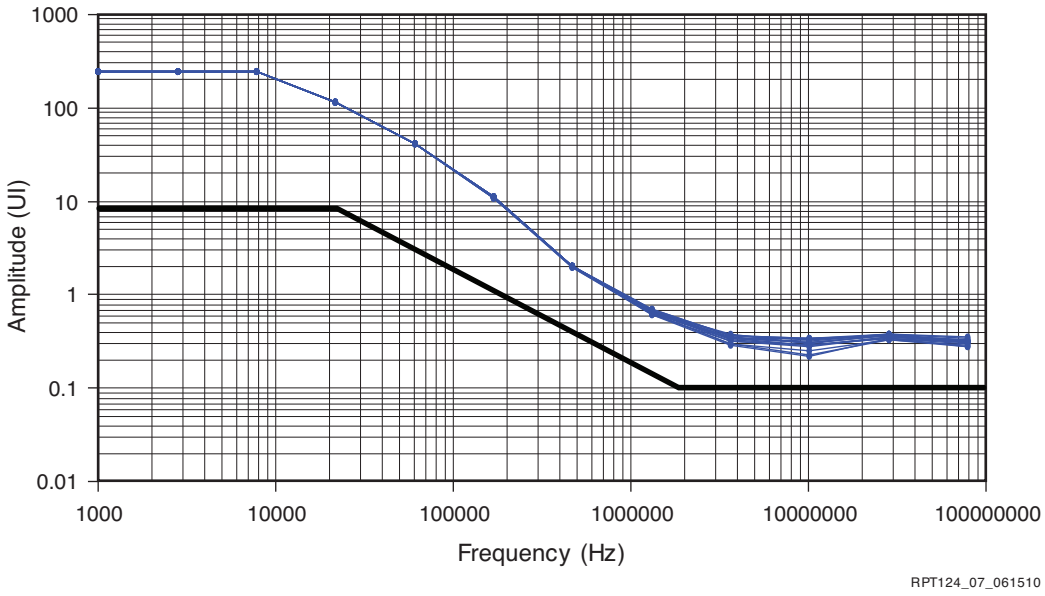

Figure 7: **Receiver Jitter Tolerance SJ Sweep Test Results (CJPAT, BER = 10^{-12})**

Table 15: **Receiver Jitter Tolerance Test Results**

Jitter Tolerance Parameter	BER	Minimum Tolerance	Units
SJ at 10.3 MHz	10^{-12}	0.219	UI
TJ	10^{-12}	0.864	UI

Receiver Differential and Common Mode Input Return Loss

Test Methodology

The receiver input should have a differential return loss better than 10 dB, and a common mode return loss better than 6 dB from 100 MHz to 2.5 GHz. This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100Ω for differential return loss and 25Ω for common mode return loss. The test setup and conditions are defined in Table 16.

Table 16: **Receiver Differential and Common Mode Input Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES Vector Network Analyzer
RX Configuration/ Amplitude	RX is configured for 100Ω differential termination (center tap to GND), and AC coupled using both internal and external capacitors: • RCV_TERM_VTTRX = FALSE • RCV_TERM_GND = TRUE • AC_CAP_DIS = FALSE
Voltage	Typical voltage
Temperature	Room temperature
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency	100 Hz

Test Results

Figure 8 shows the receiver differential input return loss measurement.

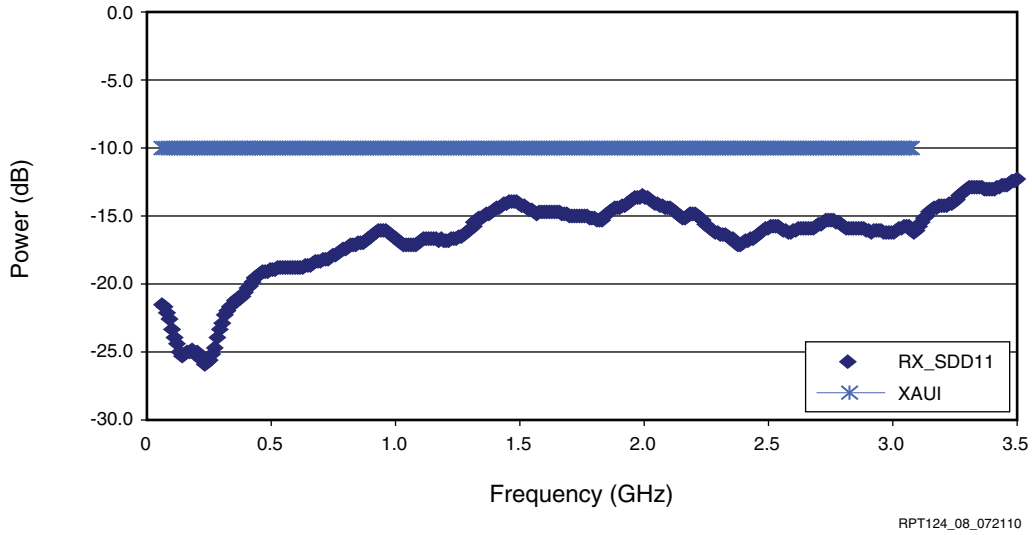

Figure 8: **Receiver Differential Input Return Loss Measurements**

Figure 9 shows the receiver common mode input return loss measurement.

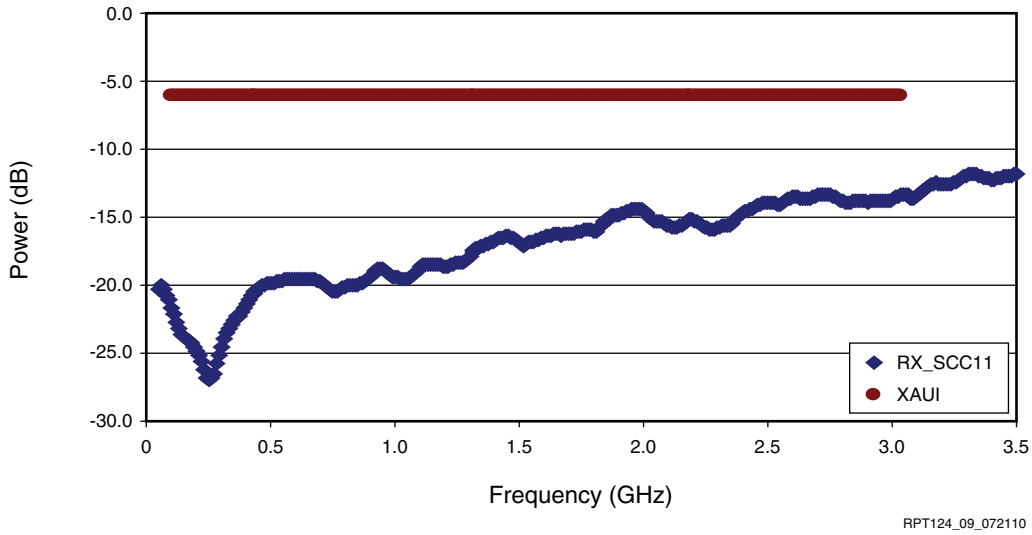

Figure 9: **Receiver Common Mode Input Return Loss Measurements**