Spartan-3AN XC3S1400AN FPGA Errata for Engineering Samples

EN034 (v1.3) August 31, 2007 **Errata Notice**

Introduction

Thank you for your interest in the Xilinx Spartan™-3AN family XC3S1400AN FPGA device engineering samples. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in this errata notification. These errata do not apply to the XC3S1400AN production FPGAs.

Device Identification

These errata apply to the XC3S1400AN engineering samples as shown in Table 1. See the top-mark in Figure 1.

Table 1: **XC3S1400AN Devices Affected by These Errata**

Device Types	XC3S1400AN
Packages	All
Speed Grades	-4
Date Codes	All
Marked as "ES"	Yes

Traceability

XC3S1400AN engineering samples are marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

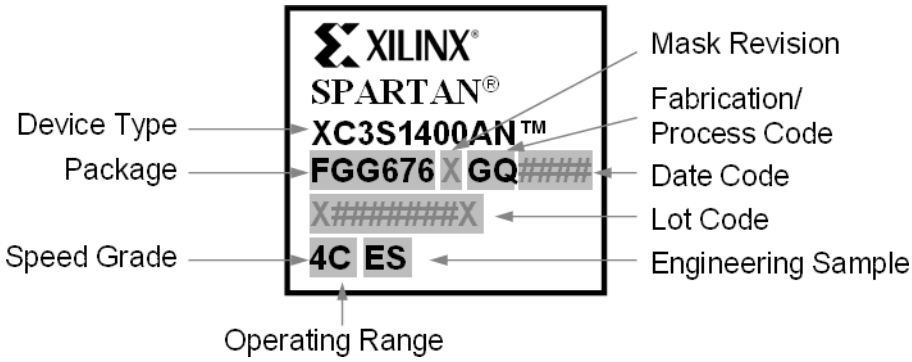

Figure 1: **XC3S1400AN FPGA Top Marking**

Hardware Errata Summary

Table 2 summarizes the known hardware issues with the XC3S1400AN engineering samples. See Hardware Errata for a detailed description of each known issue. Table 2 also shows which mask revision is affected by a particular errata item.

Table 2: **Hardware Errata Summary**

Errata Issue	Severity	Engineering Samples	Production Devices
"ICAP Commands including MultiBoot Unavailable after Configuration from In-System Flash"	Major	Applies	Fixed
"PCI Clamp Diode Unavailable"	Minor	Applies	Fixed
"Potential Data Slip Issue with ODDR2 Output Flip-Flop Using C0 Alignment"	Minor	Applies	Fixed
"Block RAM Readback Feature Unavailable"	Minor	Applies	Fixed
"QuietIO Current-Voltage Behavior is Non-monotonic at Low Voltage and Low Current"	Minor	Applies	Fixed
"In-System Flash May Be Pre-Programmed"	Minor	Applies	Fixed (Blank)

Hardware Errata

This section provides a detailed description of each known hardware issue.

ICAP Commands including MultiBoot Unavailable after Configuration from In-System Flash

Applications affected

This issue affects applications that use the In-System Flash for configuration and then use the ICAP_SPARTAN3A component for commands such as MultiBoot or readback. Applications that configure from external memory are not affected.

Description

After configuration from the In-System Flash, the ICAP_SPARTAN3A component is not available. The MultiBoot feature uses the REBOOT command on the ICAP_SPARTAN3A component. A MultiBoot request will be ignored and the current design will continue to function. The MultiBoot feature is only available after configuration from an external source, such as external SPI or Platform Flash memories.

In addition to MultiBoot, readback and access to command registers is not available through ICAP_SPARTAN3A after configuration through the In-System Flash.

Workaround

The ICAP commands for MultiBoot and readback are available after configuration from external memory. A Spartan-3AN In-System Flash MultiBoot application can be prototyped with a Spartan-3A or Spartan-3AN FPGA and external SPI Flash memory.

This issue has been corrected in production revisions of the XC3S1400AN silicon.

PCI Clamp Diode Unavailable

Applications affected

This issue only affects PCI bus and card applications that require full compliance to the PCI bus standard. It has little to no effect on point-to-point PCI solutions, such as chip-to-chip communication on the same board. The XC3S1400AN samples are still useful for PCI bus card development but must not be used for PCI bus production designs until this issue is corrected.

Description

The PCI clamp diode shunts the potentially large overshoot voltage possibly generated in a PCI bus plug-in card application, which protects the FPGA I/O circuitry. The PCI clamp diode feature is not available on the XC3S1400AN engineering samples.

Workaround

This issue has been corrected in production revisions of the XC3S1400AN silicon.

Potential Data Slip Issue with ODDR2 Output Flip-Flop Using C0 Alignment

Applications affected

The ODDR2 output flip-flop primitive is typically used in high-speed differential I/O applications, such as LVDS and RSDS interfaces. This only affects applications using DDR_ALIGNMENT=C0 or C1. The default ODDR2 flip-flop without the alignment feature remains fully supported, and the IDDR2 alignment feature is supported.

Description

Data slip has been observed under certain BUFG placement situations.

Workaround

It is possible to use an alternate implementation inside the FPGA fabric using logic slice functions and careful placement between the slice flip-flop and adjacent I/O block. For details, see Answer 24478.

This issue has been corrected in production revisions of the XC3S1400AN silicon.

Block RAM Readback Feature Unavailable

Applications affected

This issue only affects the rare application that might use the Readback feature to read block RAM contents.

Description

Reading back block RAM contents is not available in the engineering samples. This issue does not affect the iMPACT Verify operation or ChipScope™ operations.

Workaround

This issue has been corrected in production revisions of the XC3S1400AN silicon.

QuietIO Current-Voltage Behavior is Non-monotonic at Low Voltage and Low Current

Applications affected

This issue only affects applications that use the QUIETIO slew rate for the I/O standards listed below.

- IOSTANDARDs LVTTL, LVCMOS33, and LVCMOS25
- SLEW=QUIETIO
- DRIVE=2

Description

The non-monoticity at low voltage and low drive current can potentially cause issues in applications that expect higher output currents at logic High output levels.

Workaround

For the affected I/O standards, increase the drive current to 4 mA or larger.

This issue has been corrected in production revisions of the XC3S1400AN silicon.

In-System Flash May Be Pre-Programmed

Applications affected

This issue affects applications that use the FPGA before programming the In-System Flash. Applications that erase or program the In-System Flash before use on a board are not affected.

Description

The In-System Flash memory is pre-programmed as part of Xilinx testing. Engineering Samples may be shipped with this design instead of a blank device. If the Mode pins are set to configure from the In-System Flash, then the pre-programmed design will be used to configure the FPGA at power-up. The design uses the default configuration options, including pull-down resistors on unused pins. The design uses no I/O pins. The DONE pin will be driven High, and the I/O pins will have internal pull-down resistors.

Workaround

XC3S1400AN engineering sample devices should have the In-System Flash programmed with the user application, or erased, before use on a board. Alternatively, set the Mode pins to any configuration mode other than ISF so that the FPGA does not configure with the pre-programmed pattern. If the FPGA is configured with the pre-programmed pattern, make sure the internal pull-downs are acceptable on the PC board. Where necessary, add external pull-ups that are strong enough to overcome the internal pull-down value shown in the data sheet.

This issue has been corrected in production revisions of the XC3S1400AN silicon. All production devices are shipped blank.

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For questions about these errata, please contact Xilinx Technical Support http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx sales representative, http://www.xilinx.com/company/contact.htm.

Obtaining Errata Notification Updates

If this document is printed or saved locally, please check for the most recent release, available to registered users on the Xilinx web site at http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata. To receive an e-mail alert when this document changes, sign up at http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

Applicable Documents

These errata apply to the following XC3S1400AN documents:

- **DS557: Spartan-3AN FPGA Family Data Sheet**
  www.xilinx.com/bvdocs/publications/ds557.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/bvdocs/userguides/ug331.pdf
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/bvdocs/userguides/ug332.pdf
- **UG333: Spartan-3AN In-System Flash User Guide**
  www.xilinx.com/bvdocs/userguides/ug333.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Description
03/16/07	1.0	Initial release
05/21/07	1.1	Added “ICAP Commands including MultiBoot Unavailable after Configuration from In-System Flash”
06/25/07	1.2	Added “In-System Flash May Be Pre-Programmed”
08/31/07	1.3	Updated to note that all errata are fixed in production silicon