Introduction

Although Xilinx has made every effort to ensure the highest possible quality, these Virtex™-5 engineering samples (ES) are subject to the limitations described in the following errata.

Devices

These errata apply to the Virtex-5 devices, as shown in Table 1.

Table 1: **Virtex-5 Devices Affected by These Errata**

Devices	XC5VLX30CES	JTAG ID (Revision Code): 2, 3, 4, 5
	XC5VLX50CES	JTAG ID (Revision Code): 2, 3, 4, 5
	XC5VLX85CES	JTAG ID (Revision Code): 2, 4
	XC5VLX110CES	JTAG ID (Revision Code): 2, 4
	XC5VLX220CES	JTAG ID (Revision Code): 0,1
	XC5VLX330CES	JTAG ID (Revision Code): 0,1
Packages	All	
Speed Grades	-1 , -2	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Block RAM

Block RAM Synchronous FIFO Mode - LX30, LX50, LX85, and LX110

F_{MAX_FIFO} is 400 MHz when using the attribute EN_SYN = TRUE.

Block RAM ECC Scrub Mode

ECC Scrub mode (EN_ECC_SCRUB = TRUE) is not supported and will not be supported in production devices.

OSERDES

Optional inversion for the divided clock (CLKDIV) in the OSERDES is not supported.

Configuration

When reconfiguring with a different bitstream on an already configured device, in rare cases a static LUT input can be inverted. For more information see answer record 24582.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.41 (or later) and Xilinx software ISE 8.2i (or later) is required when designing for the devices covered by this errata.

- The stepping should be set to "ES" in the constraint file (UCF file):

  CONFIG STEPPING = "ES";

- A summary list of ISE software known issues pertaining to the Virtex-5 features is available at:

  http://www.xilinx.com/xlnx/xil_ans_display.jsp?iCountryID=1&iLanguageID=1&getPagePath=23625

Notes and Recommendations

V_{BATT} ESD Protection

The V_{BATT} pin ESD protection meets HBM 500V.

Power Supply Requirements - LX30, LX50, LX85, and LX110

During power-up and configuration across commercial temperature ranges, the V_{CCINT} supply requires a maximum current I_{CCINT} for the devices shown in Table 2.

Table 2: **V_{CCINT} Power Supply Maximum Current Requirements - LX30, LX50, LX85, and LX110**

Device	V_{CCINT}	I_{CCINT}
XC5VLX30CES	1.05V	2.5A
XC5VLX50CES	1.05V	2.75A
XC5VLX85CES	1.05V	3.75A
XC5VLX110CES	1.05V	4.0A

Traceability

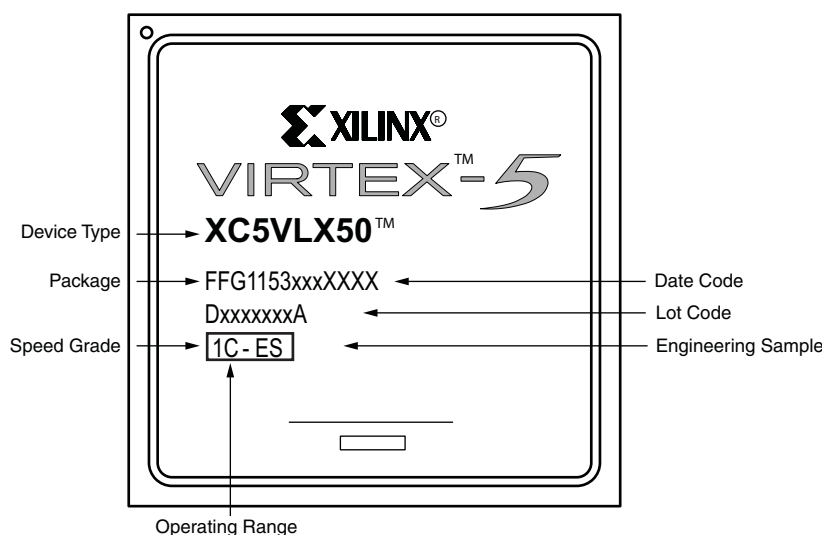The XC5VLX50CES is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

EN049_01_121806

Figure 1: **Example XC5VLX50CES Package Marking**

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Additional Questions or Clarifications

All other device functionality and timing meet the current data sheet specifications.

For additional questions regarding these errata, contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at:

http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-5 documents:

Virtex-5 Overview (http://www.xilinx.com/bvdocs/publications/ds100.pdf)

Virtex-5 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds202.pdf)

Virtex-5 User Guide (http://www.xilinx.com/bvdocs/userguides/ug190.pdf)

Virtex-5 XtremeDSP™ Design Considerations (http://www.xilinx.com/bvdocs/userguides/ug193.pdf)

Virtex-5 Configuration Guide (http://www.xilinx.com/bvdocs/userguides/ug191.pdf)

Virtex-5 Packaging and Pinout Specifications (http://www.xilinx.com/bvdocs/userguides/ug195.pdf)

Revision History

Date	Version	Description
03/31/06	1.0	Initial Xilinx release.
05/12/06	1.1	Added devices to document, including Table 1. Minor edits to the document structure including added information under Additional Questions or Clarifications. Removed BUFGMUX errata. Added Table 2 and updated XC5VLX50CES maximum current.
05/26/06	1.2	Minor typographical edits. Revised I_{CCINIT} for the XC5VLX50CES in Table 2 from 2.6A to 2.75A. Added CONFIG STEPPING = ES requirement to Design Software Requirements.
08/04/06	1.3	Added Block RAM Synchronous FIFO Mode - LX30, LX50, LX85, and LX110 errata. Added link to ISE software known issues in the Design Software Requirements section.
12/27/06	1.4	Revised JTAG ID codes in Table 1. Some errata removed with the removal of JTAG ID 0 and 1. Revised Power Supply Requirements - LX30, LX50, LX85, and LX110, page 2. Updated Figure 1. Added Block RAM ECC Scrub Mode errata.
04/03/07	1.5	Added XC5VLX220CES and XC5VLX330CES devices. Added device-specific text to the Block RAM and Power Supply Requirements - LX30, LX50, LX85, and LX110 sections. Added Configuration errata.
05/11/07	1.6	Added OSERDES errata. Updated Block RAM ECC Scrub Mode section.