Virtex-5 Errata: XC5VSX35TCES and XC5VSX50TCES

EN052 (v1.3) May 14, 2008 **Errata Notification**

Introduction

Although Xilinx has made every effort to ensure the highest possible quality, these Virtex™-5 engineering samples (ES) are subject to the limitations described in the following errata.

Devices

These errata apply to the Virtex-5 devices, as shown in Table 1.

Table 1: **Virtex-5 Devices Affected by These Errata**

Devices	XC5VSX35TCES	JTAG ID (Revision Code): 1, 3
	XC5VSX50TCES	JTAG ID (Revision Code): 1, 3
Packages	All	
Speed Grades	-1, -2	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Block RAM ECC Scrub Mode

ECC Scrub mode (EN_ECC_SCRUB = TRUE) is not supported and will not be supported in production devices.

Configuration

When reconfiguring with a different bitstream on an already configured device, in rare cases a static LUT input can be inverted. For more information see answer record 24582.

Integrated Endpoint Block for PCI Express

Configuration Space

The version field of the Power Management capability is incorrectly set to `010b`, however, the functionality is not affected.

Error Reporting

Error Signaling Message Transaction Layer Packets are incorrectly sent for Ignored Messages, Unsupported Requests, and Poisoned TLPs.

Transaction Layer Interface

Gaps in user request receive data destination (LLKRXDSTREQN) cannot be longer than four cycles, unless the gaps are between packets.

Workaround

Prevent gaps in LLKRXDSTREQN of longer than four cycles. Users of the LogiCORE™ Endpoint Block Plus for PCI Express (v1.1) are not affected by this errata. Users of the LogiCORE Endpoint Block for PCI Express (v1.1 or later) must implement this work around.

LLKRXDSTREQN must be deasserted in the same cycle that LLKRXSRCLASTREQN is asserted.

Workaround

Deassert LLKRXDSTREQN in the same cycle that LLKRXSRCLASTREQN is asserted. The LogiCORE Endpoint Block Plus for PCI Express (v1.1) implements this workaround. This workaround is not incorporated in the LogiCORE Endpoint Block for PCI Express (v1.1 or later).

Transaction Ordering

The transaction ordering implemented by the Virtex-5 Integrated Endpoint block for PCI Express designs has the following differences from the PCI Express base specification, revision 1.1, Table 2-23.

- Completion packets can be blocked by non-posted packet requests.

  Workaround

  A user application waiting for a completion packet must drain the non-posted queue to ensure that the completion packet already in the RX buffer can be drained. In addition, if a far-end device is waiting for a completion packet, the far-end device must free up non-posted flow control credits before the Integrated Endpoint block will transmit a completion packet waiting in its TX buffer.

- Packets without flow control credits can sometimes be transmitted, when a link partner does not advertise infinite completion flow control credits and the endpoint is in an 8-lane configuration, causing flow control protocol errors.

  Workaround

  The user application must put posted packets in the transmit queue only if sufficient credits are available.

- Posted packets waiting for flow control credits in the transmit buffer can sometimes be passed by completion or non-posted packets. For example, a memory read packet could pass a memory write packet with overlapping addresses, resulting in incorrect data being read. After this violation occurs, transmission of completion packets and/or non-posted packets could be halted if the posted packet buffer becomes empty. Transmission of completion packets and/or non-posted packets in the buffer will resume once a new posted packet is transmitted

  Workaround

  The user application must put posted packets in the transmit queue only if sufficient credits are available.

GTP Transceivers

RX Buffer Bypass (RX Low Latency Mode)

The receiver buffer bypass mode is only supported for 10-bit internal data paths with a receiver PLL divider of 1. Receiver PLL divider settings of 2 or 4 are not currently supported.

Reference Clock Input Resistance

The differential input resistance R_{IN} of the RocketIO GTP reference clock ranges from 160Ω to 180Ω. The higher resistance should not affect the performance of the GTP transceiver.

AC JTAG

AC JTAG mode is not supported and will not be supported in production devices.

GTP CRC Parallel Interface Timing

For proper timing, the parallel CRCIN interface must be clocked off of an inverted CRCCLK and sourced from a register clocked on the noninverted CRCCLK in the CLB fabric. The CRC CORE Generator™ Wizard generates wrapper files that include this circuitry. See Answer Record #24879 for more details.

GTP Transmit Interface Timing

For proper timing, the transmit interface must be clocked off of an inverted TXUSRCLK2 and sourced from a register clocked on the noninverted TXUSRCLK2 in the CLB fabric. The GTP CORE Generator Wizard generates wrapper files that include this circuitry.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.51 (or later) and Xilinx software ISE 9.1i SP1 (or later) is required when designing for the devices covered by this errata.
- The stepping should be set to ES in the constraint file (UCF file):

  CONFIG STEPPING = “ES”;

- A summary list of ISE software known issues pertaining to the Virtex-5 features is available at:

  http://www.xilinx.com/xlnx/xil_ans_display.jsp?iCountryID=1&iLanguageID=1&getPagePath=23625

Notes and Recommendations

ESD Protection

- The MGTREFCLKN, MGTREFCLKP, and MGTVREF pins ESD protection meet HBM 1000V and 150V CDM. Added care is recommended during handling.

Traceability

The XC5VSX50TCES is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

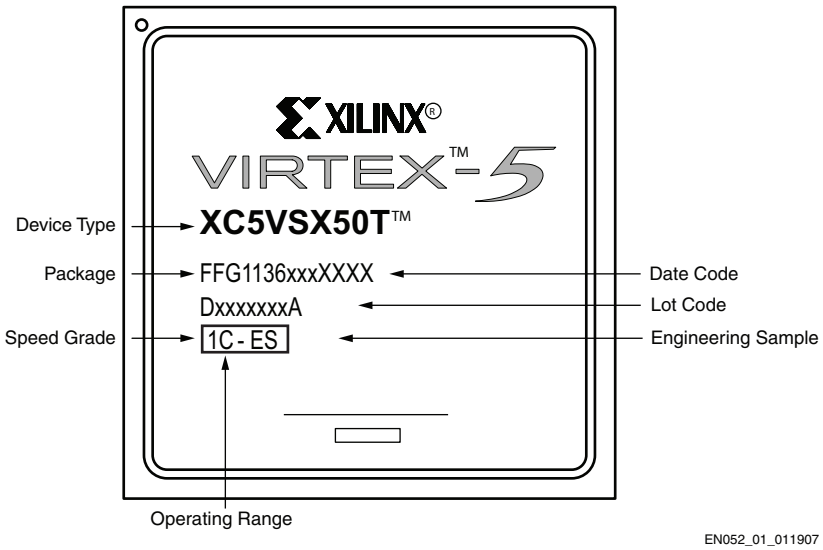

Figure 1: **Example XC5VSX50TCES Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the current data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

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http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-5 documents:

- Virtex-5 Overview (http://www.xilinx.com/bvdocs/publications/ds100.pdf)
- Virtex-5 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds202.pdf)
- Virtex-5 User Guide (http://www.xilinx.com/bvdocs/userguides/ug190.pdf)
- Virtex-5 XtremeDSP™ Design Considerations (http://www.xilinx.com/bvdocs/userguides/ug193.pdf)
- Virtex-5 Configuration Guide (http://www.xilinx.com/bvdocs/userguides/ug191.pdf)
- Virtex-5 Packaging and Pinout Specification (http://www.xilinx.com/bvdocs/userguides/ug195.pdf)
- Virtex-5 RocketIO GTP Transceiver User Guide (http://www.xilinx.com/bvdocs/userguides/ug196.pdf)
- Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs (http://www.xilinx.com/bvdocs/userguides/ug197.pdf)
- Virtex-5 Embedded Tri-mode Ethernet MAC User Guide (http://www.xilinx.com/bvdocs/userguides/ug194.pdf)

Revision History

Date	Version	Description
02/09/07	1.0	Initial Xilinx release.
04/09/07	1.1	Updated the Configuration section. Removed the GTP CRC Parallel Interface Timing section.
05/11/07	1.2	Added the Block RAM ECC Scrub Mode, AC JTAG, GTP CRC Parallel Interface Timing, and GTP Transmit Interface Timing errata. Updated the Configuration section. Removed the GTP CRC Parallel Interface Timing section.
05/14/08	1.3	Updated JTAG IDs in Table 1.

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