Spartan-3E XC3S1600E FPGA Errata

EN094 (v1.0) October 19, 2007 **Errata Notice**

Hardware Errata

There are no errata for the Spartan-3E XC3S1600E FPGA.

See the "Production Stepping" section in the data sheet for additional information:
http://www.xilinx.com/bvdocs/publications/ds312.pdf

Advisories

This section advises designers of any potential software changes that may affect their XC3S1600E FPGA applications. Table 1 summarizes the advisories and indicates which software update will correct the issue.

Table 1: **Advisories and Software Update**

Advisory	ISE™ Software Version
"Persist I/O Conflict"	10.1

Persist I/O Conflict

Applications affected

This issue affects applications that use the Persist option in the Bitstream Generator and use configuration address pins A20-A23 in the design. The current software allows this conflict between Persist and user functionality, so the user must be careful to avoid this situation. Persist is set to No by default, and can be enabled by *Persist:Yes* at the command line or *"Allow SelectMAP Pins to Persist"* in the Project Navigator. Persist is most commonly used to allow Readback through the Slave Parallel (SelectMAP) configuration port after configuration. This issue affects all XC3S1600E devices.

Description

Using the Persist option in the Bitstream Generator, and setting the Mode pins to a parallel configuration mode including Byte Peripheral Interface (BPI) or Slave Parallel (SelectMAP) modes, will retain the parallel configuration interface. This is useful when configuring in the SelectMAP mode to allow configuration commands such as Readback to be used after configuration. The pins affected by Persist cannot be used in the design, including M[2:0], CCLK, D[7:0], INIT_B, CSI_B, RDWR_B, and BUSY, as described in the documentation.

The issue is that Persist will block four additional specific dual-purpose I/Os from use by the design when Persist is enabled and the Mode pins are set for a parallel configuration mode. These pins become disconnected from the user design when Persist is used and therefore cannot be used by the design. If unused in the design, these pins will have a weak pull-down resistor when Persist is used. If used in the design, the pin state is design-dependent.

The affected I/Os are the highest order address lines for the configuration interface, A20-A23. The associated pin numbers are shown in Table 2. No other address lines will be affected by Persist.

This issue affects all Spartan-3E part/package combinations that support A20-A23. This issue does not affect the XC3S100E device, or the VQ(G)100 and TQ(G)144 packages.

Table 2: **Affected Pins**

Package	A20(1)	A21(2)	A22(2)	A23(2)
FG(G)320	R14	T14	R13	P13
FG(G)400	V16	U16	Y14	Y15
FG(G)484	Y18	W18	AB17	AA17

Notes:

1. In FG(G)400 and FG(G)484, pin name IO_LxxN_2/A20, not ball location A20.
2. In FG(G)484, pin names IO_L38P_2/A21, IO_L35N_2/A22, and IO_L35P_2/A23, not ball locations A21, A22, A23.

Workaround

Customers who use the Persist option in the Bitstream Generator and who use a parallel configuration mode must not use the affected I/O pins in the design. No I/O should be placed on these pins by the user, and the pins need to be prohibited for the tools by using the Prohibit constraint on each pin. This constraint can be specified in the User Constraints File (UCF) with the following syntax:

```
CONFIG PROHIBIT=R14,T14,R13,P13;
```

Alternatively, consider not using Persist if post-configuration Readback is not required.

These pins will be added to the list of pins that Persist in the documentation. In ISE software version 10.1 and later, an error message will be provided by the bitstream generator if Persist is used and the design uses these four pins.

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For questions, please contact Xilinx Technical Support http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx sales representative, http://www.xilinx.com/company/contact.htm.

Obtaining Errata Notification Updates

If this document is printed or saved locally, please check for the most recent release, available to registered users on the Xilinx web site at http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata. To receive an e-mail alert when this document changes, sign up at http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

Applicable Documents

These errata apply to the following XC3S1600E documents:

- **DS312: Spartan™-3E FPGA Family Data Sheet**
  www.xilinx.com/bvdocs/publications/ds312.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/bvdocs/userguides/ug331.pdf
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/bvdocs/userguides/ug332.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Description
10/19/07	1.0	Initial version