

## Introduction

Thank you for participating in the Virtex®-6 FPGA Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

## Devices

These errata apply to the devices shown in [Table 1](#).

*Table 1: Devices Affected by These Errata*

Devices	XC6VHX255T CES	JTAG ID (Revision Code): 2
	XC6VHX380T CES	JTAG ID (Revision Code): 2
	XC6VHX565T CES	JTAG ID (Revision Code): 0
Packages	FF(G)1155, FF(G)1923, FF(G)1924	
Speed Grades	-1, -2	

## Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

### MMCM

#### ***Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED***

When the Phase Frequency Detector (PFD) frequency ( $F_{IN}/D$ ) is lower than 135 MHz and the BANDWIDTH attribute of the MMCM is set to HIGH or OPTIMIZED, a phase error between MMCM output clocks can occur, making the output clock signals invalid. This condition can also cause the fractional output counter to fail.

The ISE® software v12.4 and later provides appropriate warnings for possible violations of this restriction.

The ISE software v12.4 and later correctly handles designs set to OPTIMIZED bandwidth for all valid PFD frequencies.

This issue will not be fixed in the devices listed in [Table 1](#).

#### **Work-around**

PFD frequencies lower than 135 MHz must use LOW bandwidth mode to ensure correct operation.  
See [Answer Record 38132](#) for more information.

#### ***Restriction of Clock Divider Values***

The input clock divider (DIVCLK\_DIVIDE) cannot have a value of 3 or 4 when the input clock frequency ( $F_{IN}$ ) of the MMCM is above 315 MHz.

The ISE software v12.4 and later provides appropriate warnings for possible violations of this restriction.

This issue will not be fixed in the devices listed in [Table 1](#).

#### **Work-around**

In all designs in which  $F_{IN}$  is above 315 MHz and DIVCLK\_DIVIDE is set to 3 or 4, double the CLKFBOUT\_MULT\_F and DIVCLK\_DIVIDE values. See [Answer Record 38133](#) for more information.

## Block RAM

### ***Dual Port Block RAM Address Overlap in READ\_FIRST and Simple Dual Port Mode***

When using the block RAM in True Dual Port (TDP) Read\_First mode, Simple Dual Port (SDP) mode, or ECC mode with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.3.1 (or later) of [UG363](#), *Virtex-6 FPGA Memory Resources User Guide*.

This description was originally added in UG363 (v1.1), published 9/16/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. The ISE v12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in [Table 1](#).

#### **Work-around**

The recommended work-around is to configure the block RAM in WRITE\_FIRST mode. WRITE\_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE\_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.2 and later. See [Answer Record 34859](#).

### ***Synchronous Built-in FIFO***

When using the Built-In FIFO as a Synchronous FIFO (EN\_SYN=TRUE) with asynchronous reset, correct behavior of the FIFO flags cannot be guaranteed after the first write.

All configurations other than EN\_SYN=TRUE are not affected by this issue.

#### **Work-arounds**

To work around this issue, synchronize the negative edge of reset to RDCLK/WRCLK.

For more information and additional work-arounds see [Answer Record 41099](#).

## Configuration

### ***PROGRAM\_B Pin Behavior During Power-On***

Holding the PROGRAM\_B input statically Low prior to the completion of the power-on reset does not hold the FPGA in configuration reset. Instead, the FPGA proceeds with its standard power-on configuration sequence.

This issue will not be fixed in the devices listed in [Table 1](#).

#### **Work-around**

For systems that need to delay the FPGA configuration sequence at power-on, hold the INIT\_B pin Low.

See [Answer Record 38134](#) for more information.

### ***Input Logic Resets Using GSR***

When coming out of configuration after power-up or after asserting the PROGRAM\_B\_0 pin, the ILOGIC input registers (IFF, IDDR, and ISERDES) are not guaranteed to be initialized to zero. The same holds true if the GSR input of the STARTUP\_VIRTEX6 block is used to reset the ILOGIC input registers. Initializing the registers to a one (using the "INIT=1" attribute) works as expected.

#### **Work-around**

If the user application requires the input registers to be initialized to zero, then a separate reset using general interconnect must be implemented.

## GTH Transceivers

### **Supported PCB Trace Characteristics**

The GTH transceiver in the devices listed in [Table 1](#) is intended for use in short-reach applications with a PCB trace of up to 8 inches or less of FR-4. The recommended near end transmit signal swing should be between 370 mVppd and 770 mVppd for best jitter performance. For the devices listed in [Table 1](#), backplane applications are not supported.

Refer to [Answer Record 38283](#) for details.

### **RX Equalization Auto-Adaptation**

Auto-adaptation is not supported in the devices listed in [Table 1](#).

Refer to [Answer Record 37414](#) for details regarding RX AGC and DFE settings.

### **T\_BLOCK\_TYPE Misclassification in 10 Gigabit Ethernet 64B/66B Mode**

The GTH transceiver implements a 10 Gigabit Ethernet 64B/66B block based on IEEE Std 802.3-2008 Clause 49. The GTH transceiver deviates from the T\_BLOCK\_TYPE classification requirements in Subclause 49.2.13.2.3.

In Subclause 49.2.13.2.3, an excerpt of T\_BLOCK\_TYPE states that:

T\_BLOCK\_TYPE will = C when: "one valid ordered set and four valid control characters other than /O/, /S/ and /T/."

The GTH 64B/66B encoder implements the following:

T\_BLOCK\_TYPE will = C when: "one valid ordered set and four valid control characters other than /E/, /O/, /S/ and /T/."

Refer to [Answer Record 38283](#) for details.

### **Near End PMA Loopback**

Near end PMA loopback using the post driver (PMA\_LPBK\_CTRL\_LANE<n> = 2'b01) is not supported.

### **IEEE Std 1149.6 (AC-JTAG) Test Utilizing GTH Transceivers**

AC-JTAG test is not supported with unconfigured GTH transceivers.

#### **Work-around**

Refer to [Answer Record 37763](#) for details.

## GTX Transceivers

### **GTX Transceiver Initialization for Proper TXOUTCLK Functionality**

TXOUTCLK can operate at an incorrect frequency or can remain in a static state when the TXPLL\_DIVSEL\_OUT attribute is set to 2 or 4 and the TXOUTCLK\_CTRL attribute is set to "TXOUTCLKPCS", "TXOUTCLKPMA\_DIV1", or "TXOUTCLKPMA\_DIV2".

An updated reset sequence that ensures proper functionality is documented in version 2.4 of [UG366](#), *Virtex-6 FPGA GTX Transceiver User Guide*. Also see [Answer Record 35681](#) for more information.

## ***RXRECCLK Static Operating Behavior***

The RXRECCLK output port might operate at reduced frequency in buffer bypass mode if conditions (1) and (2) persist for more than 15,000 cumulative hours at 65°C T<sub>j</sub>, 2,500 cumulative hours at 85°C T<sub>j</sub>, or 800 cumulative hours at 100°C T<sub>j</sub>:

1. Power has been applied to V<sub>CCINT</sub>.
2. The device is in one of the following states:
  - a. The FPGA is not configured
  - b. The FPGA is configured, but the transceiver is uninstantiated
  - c. The transceiver is instantiated, but no reference clock is toggling
  - d. The transceiver is instantiated, but is held in reset or power-down

### **Work-around**

#### ***Transceivers Uninstantiated in User Design but are Planned to be Used in the Future***

For transceivers that are not instantiated in the user design but are planned to be used in the future, power must be applied to MGTAVCC, and the user design must be implemented using ISE v12.1 (or later) software for automatic insertion of the work-around circuit.

#### ***Transceivers Uninstantiated in User Design but are Not Planned to be Used in the Future***

Automatic insertion of the work-around circuit can be disabled for uninstantiated transceivers that will not be used.

#### ***Transceivers Instantiated in User Design***

Transceivers instantiated in user design do not require a work-around circuit if the reference clock is toggling and the transceiver is not held in reset or power-down.

See [Answer Record 35055](#) for more information.

## ***GTX Transceiver Delay Aligner***

The GTX Transceiver Delay Aligner circuit is used when the TX Buffer and/or RX Elastic Buffer are bypassed.

The Transmitter Delay Aligner is no longer supported; additionally, the use model of the Receiver Delay Aligner must be changed.

Applications that use the TX Buffer and RX Elastic Buffer are not affected by this errata item.

Applications currently bypassing the TX Buffer and/or RX Elastic Buffer, including XAUI, RXAUI, CPRI, OBSAI, and PLBv46 RC/EP Bridge for PCI Express® IP cores and the Integrated Block for PCIe, must implement the following work-around.

### **Work-around**

The TX Buffer and RX Elastic Buffer can still be bypassed using work-arounds described in [Answer Record 39430](#) to maximize system margin.

## **System Monitor**

### ***System Monitor Internal Reference Voltage***

The System Monitor Internal Reference Voltage is not supported in the devices listed in [Table 1](#). The External Reference Voltage must be used. See the System Monitor Dedicated Pins figure in [UG370](#), Virtex-6 FPGA System Monitor User Guide.

### ***System Monitor Maximum DCLK Frequency***

The System Monitor intermittently generates an incorrect analog-to-digital conversion when the clock (DCLK) frequency is greater than 80 MHz. The maximum frequency specification for DCLK is being revised down from 250 MHz to 80 MHz. All designs should be updated to use 80 MHz maximum.

This issue will not be fixed in the devices listed in [Table 1](#).

The maximum frequency specification has been updated in DS152, v2.9 (9/20/10).

## Auxiliary Analog Channel Support

Channels 8 to 15 on bank #25 are not supported. All devices listed in [Table 1](#) are affected.

## Operational Guidelines

### GTH Attribute and Port Settings

For GTH transceiver attribute settings, see [Answer Record 37414](#).

### GTH Transceiver Initialization Sequence

The initialization sequence defined in [Answer Record 37412](#) must be performed.

### GTH TXUSERCLKOUT and RXUSERCLKOUT in 10 Gigabit Ethernet 64B/66B Mode

See [Answer Record 38283](#) for additional information.

## Design Software Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx development software installations.

- Xilinx ISE Design Suite 12.3 or later version of software.
- See Known Issues in [Answer Record 34466](#).

## Traceability

The XC6VHX380T is marked as shown in [Figure 1](#).

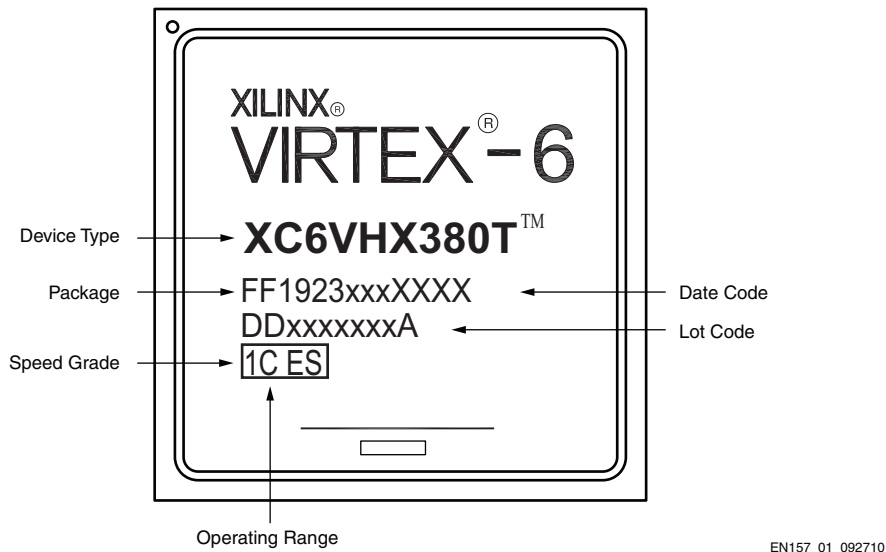


Figure 1: Example Device Top Mark

## Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact.htm>.

## Revision History

Date	Version	Description
09/30/10	1.0	Initial Xilinx release.
11/16/10	1.1	Added HX255T device to document. Updated <a href="#">Table 1</a> . Added <a href="#">Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED</a> , <a href="#">Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED</a> , <a href="#">Restriction of Clock Divider Values</a> , <a href="#">PROGRAM_B Pin Behavior During Power-On</a> , <a href="#">Configuration Readback</a> , and <a href="#">GTX Transceiver Initialization for Proper TXOUTCLK Functionality</a> .
01/17/11	1.2	Removed Configuration Readback; it does not apply to these devices. Updated TXOUTCLK and RXRECCLK Static Operating Behavior; no longer applicable to TXOUTCLK. Added <a href="#">GTX Transceiver Delay Aligner</a> per Xilinx Customer Notice XCN11009.
04/11/11	1.3	Added <a href="#">Synchronous Built-in FIFO</a> and <a href="#">Input Logic Resets Using GSR</a> .

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