Introduction

Thank you for designing with the Spartan®-6Q FPGA defense-grade family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the Spartan-6Q devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	JTAG ID (Revision Code)
XQ6SLX75	2 or higher
XQ6SLX75T	2 or higher
XQ6SLX150	4 or higher
XQ6SLX150T	4 or higher
Package	All
Speed Grades	-1L, -2, -2Q, -3

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

IODELAY2

Speed Grades -2, -2Q, -3

In the devices listed in Table 1, for speed grades -2, -2Q, and -3, the IODELAY2 block can experience single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

Single Data Bit Corruption in IDELAY and ODELAY Modes

The IODELAY2 block can corrupt a single data bit for some IDELAY_VALUE and ODELAY_VALUE settings.

Work-arounds

IDELAY_TYPE=FIXED, VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX or DIFF_PHASE_DETECTOR, or when used in ODELAY mode

Limit the data rate through the IODELAY2 to the maximum specifications in Table 2.

Table 2: **Maximum IODELAY2 Data Rate**

V_{CCINT} Range	Temperature	Maximum Data Rate (Mb/s)[1]	
		-3	-2, -2Q
Standard Performance (Standard V_{CCINT})	Industrial, Q-Grade	740	625
Extended Performance (Requires Extended Performance V_{CCINT})		860	700

Notes:

1. Higher data rates are achievable when certain system design restrictions or considerations are taken into account. See Answer Record 41083 for additional information.

IDELAY_TYPE=FIXED or VARIABLE_FROM_ZERO or when used in ODELAY mode, with tap limit

When using a fixed tap value and requiring higher performance than specified in Table 2, restricting the maximum IDELAY_VALUE or ODELAY_VALUE can avoid data corruption at the higher indicated data rates. Table 3 provides a summary of these higher data rates for fixed tap values.

Table 3: **Maximum IDELAY_VALUE or ODELAY_VALUE**

Maximum DELAY Value	Maximum Data Rate (Mb/s)	
	-2, -2Q	-3
6	950	1,080
7		1,050
8		1,000
9		950
14	800	800
18	700	See Table 2
20	667	See Table 2

Speed Grade -1L

The Lower Power -1L devices in Table 1 do not support the IODELAY2 block except when using tap 0. Table 4 shows the supported attributes for the IODELAY2 block.

Table 4: **Supported IODELAY2 Attributes for -1L**

Mode	IDELAY_TYPE	Tap Selection
IDELAY (Input)	FIXED	IDELAY_VALUE=0
	DEFAULT	N/A
ODELAY (Output)	N/A	ODELAY_VALUE=0

MCB interfaces are not affected by the IODELAY2 errata.

See Answer Record 41356 for additional information.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installation:

- Refer to the Spartan-6 Device Production Software and Speed Specification Release table in DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* for the Xilinx ISE Design Suite version required for the selected part.
- See ISE 13 Software Known Issues with regards to Spartan-6 FPGAs in Answer Record 40000.

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
07/11/11	1.0	Initial Xilinx release.

Notice of Disclaimer