

GTPs

SATA, SFP and SGMII

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USB Host
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Headers for
System Mon

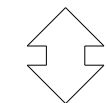
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2 line
Character LCD

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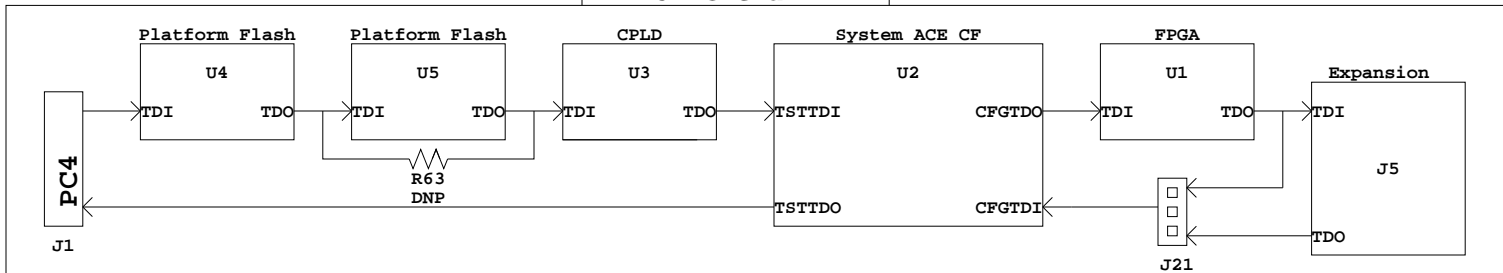
PS2 Keybaord &
Mouse

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PC4

JTAG Chain



5V
PWR
Jack

Power Supply

Page 25-26

Switcher

5.0V@10A max

Linear

0.9V@1.4A max

Switcher

3.3V@10A max

Linear

2.5V@3A max

Linear - VCCAUX

2.5V@3A max

Linear MGT PLL

1.2V@3A max

Linear - MGT AVTT RX

1.2V@3A max

Switcher

1.8V@10A max

Linear - MGT AVCC

1.0V@3.0A max

Linear - MGT AVTT TX

1.2V@3.0A max

Switcher

1.0V@16A max



Title: ML505/6/7 Block Diagram
SCHEM, ROHS COMPLIANT
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

Date: 1-22-2008_14:51

Ver: A

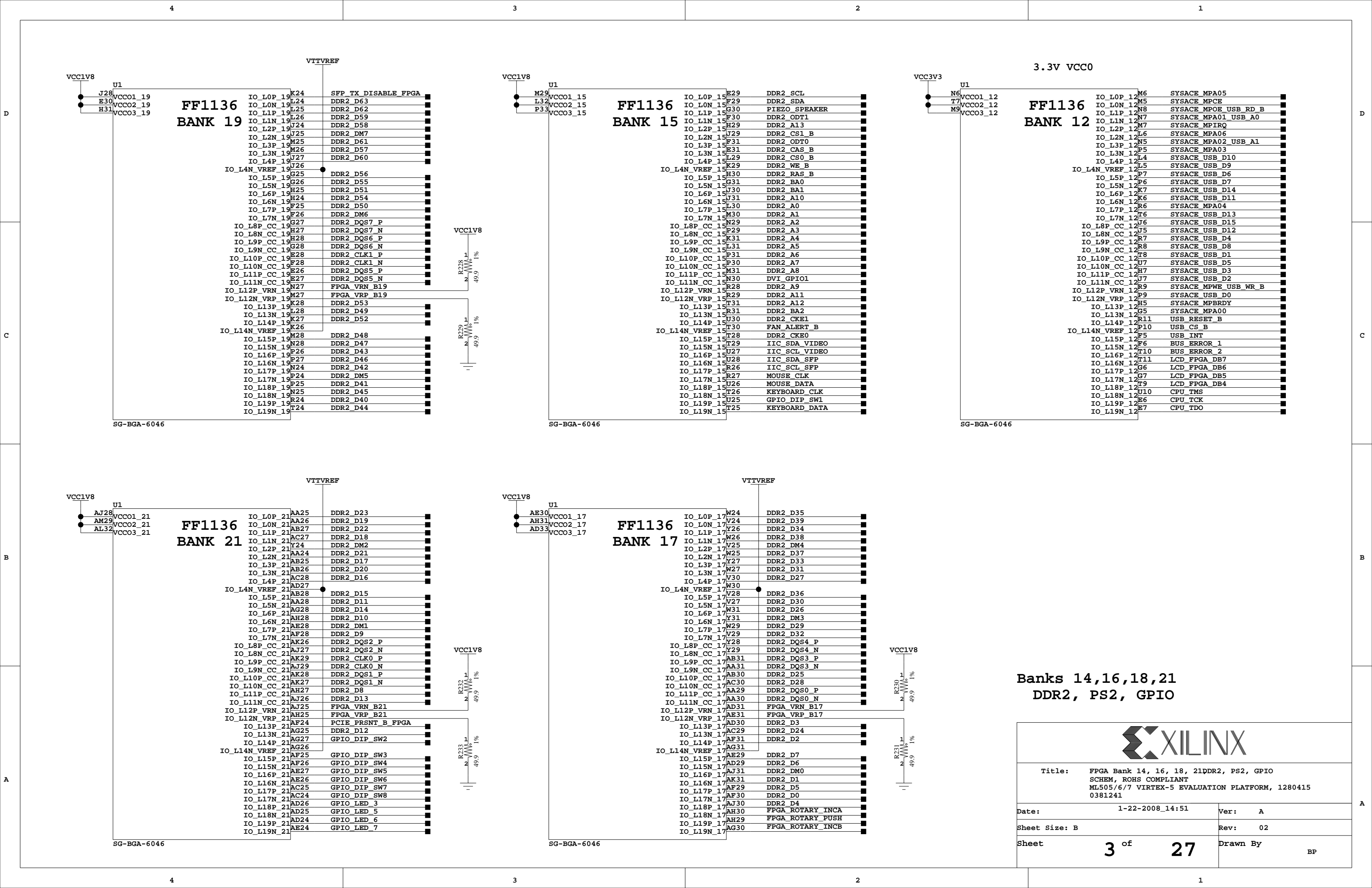
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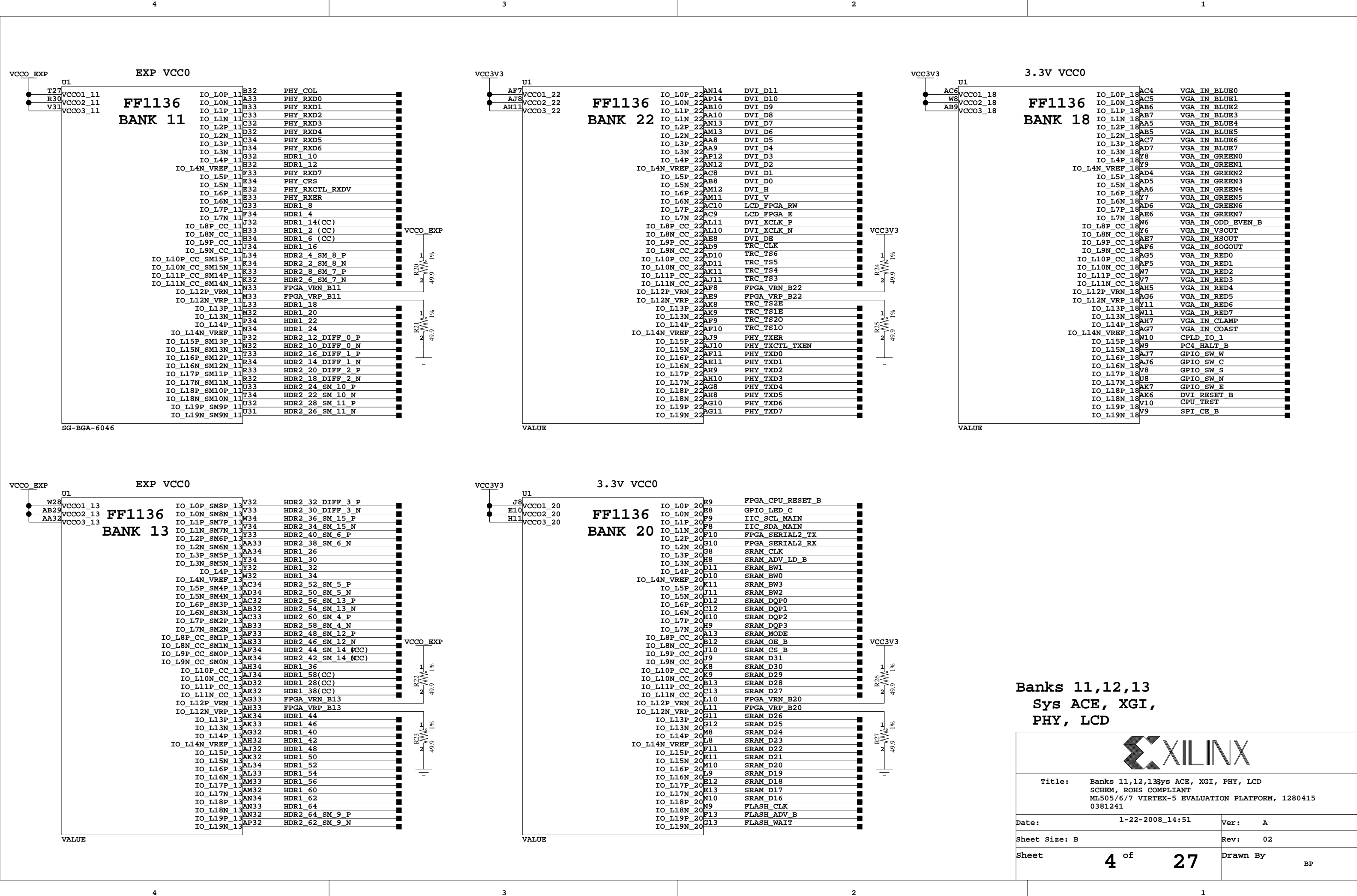
Rev: 02

Sheet 1 of

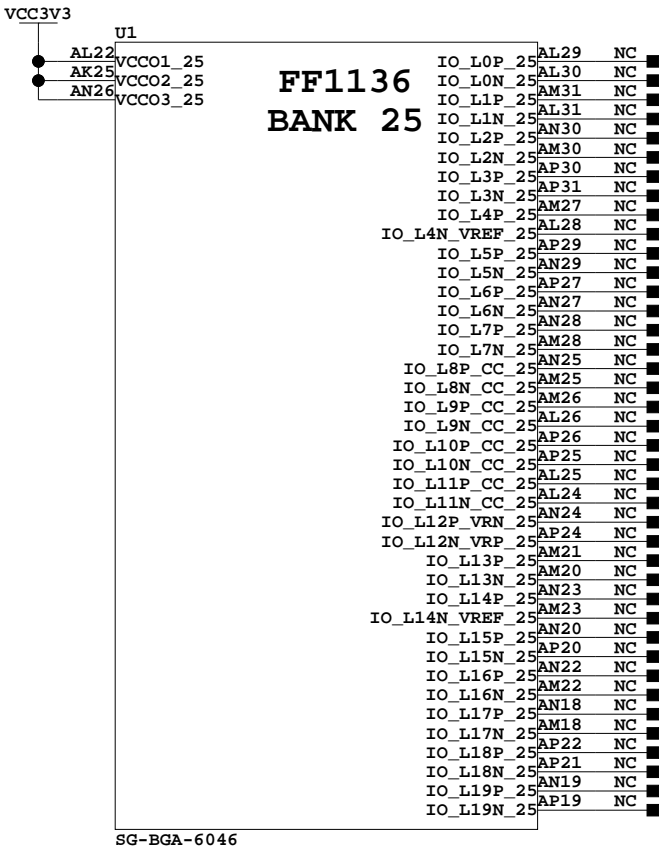
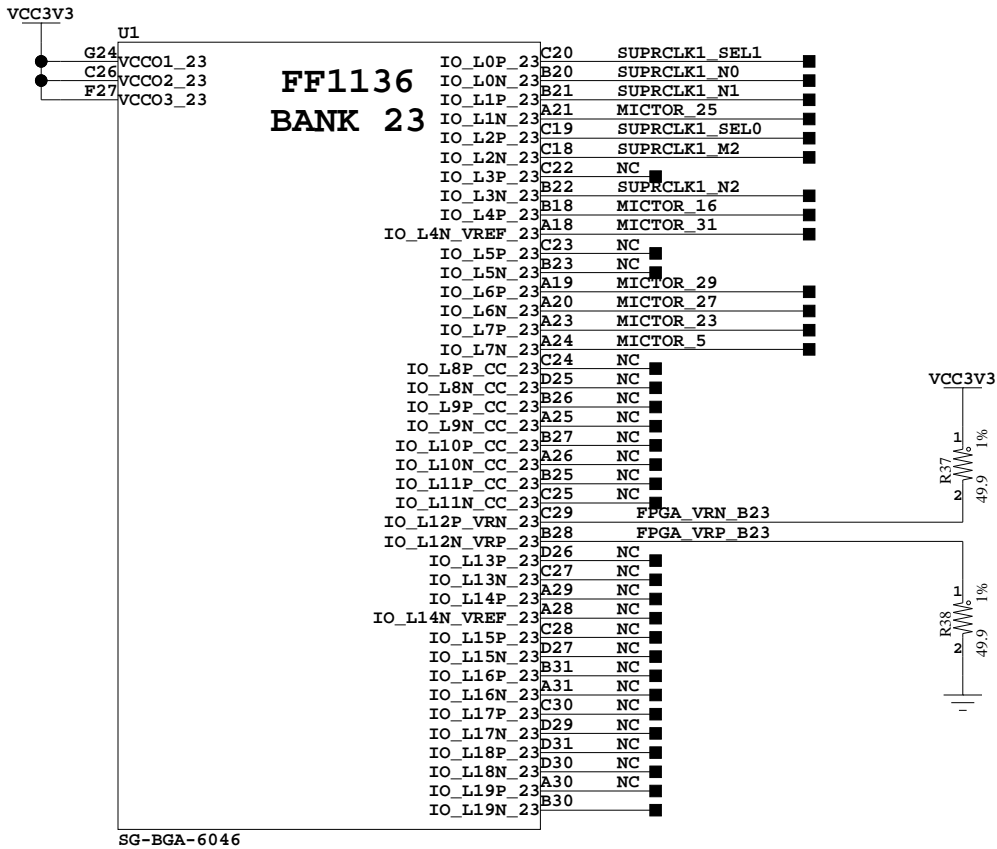
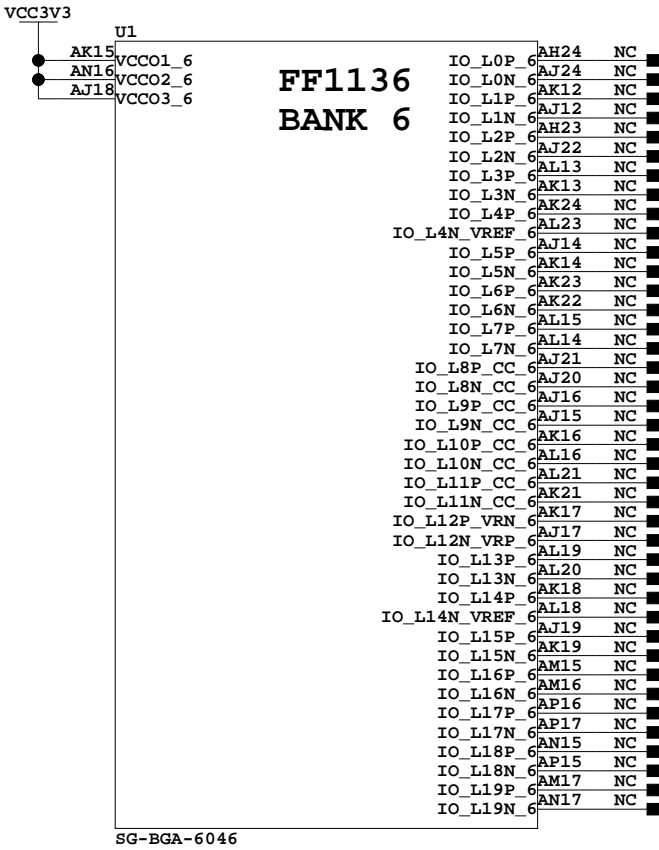
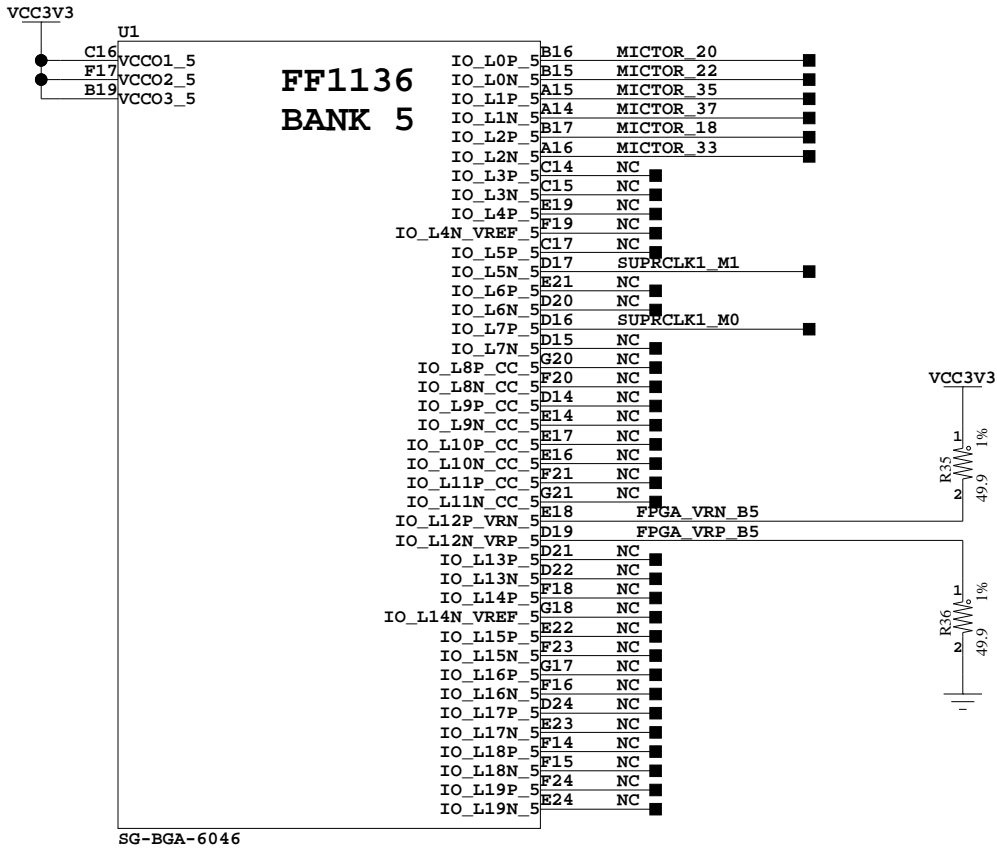
27

Drawn By BP






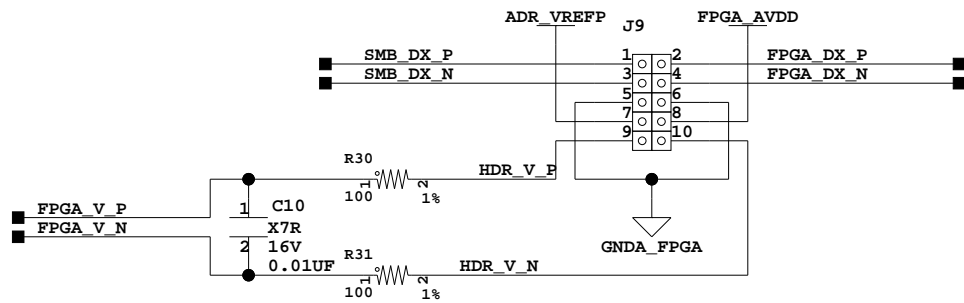
Unused banks on the LX50T and SX50T



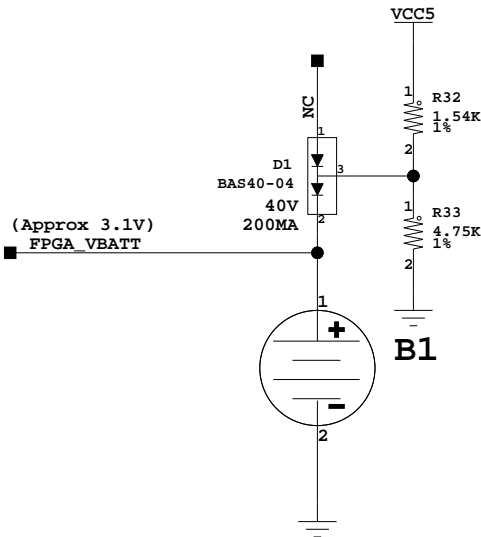
Banks 15, 17
VGA, IIC, PHY
SRAM, FLASH, GPIO

			
Title:		Banks 11,12,13,VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
Sheet	5 of 27	Drawn By	BP

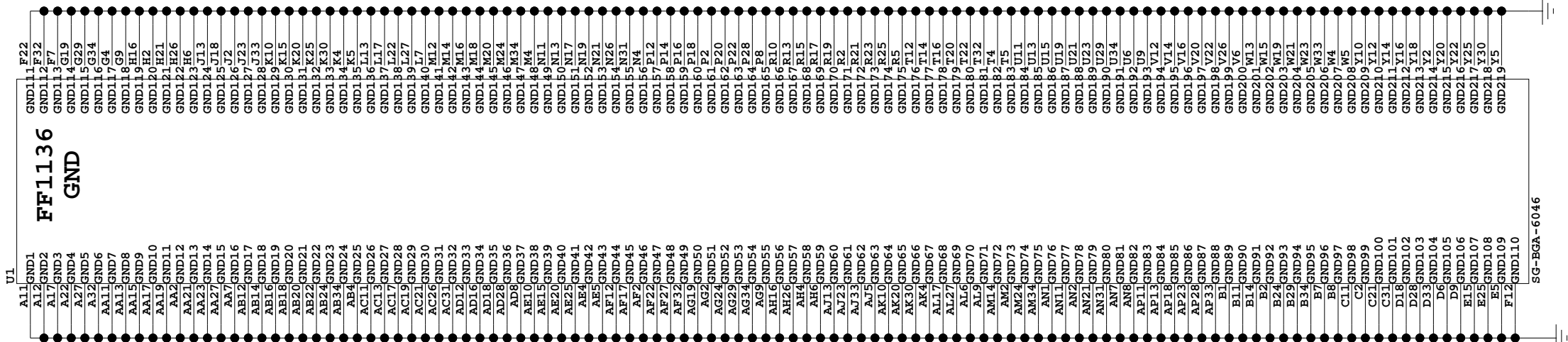
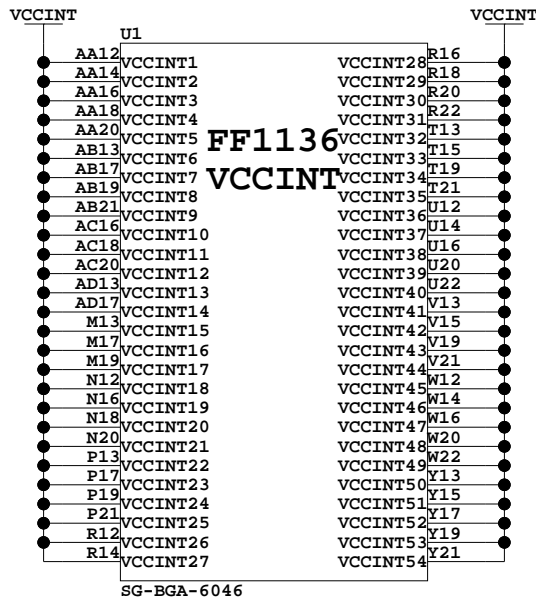
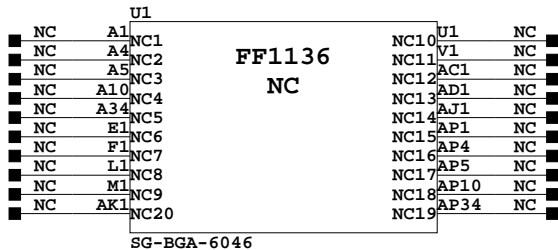
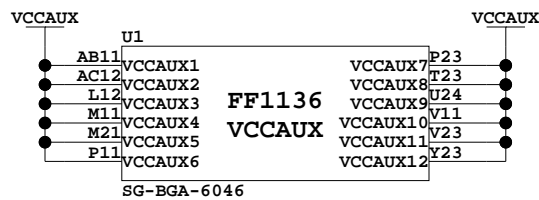
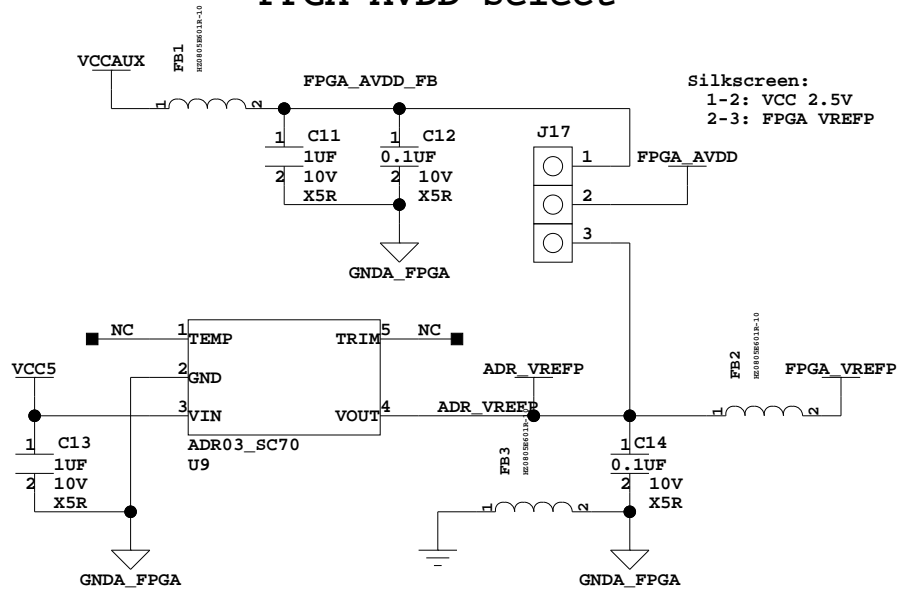
System Monitor Header



Rechargeable Battery



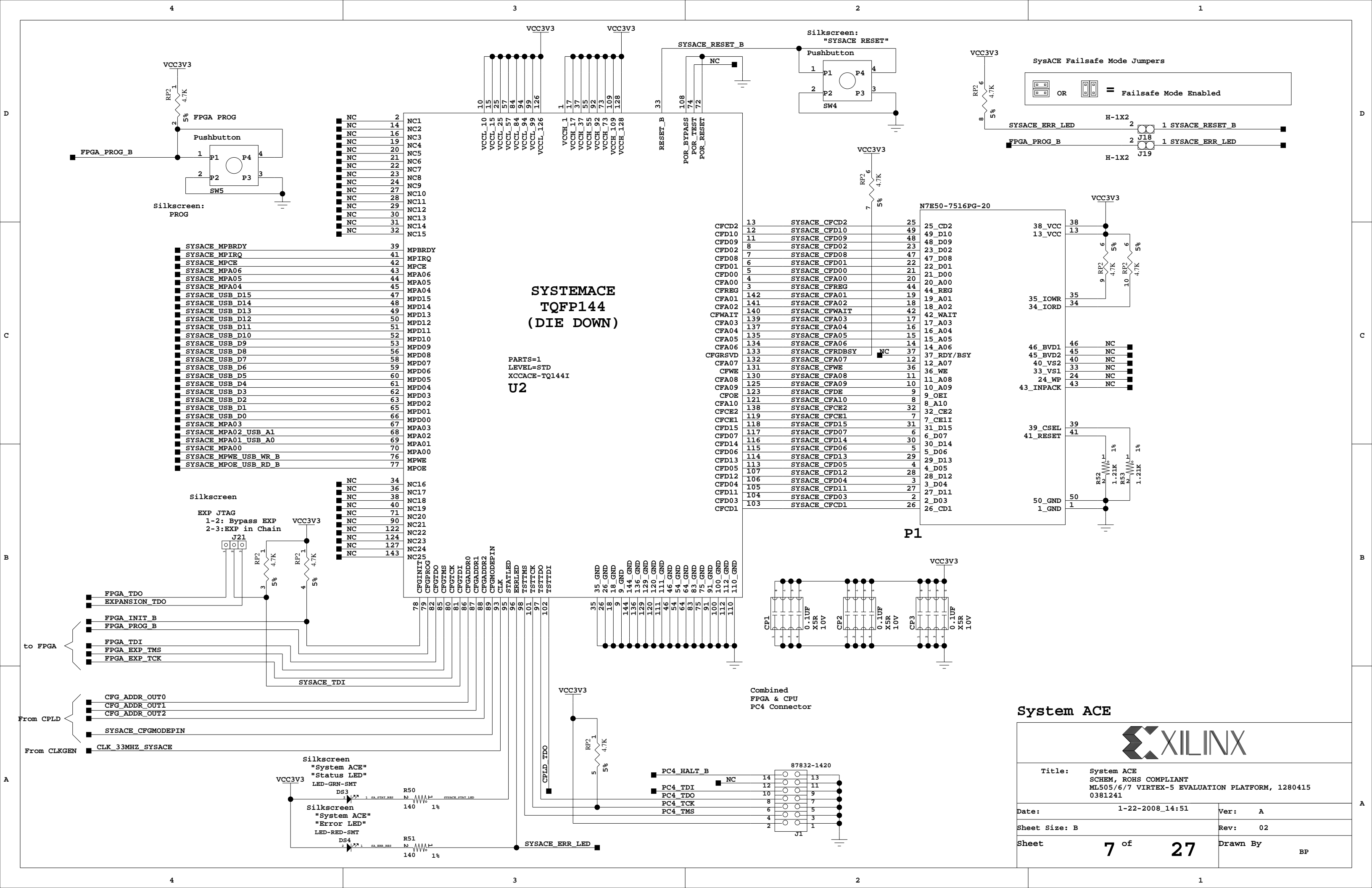
FPGA AVDD Select

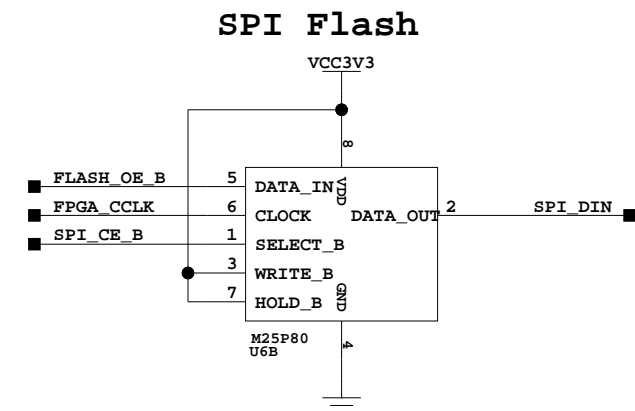
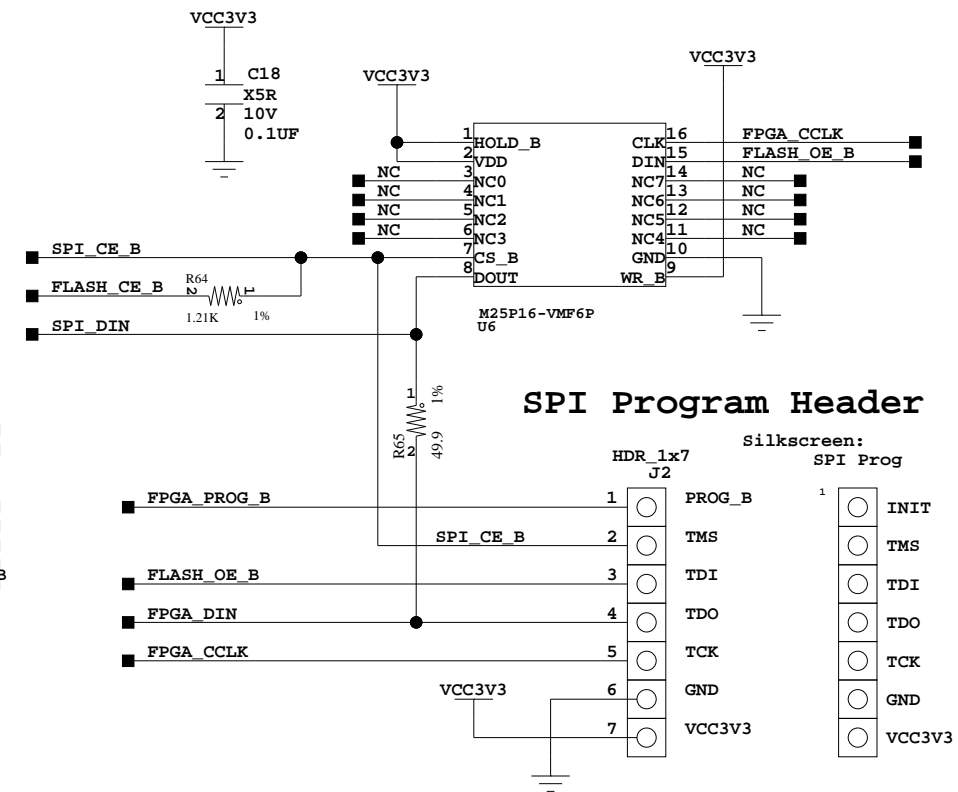
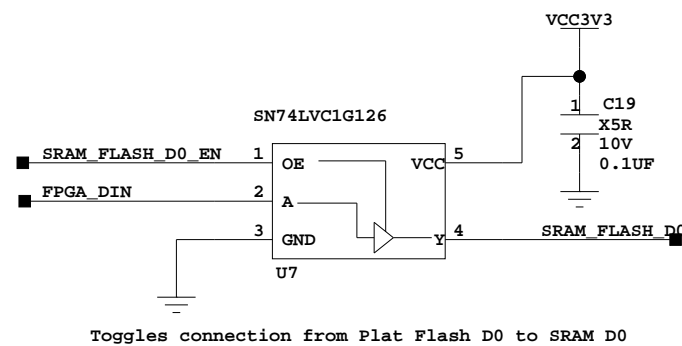
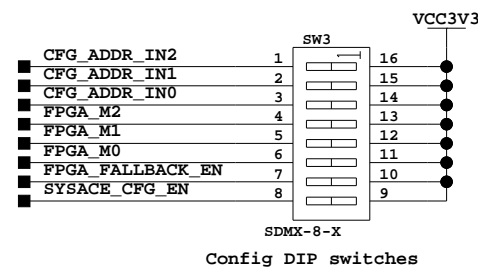
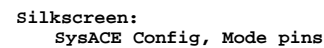
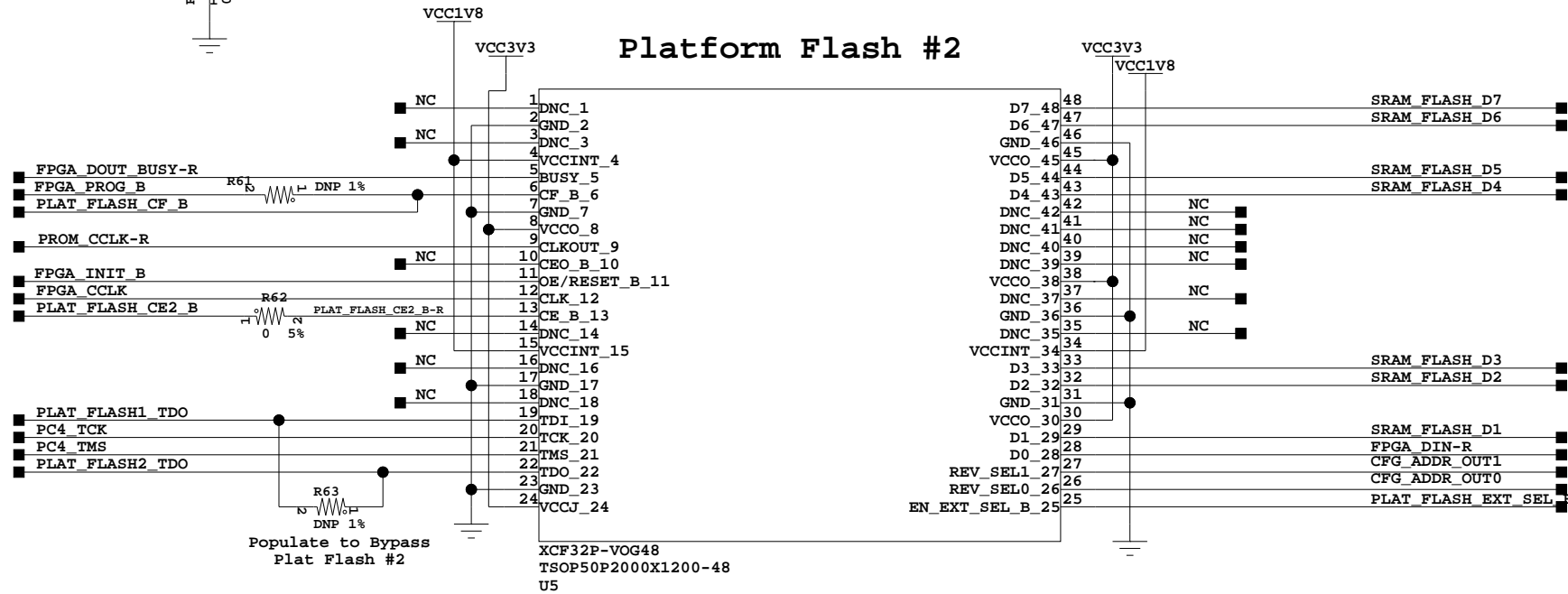
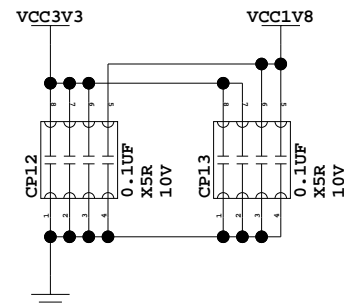
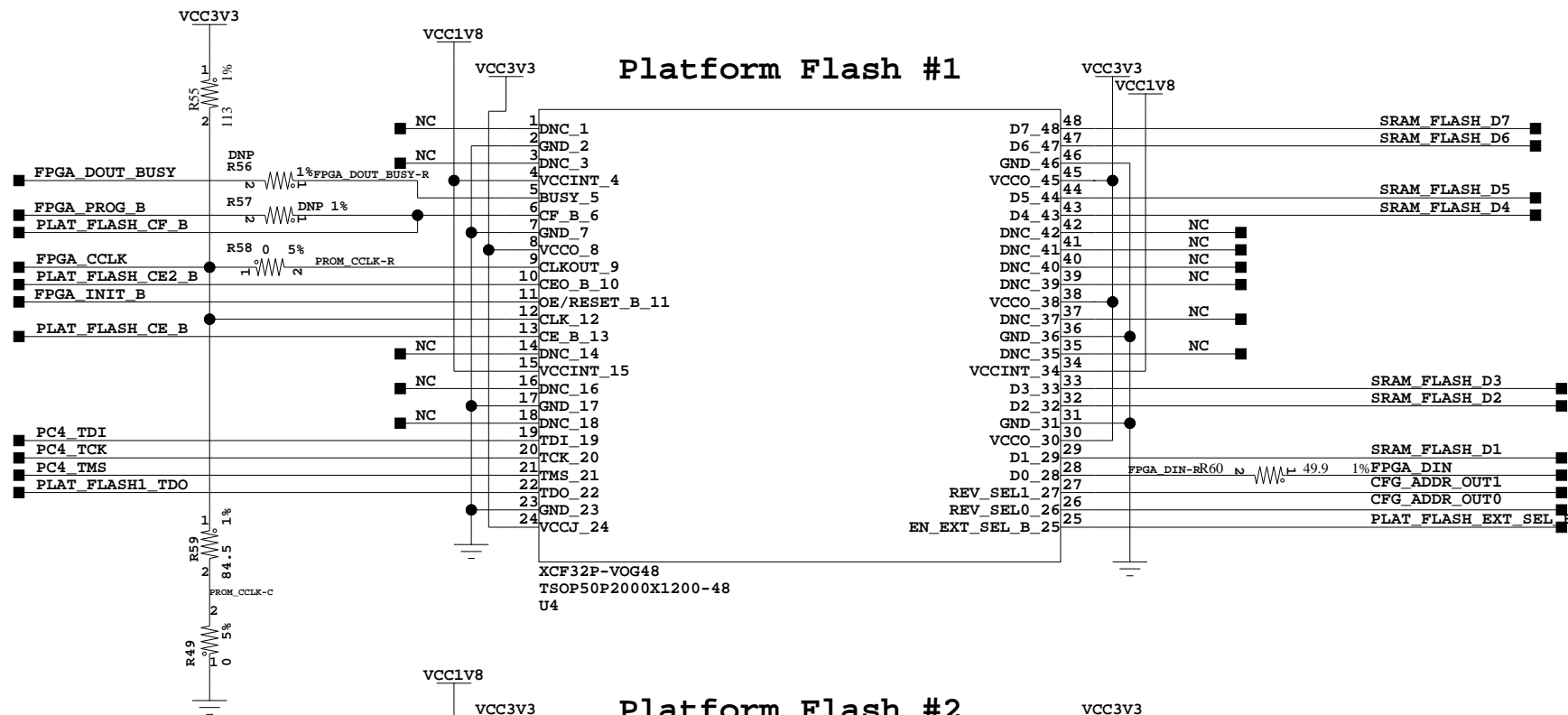
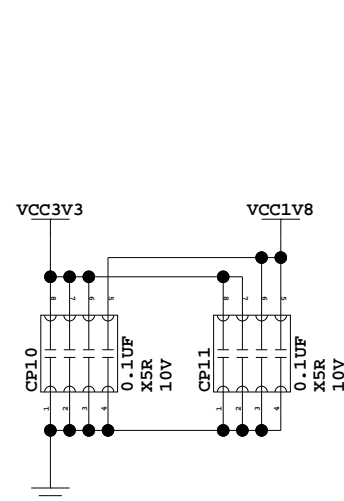


Power and Misc FPGA Banks
VCCINT, VCCAUX, NCs, GND
Battery and System Monitor



Title: FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
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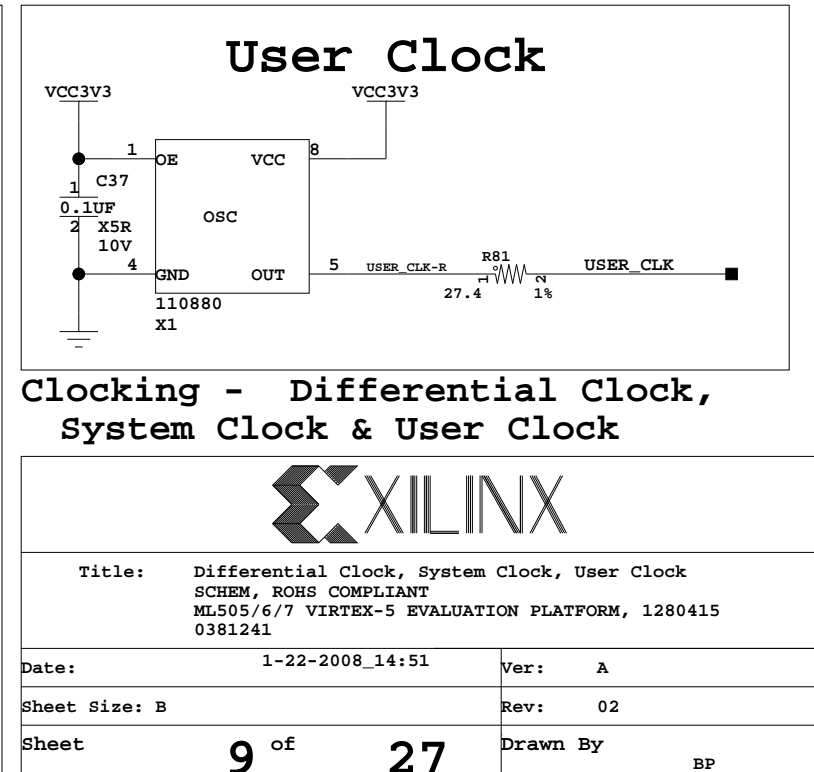
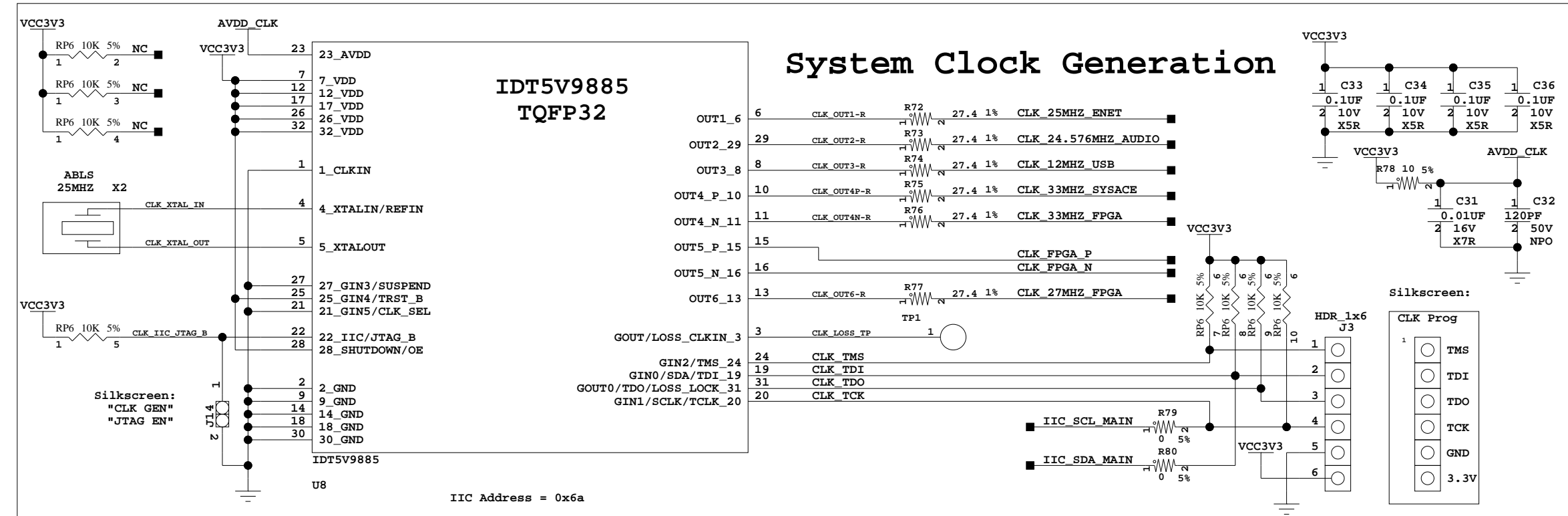
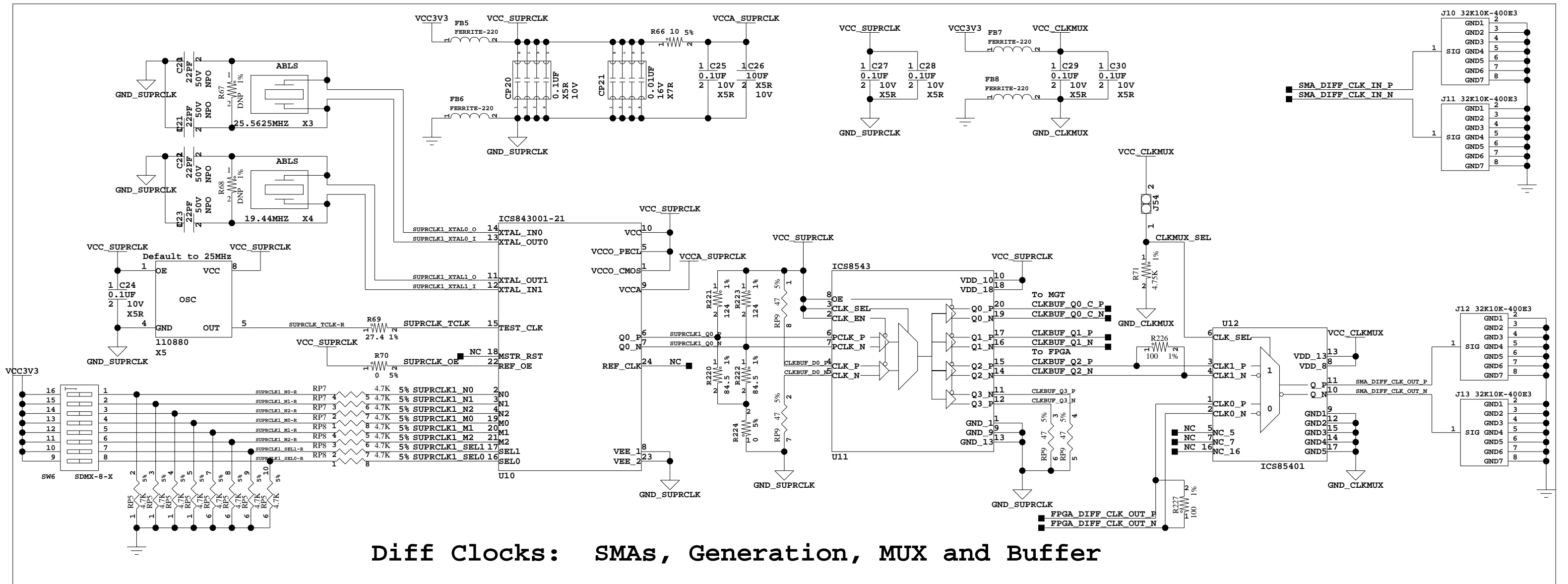


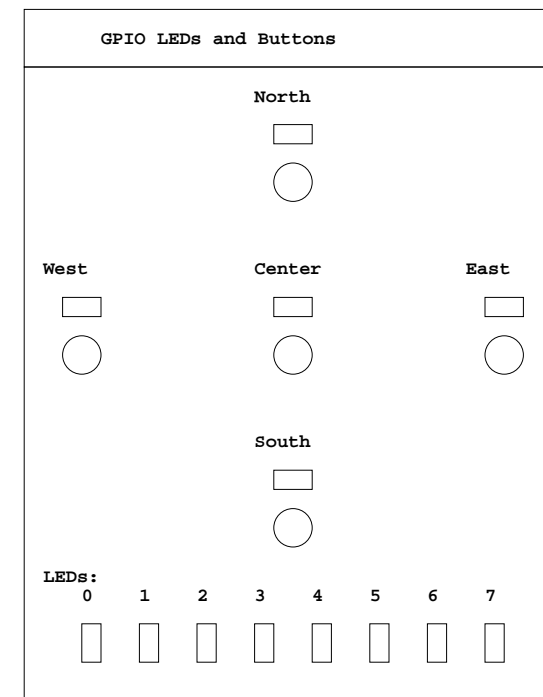
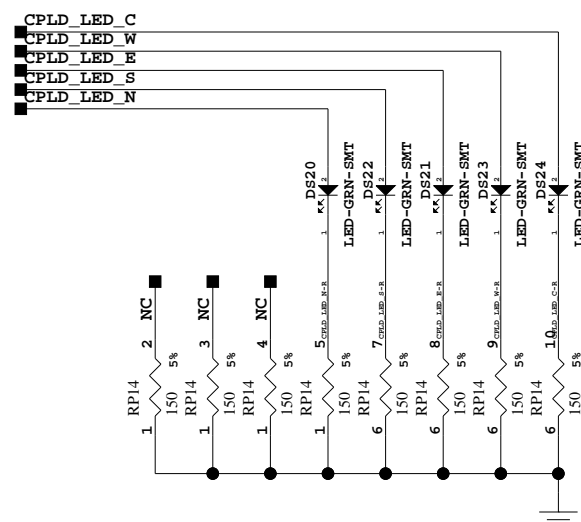
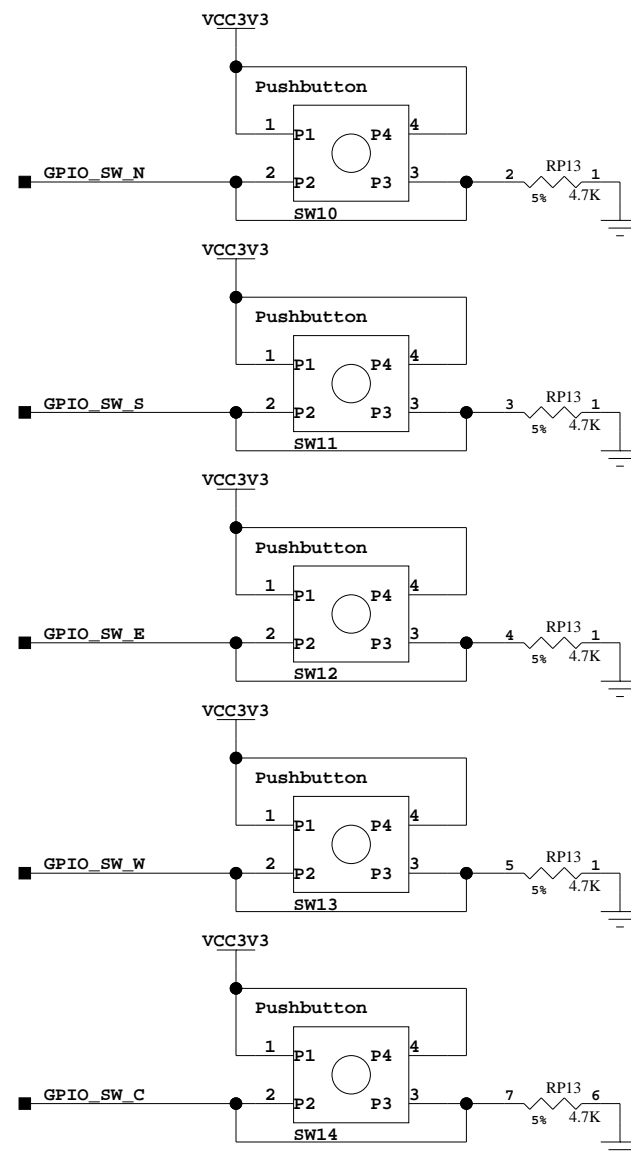
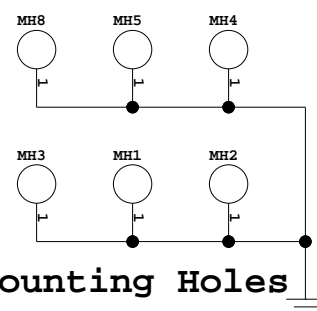
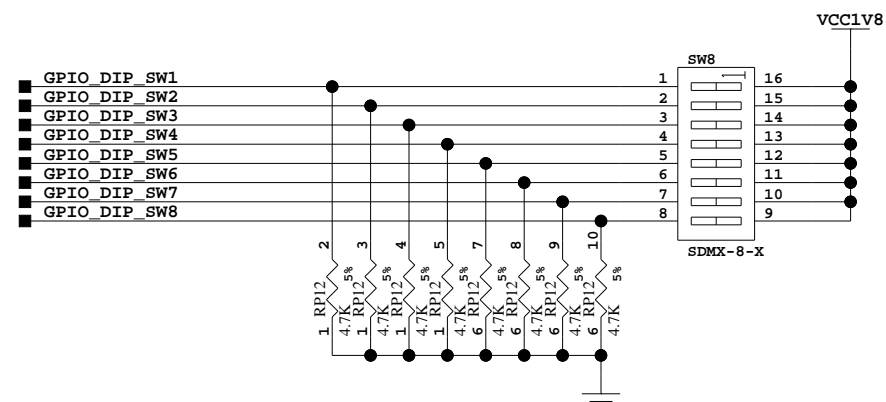
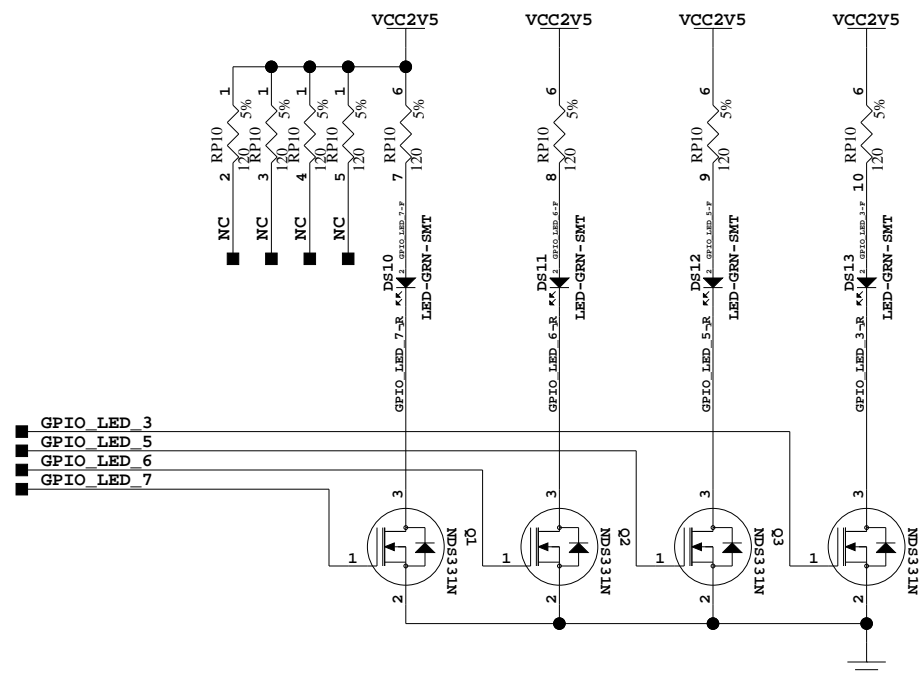
```
Misc Config
Platform Flash,
SPI Flash
```



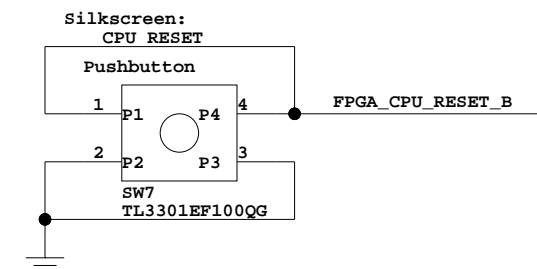
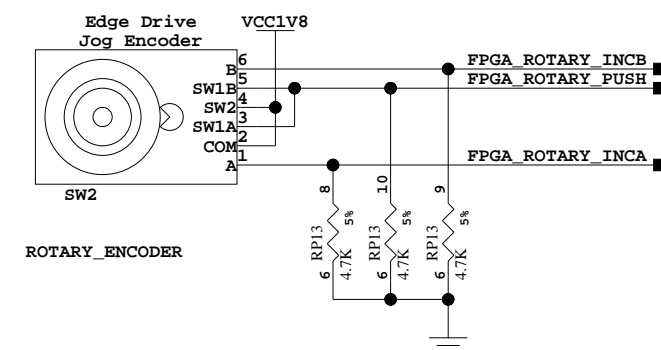
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Title:      Misc Config,Platform Flash, SPI Flash
           SCHEM, ROHS COMPLIANT
           ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415
           0381241
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Sheet Size: B		Rev:	02
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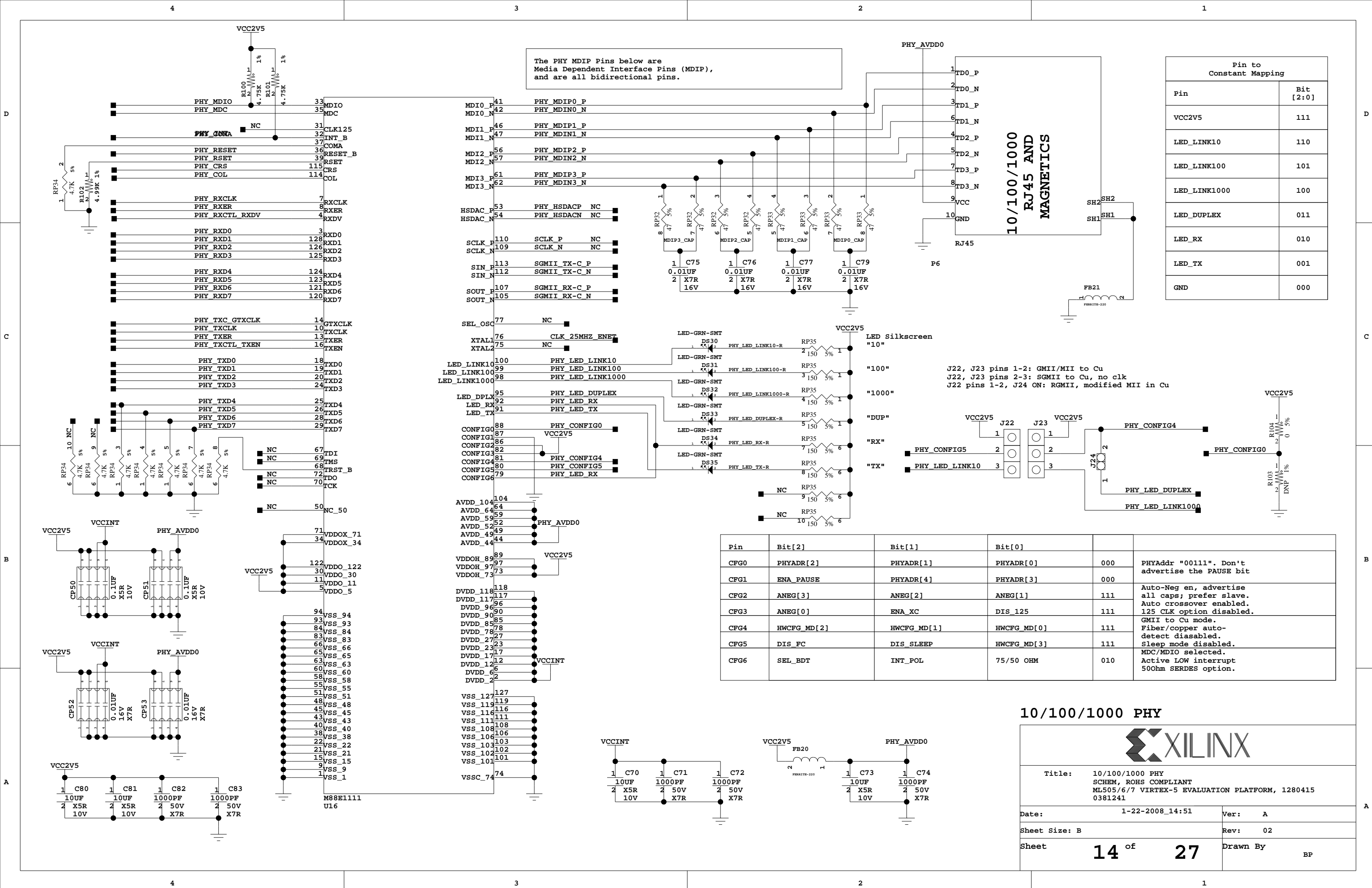
Edge Drive Jog Encoder Switch

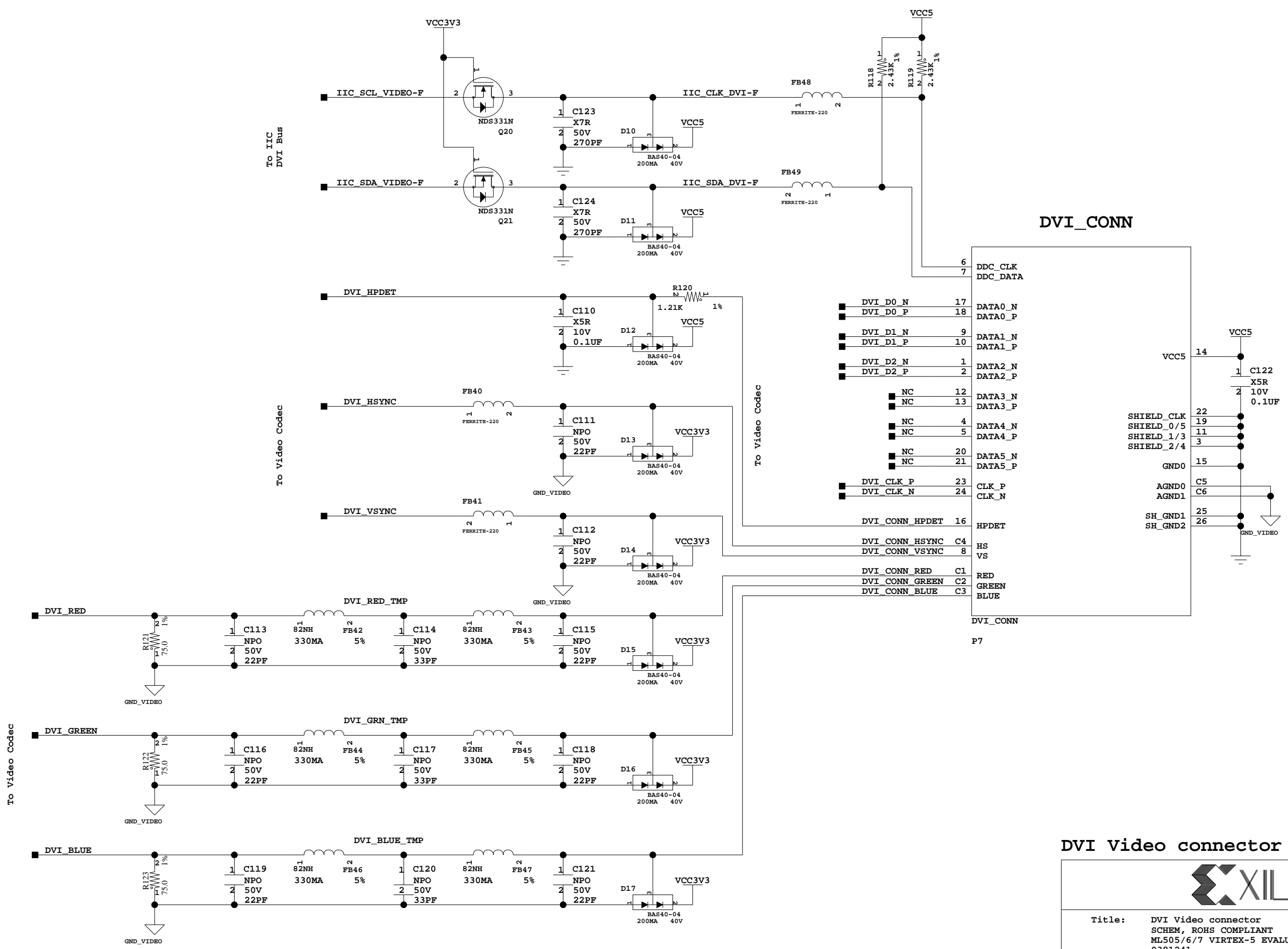


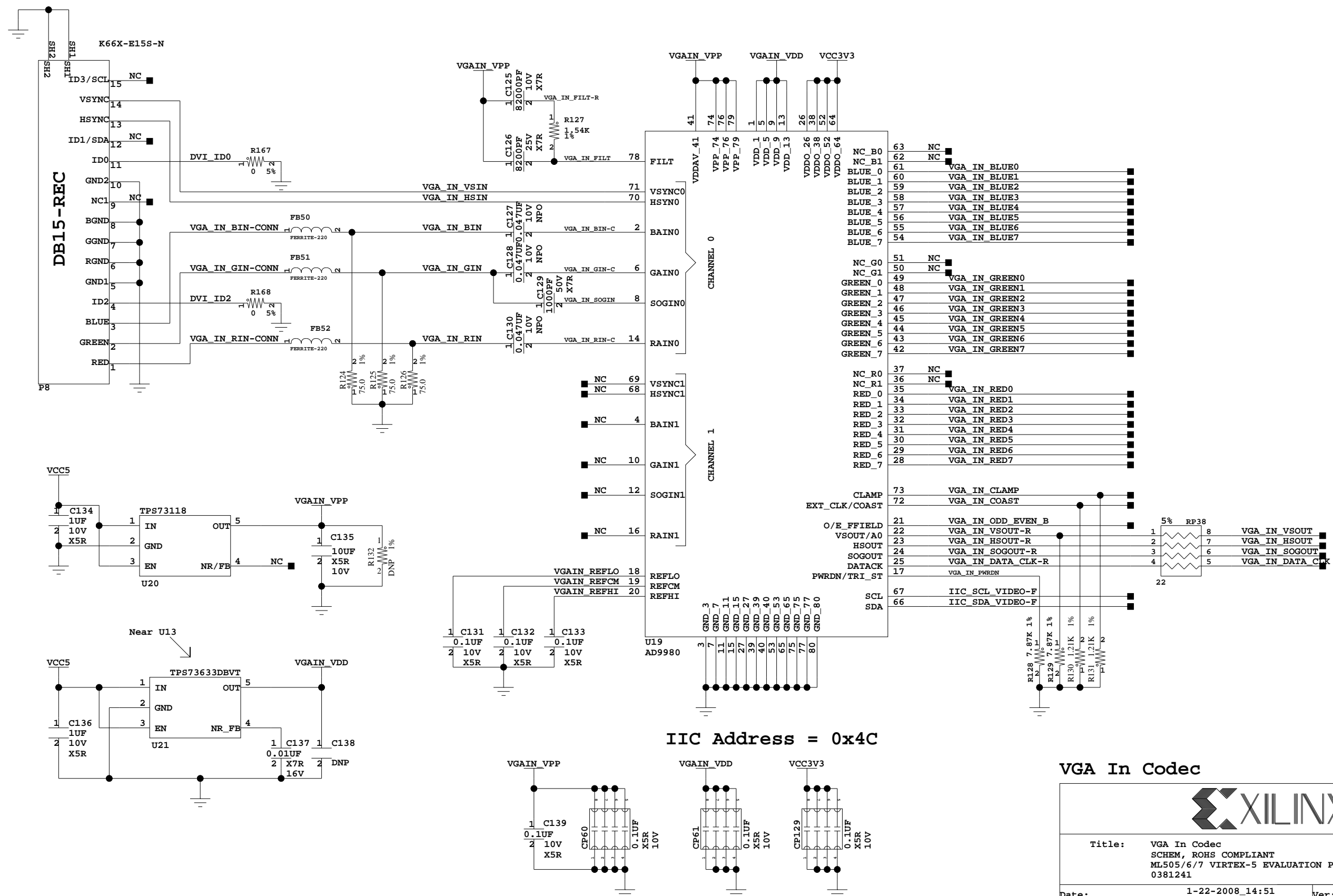
GPIO - Buttons, LEDs, Switches



Title: GPIO Buttons, LEDs, Switches GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
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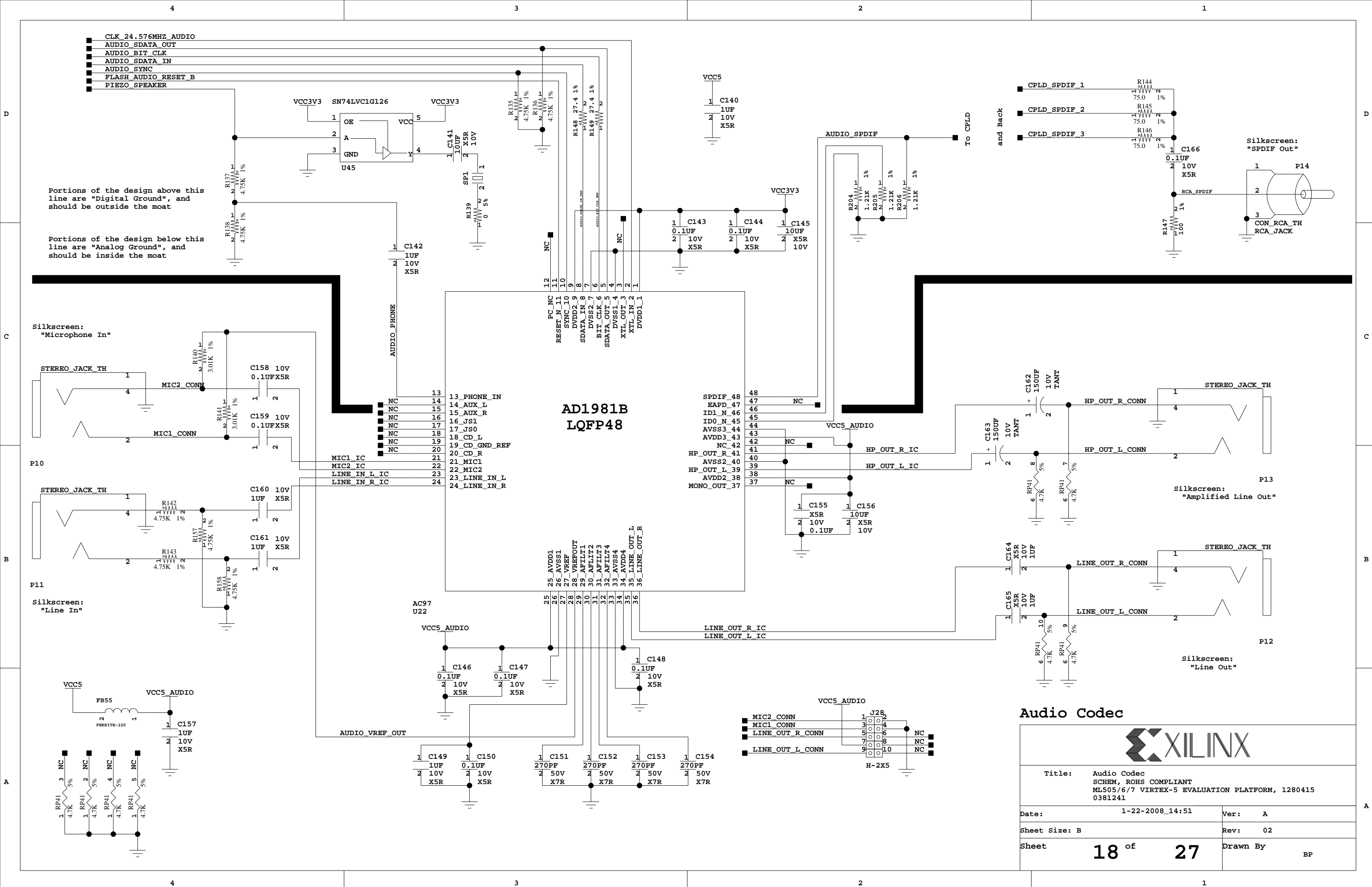




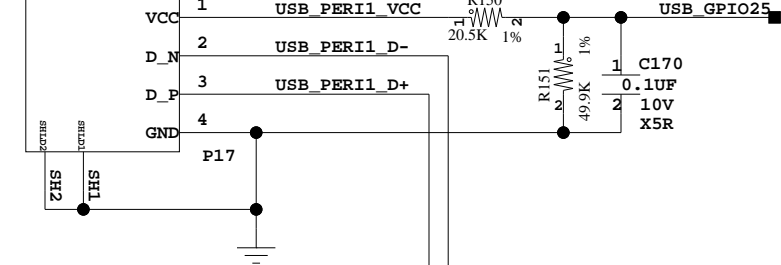
IIC Address = 0x4C

VGA In Codec

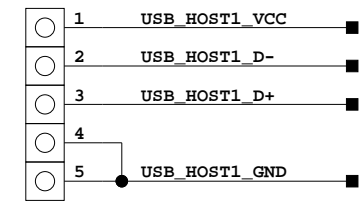
Title: VGA In Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241			
Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
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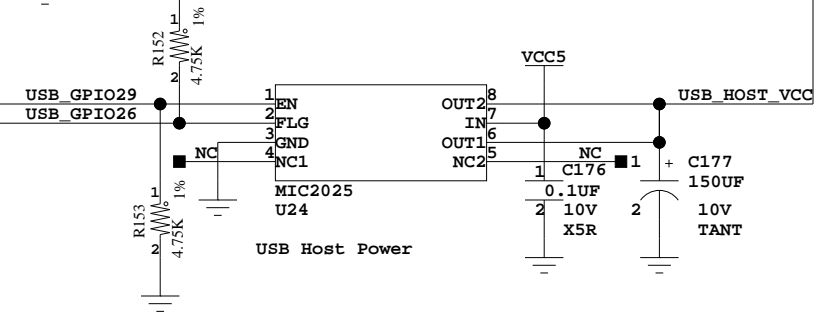
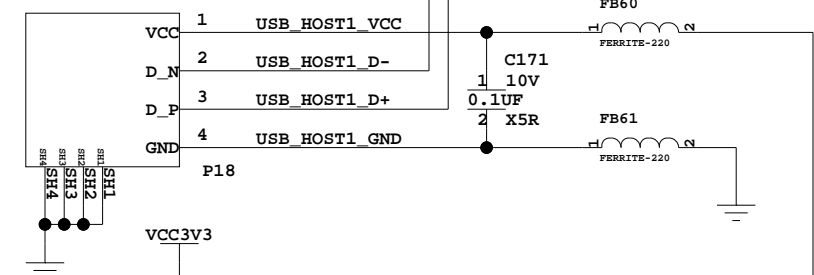
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USB_B_PERI_SMT



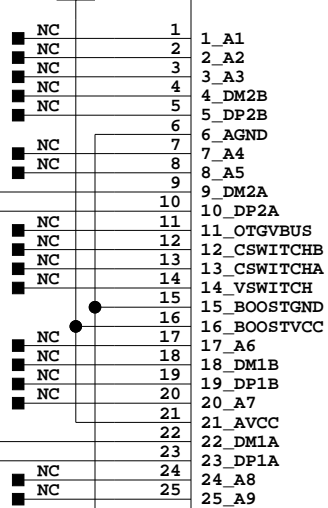
HDR1x5
J83



Silkscreen:
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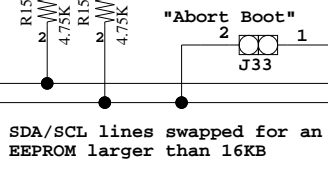
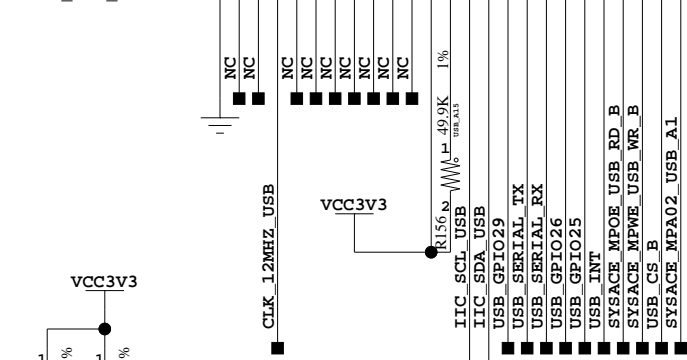
VCC3V3



CY7C67300-100AI

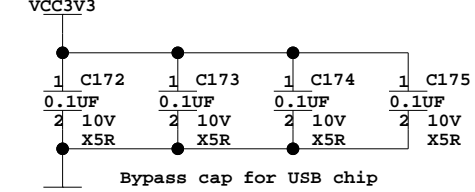
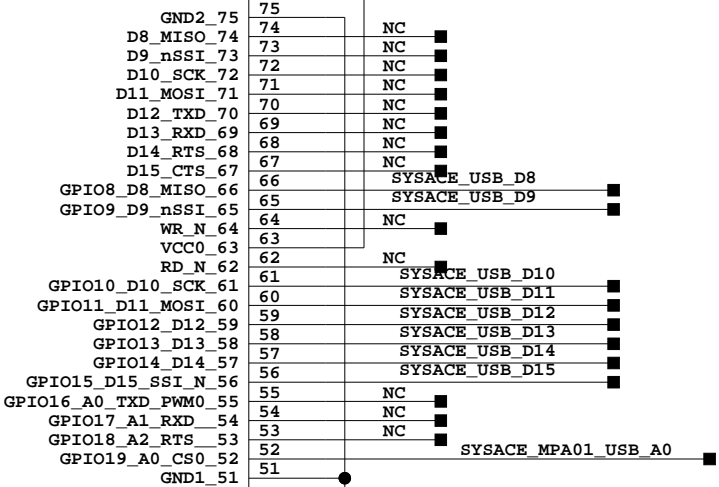
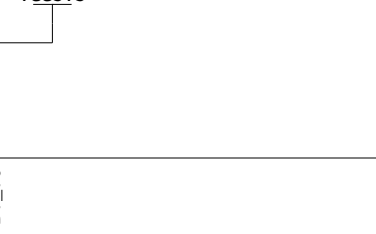
(DIE UP)

U23
CYP_USB_HOST



SDA/SCL lines swapped for an EEPROM larger than 16KB

VCC3V3

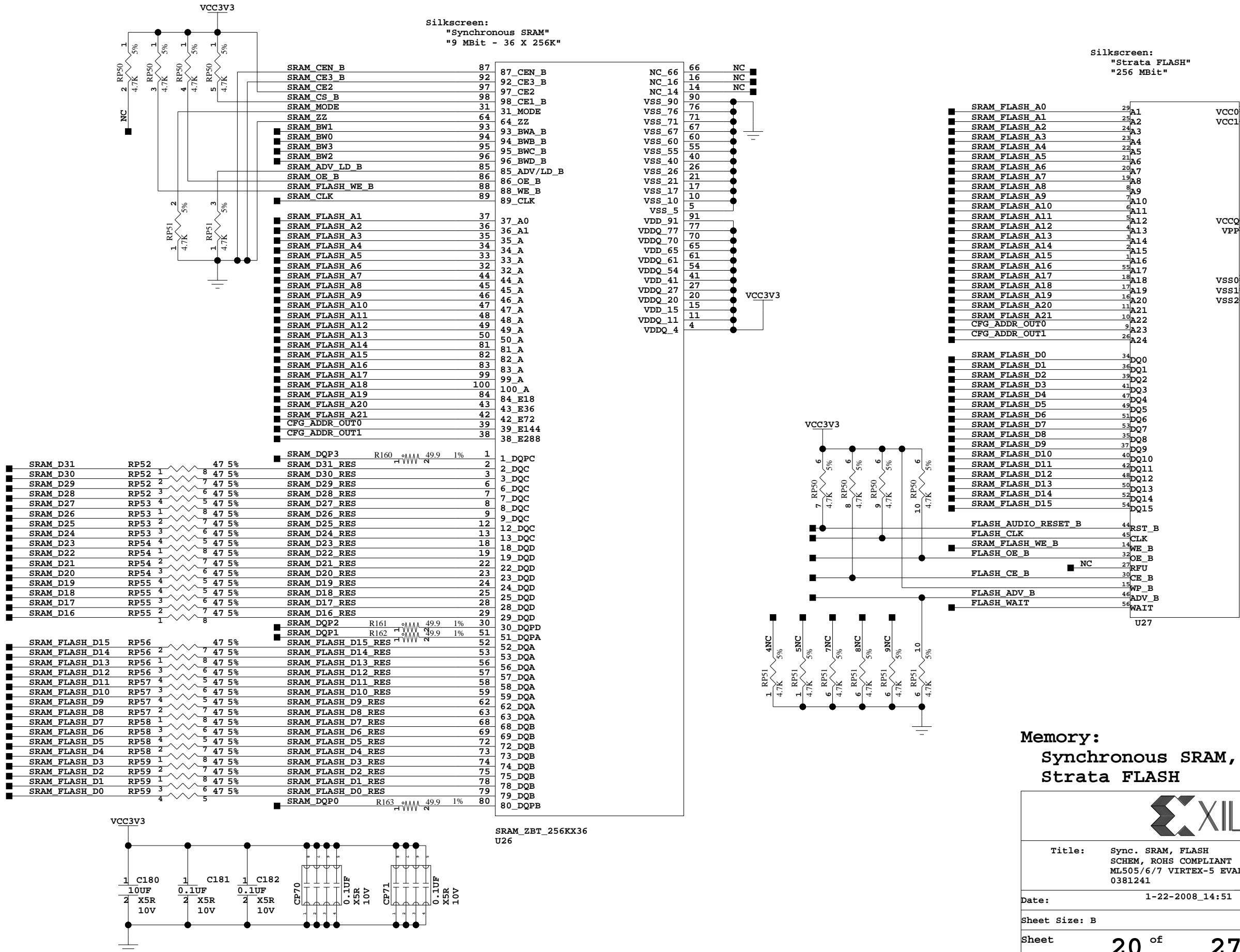


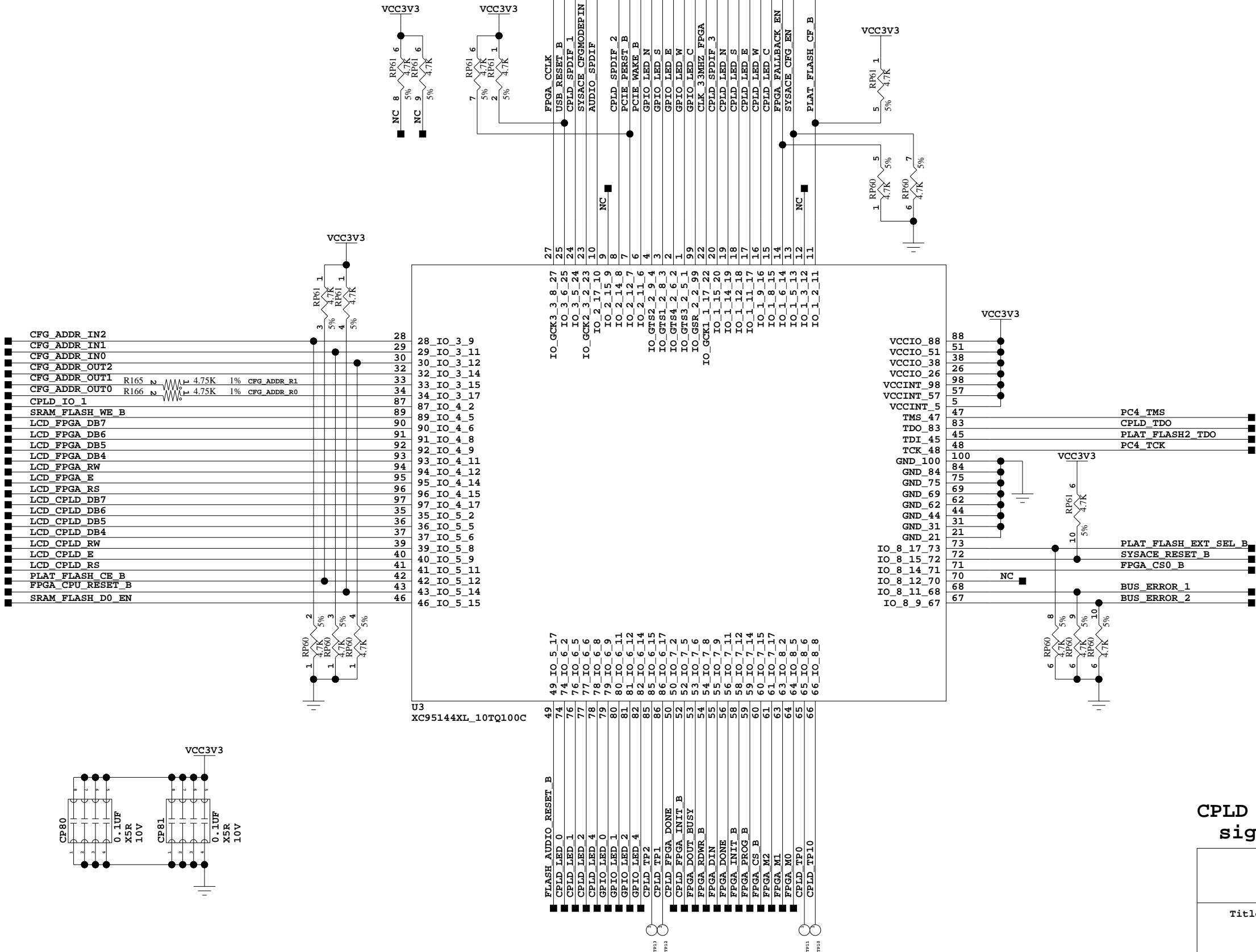
USB Controller



Title: USB Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
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The burst order mode of the SRAM is set to "Linear" by default



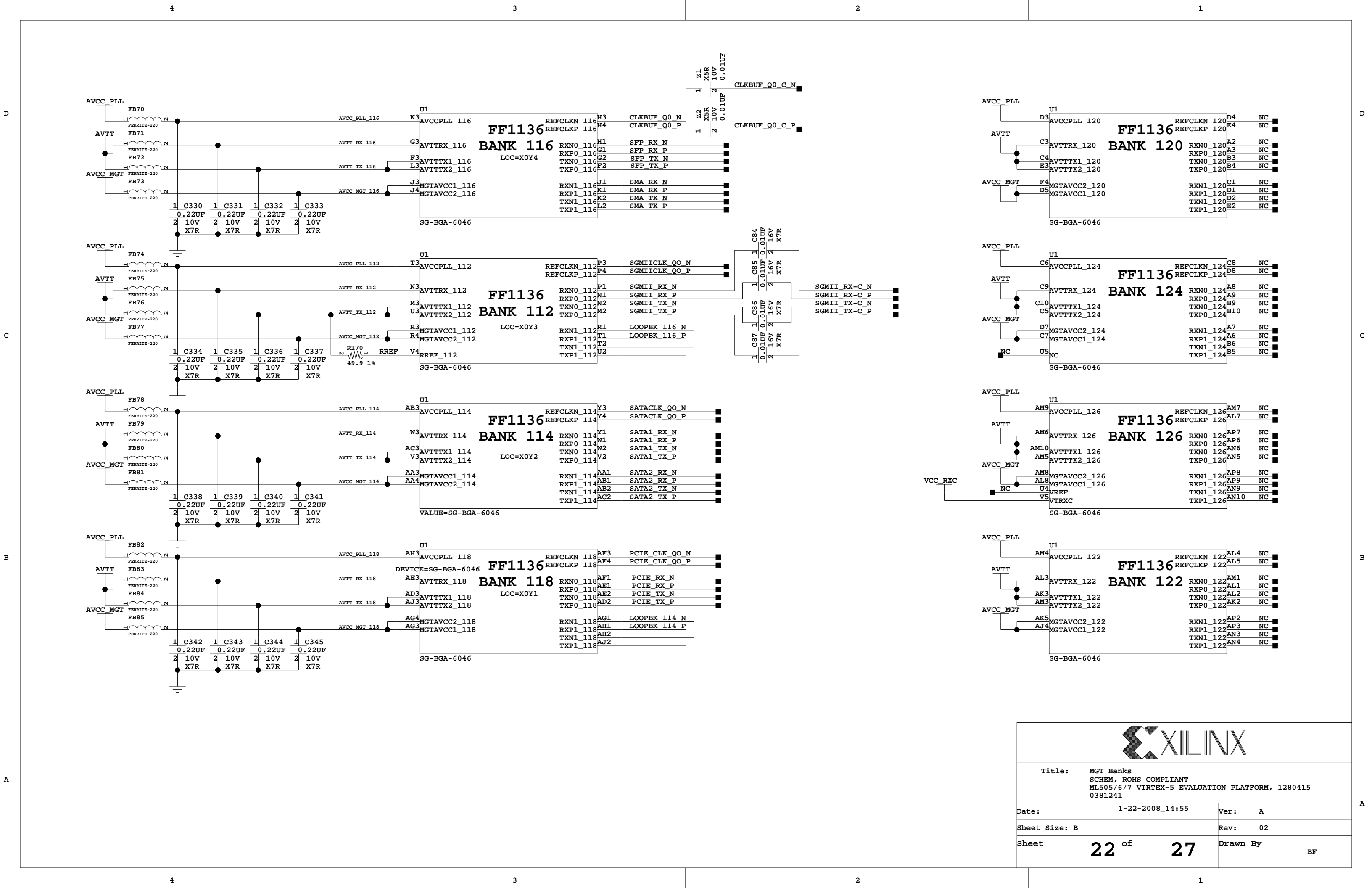


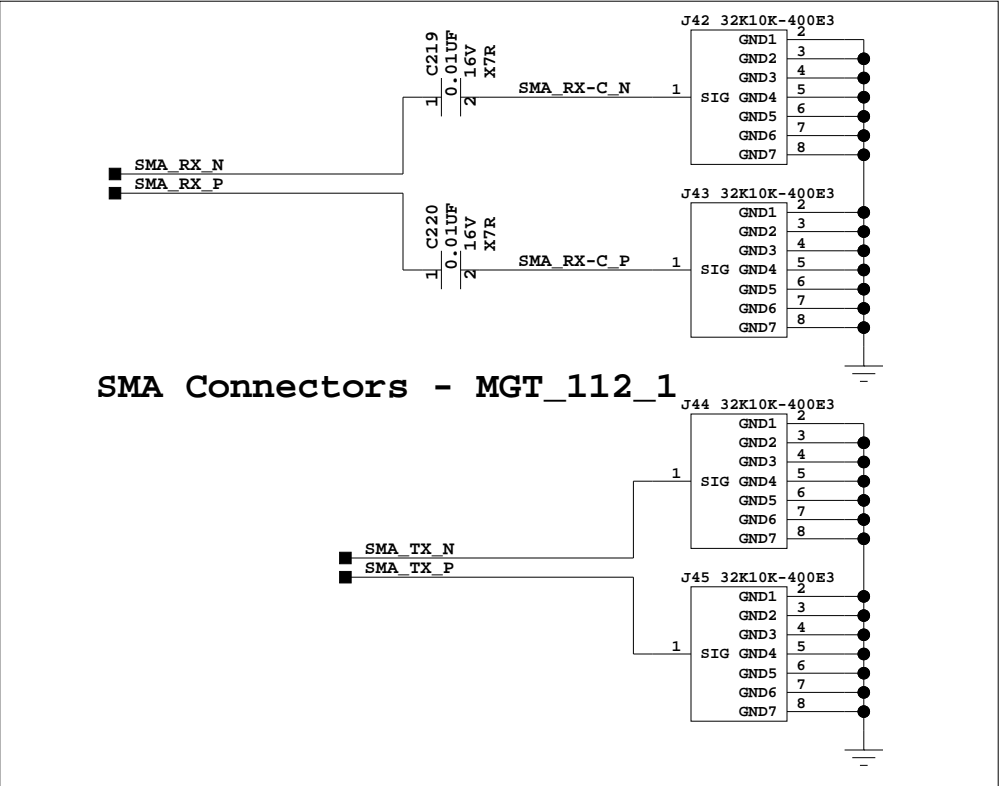
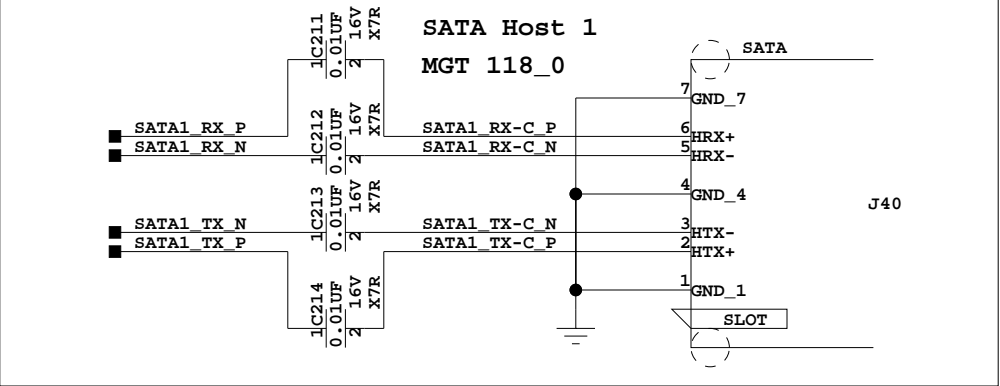
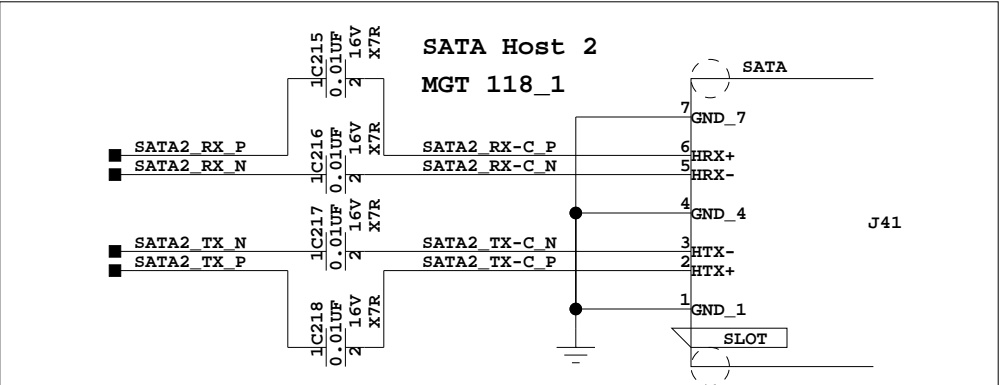
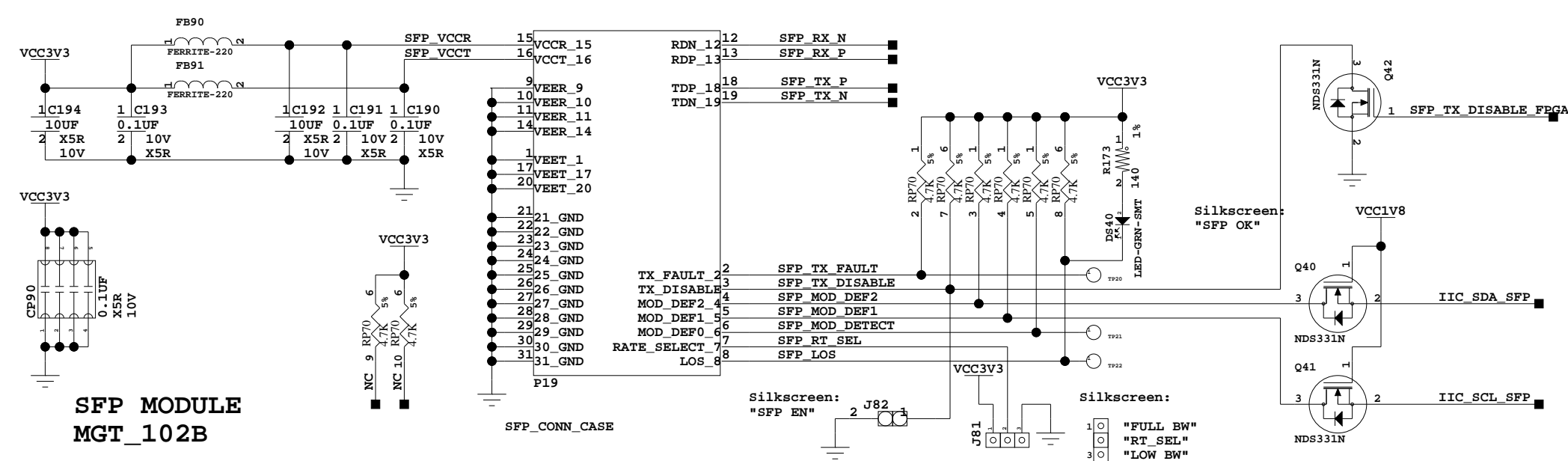
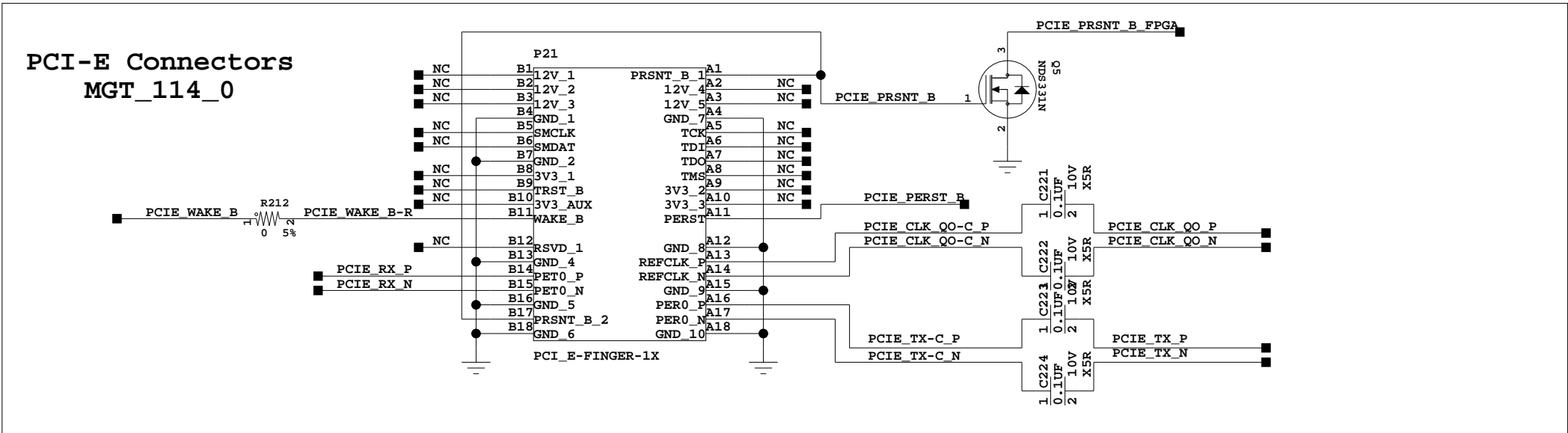
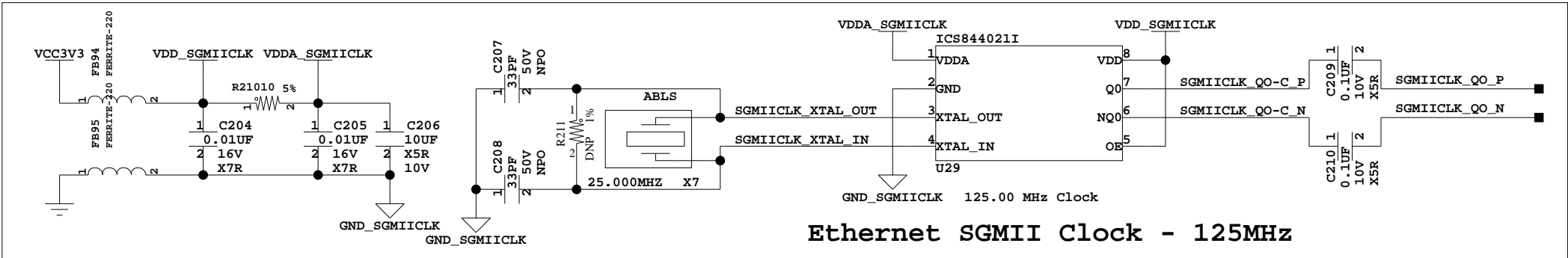
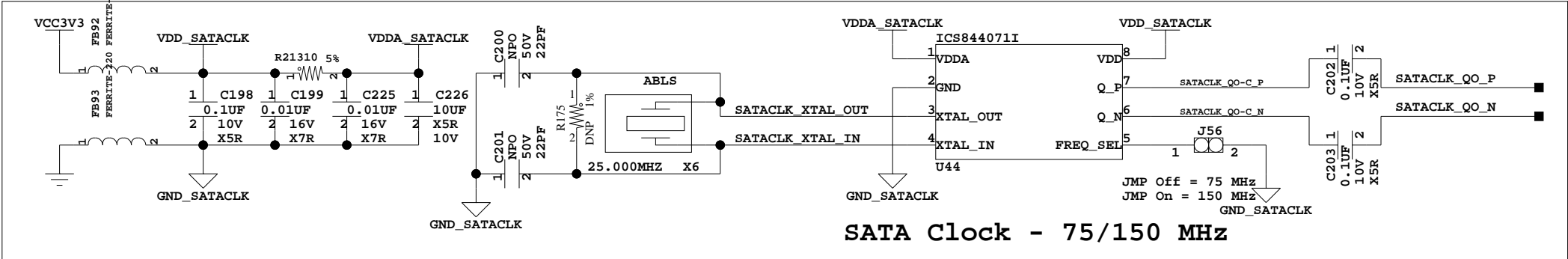
CPLD - Misc
signal control



Title: CPLD - Misc signal control
SCHEM, ROHS COMPLIANT
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

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MGT Clocks and Connectors

Title: MGT Connectors SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241			
Date: 1-22-2008_14:51	Ver: A		
Sheet Size: B	Rev: 02		
Sheet 23 of 27	Drawn By BF		

MGT PLL Regulator

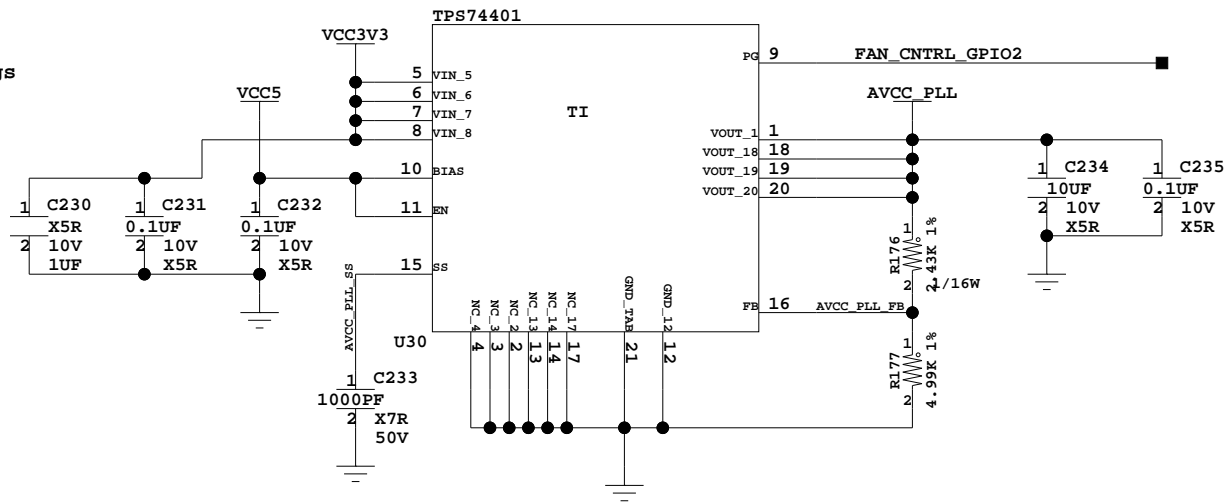
Voltage Output Settings

LXT & SXT (ML505/6)
AVCC_PLL = 1.2V @ 3A

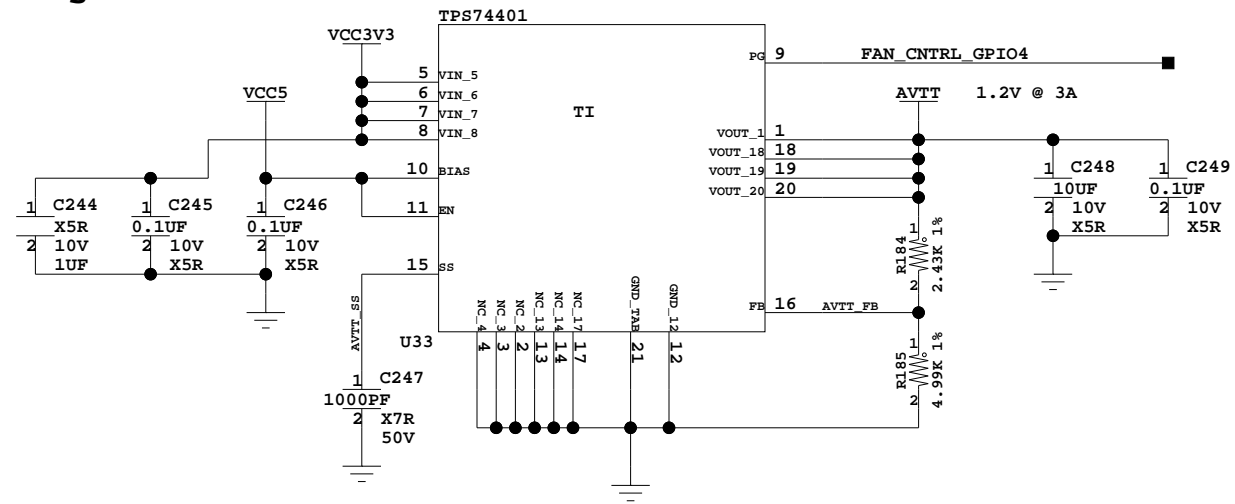
R176 = 2.43K 1%
R177 = 4.99K 1%

FXT Only (ML507)
AVCC_PLL = 1.0V @ 3A

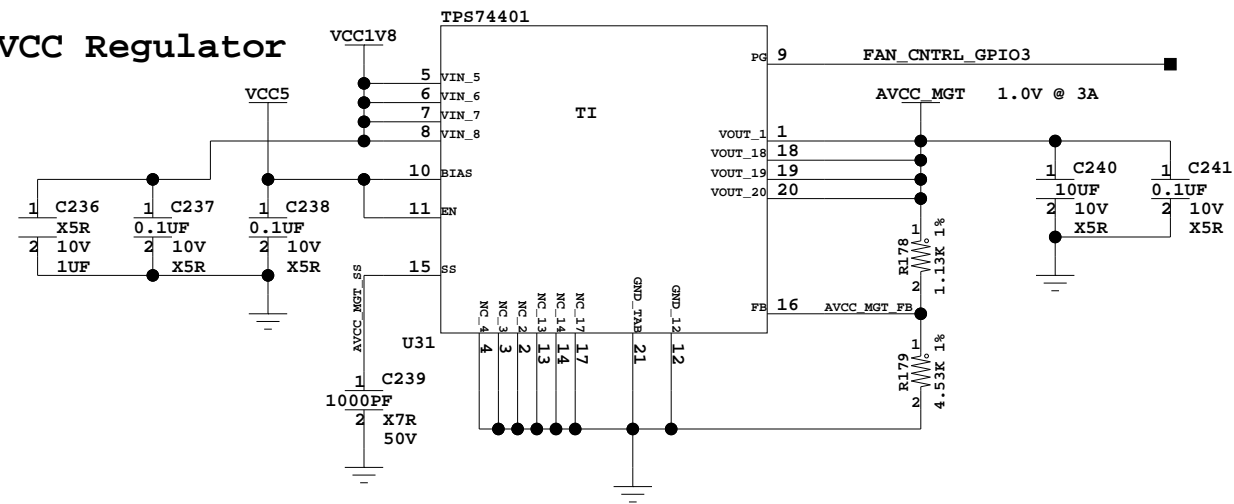
R176 = 1.13K 1%
R177 = 4.53K 1%



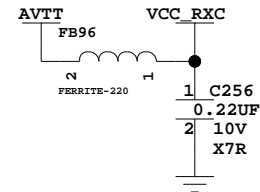
MGT VTT Regulator



MGT AVCC Regulator



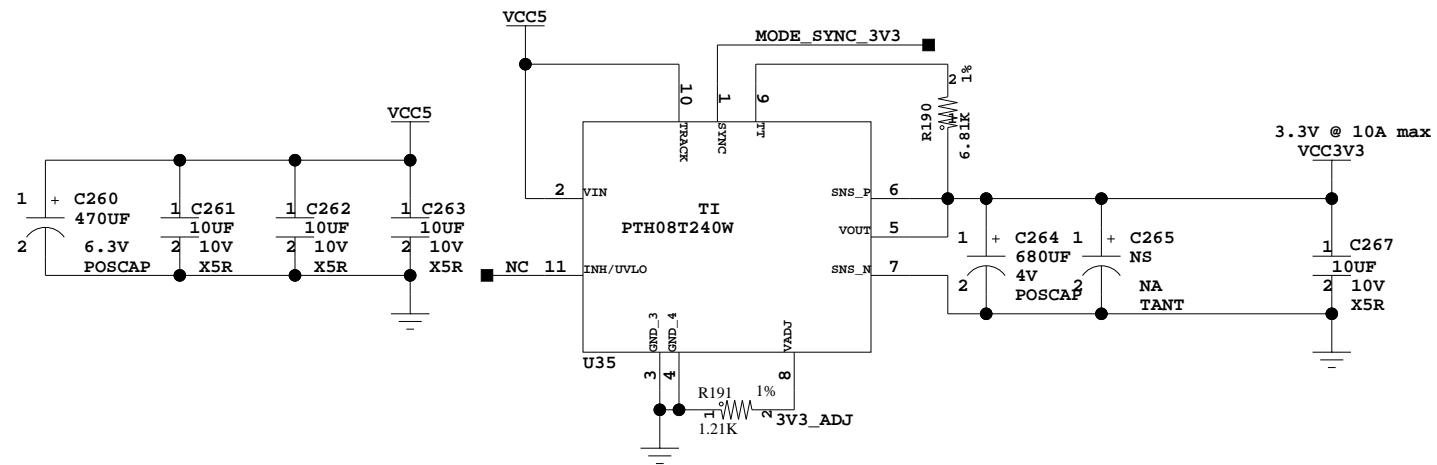
MGT RXC Regulator



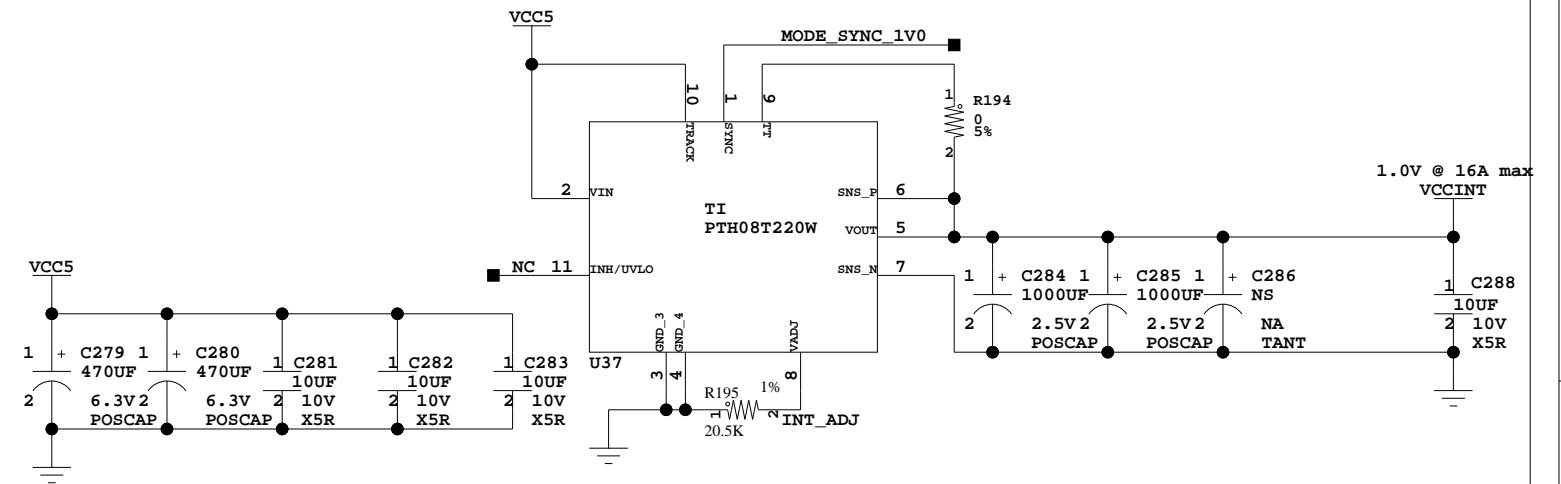
MGT Power Supplies

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Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
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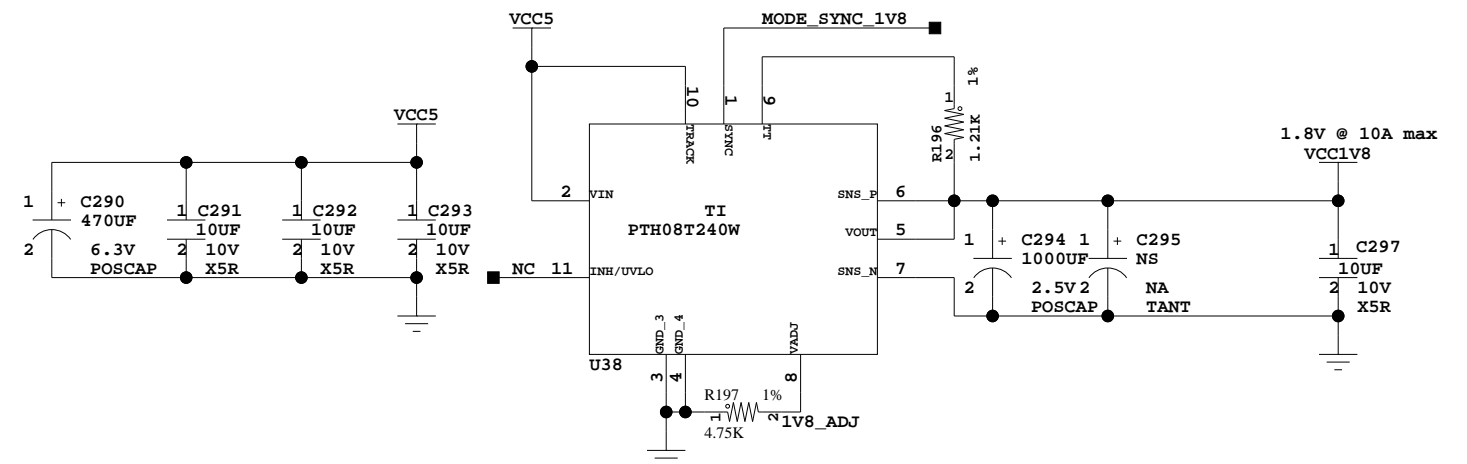
5v to 3.3V Regulator



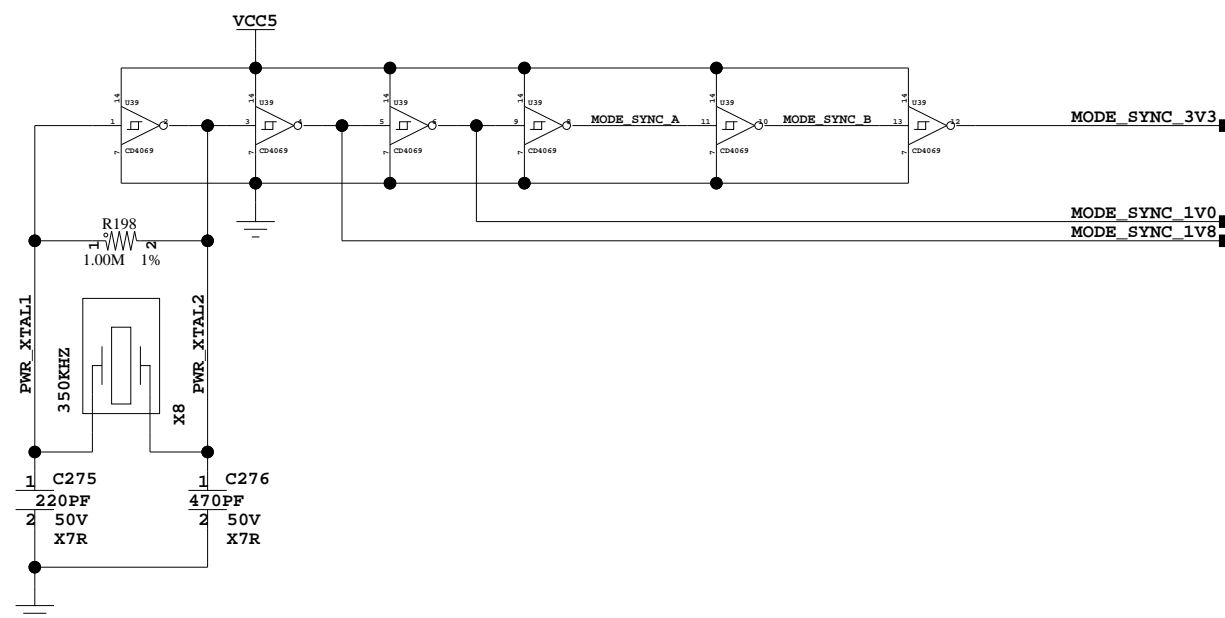
5v to 1.0V Regulator



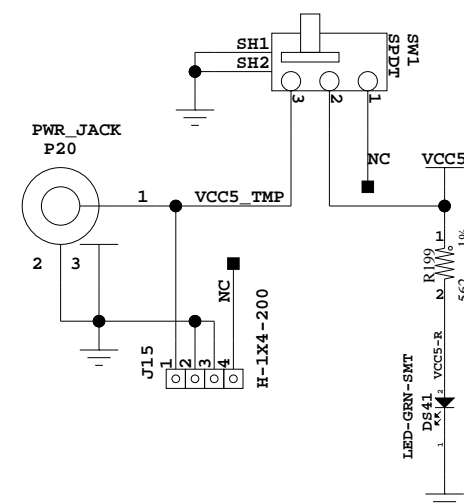
5v to 1.8V Regulator



5V Power Synchronizing Circuit



5V Power - Jack, Switch and LED



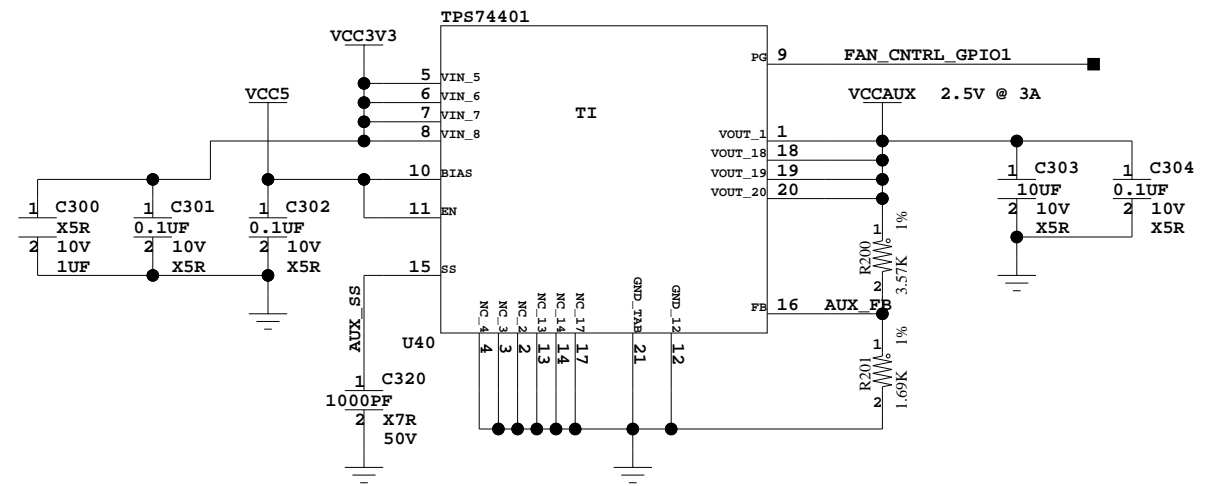
5V Power Supplies



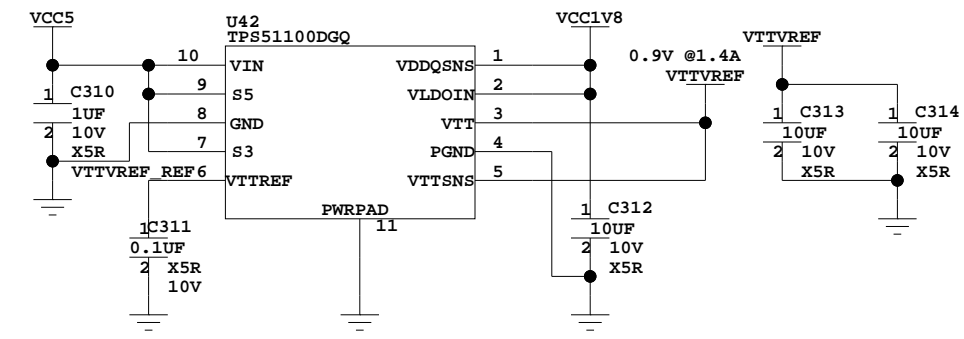
Title: Power Supplies
SCHEM, ROHS COMPLIANT
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
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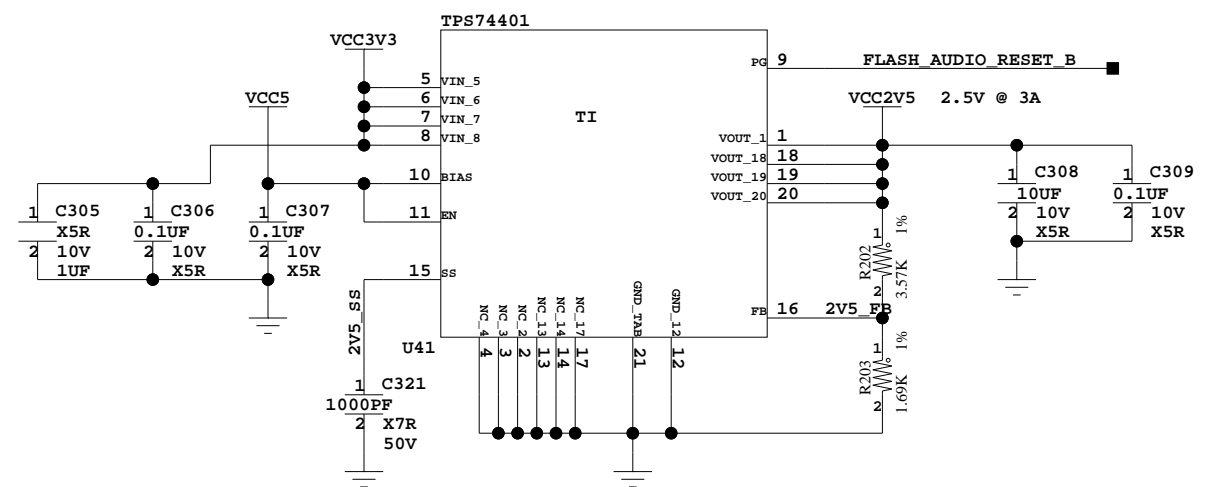
3.3v to 2.5V (VCC AUX) Regulator



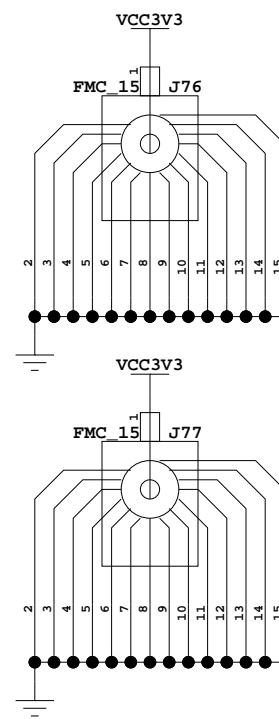
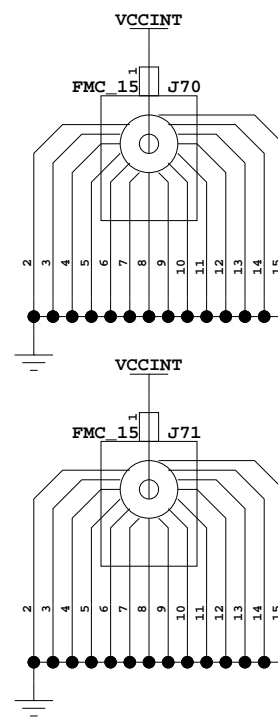
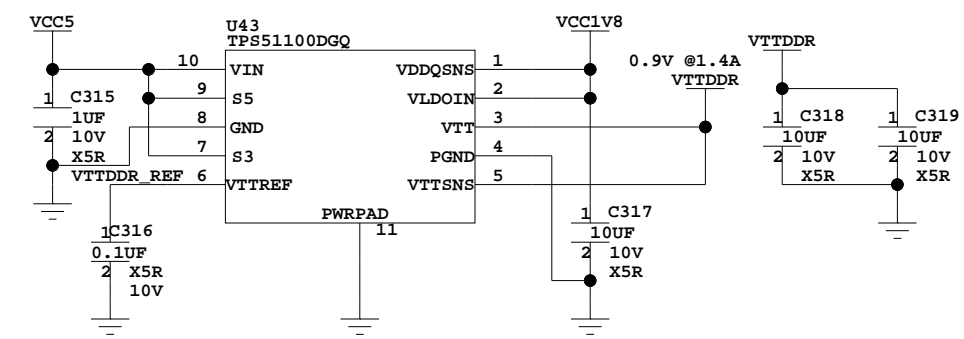
5V to 0.9V (DDR VTT VREF) Regulator



3.3v to 2.5V Regulator



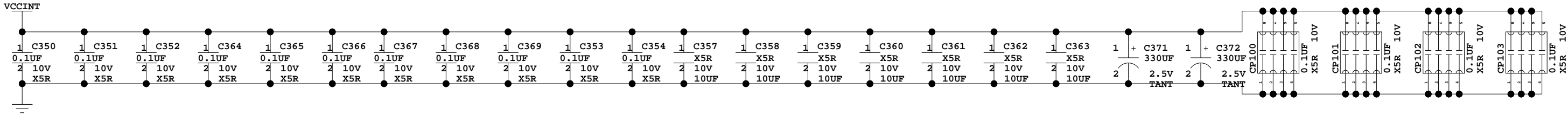
5V to 0.9V (DDR2 VTT DDR) Regulator



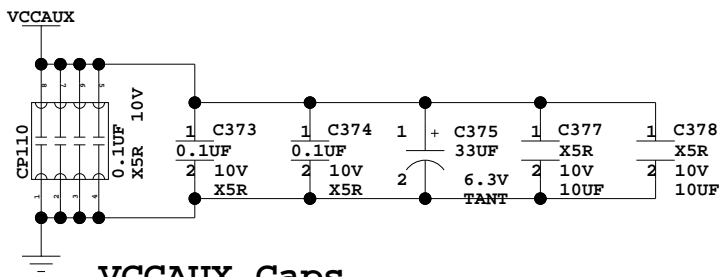
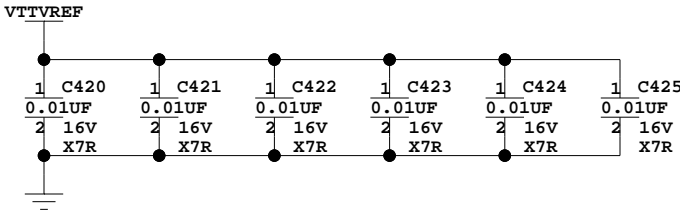
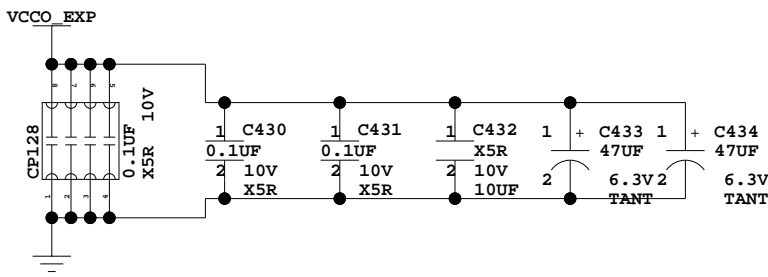
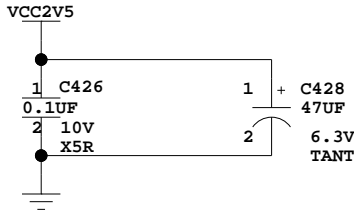
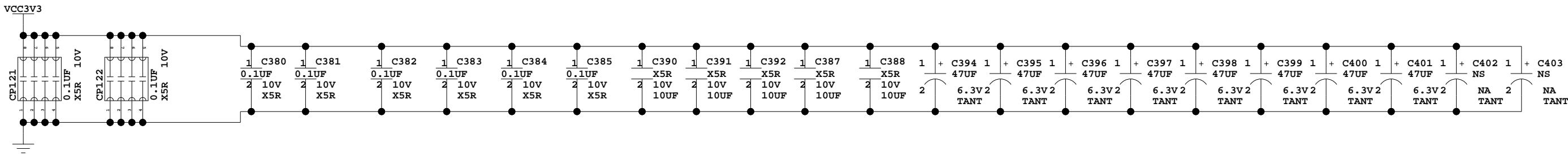
5V and 3.3V Power Supplies

Title: Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
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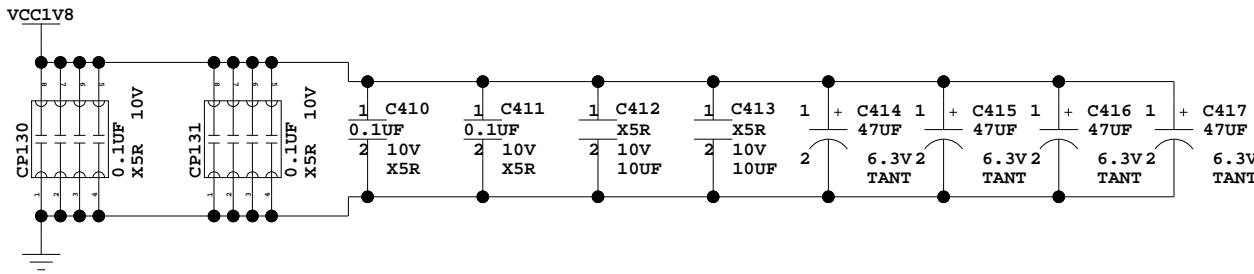
VCCINT Caps



VCCO Caps



VCCAUX Caps



Title: FPGA Decoupling SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 27 of 27	Drawn By BP