Virtex-5 FPGA Fibre Channel Protocol Standard

Characterization Test Report

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/14/07	1.0	Initial Xilinx release.

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Virtex-5 FPGA Fibre Channel Protocol Standard

Introduction

Virtex™-5 FPGA system connectivity technology delivers the lowest power solutions for building high-speed, high-bandwidth connections between devices, boards, and boxes. The RocketIO™ GTP transceiver design and SelectIO™ parallel I/O technologies enable flexible bridging between emerging serial standards and existing parallel standards. The features of the GTP transceivers in Virtex-5 FPGAs include:

- Current Mode Logic (CML) drivers/buffers with configurable termination, voltage swing, and coupling
- Programmable transmit pre-emphasis and receive equalization for optimal signal integrity
- Line rates from 500 Mb/s to 3.75 Gb/s with optional 5X oversampling for data rates from 100 Mb/s to 500 Mb/s
- Optional built-in Physical Coding Sublayer (PCS) features such as 8B/10B encoding/decoding, comma alignment, channel bonding, and clock correction
- Fixed latency modes for minimized, deterministic datapath latency
- Out-of-band signaling support (specifically designed to address the requirements of PCI Express® technology and Serial ATA protocols)
- Built-in pseudorandom bitstream (PRBS) generation/checking logic for easier bit error rate checking
- A configuration wizard provided in the CORE Generator™ tool and an internal bit error rate tester (IBERT) integrated into the ChipScope™ Pro tools for easy implementation of GTP transceiver interfaces

This characterization report compares the electrical performance of the GTP transceiver against the various Fibre Channel (FC) specifications (see "Appendix A: References," page 23) across process, voltage, and temperature conditions for 1 and 2 Gb/s operation. The GTP transceiver electrical characteristics were measured using a combination of lab bench setups and a High Volume Characterization (HVC) system. The methods used to characterize the transceiver are based on the standards specifications and also follow the best-practice methods for some parameters. A high-level description of GTP transceiver testing for the Virtex-5 LXT platform according to specifications from ANSI publications (INCITS T11.2) is also included.

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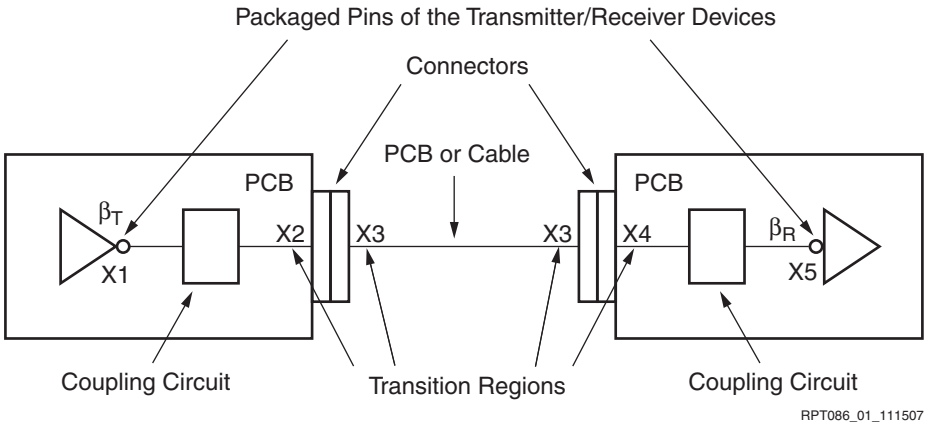
Background

The Fibre Channel standard references the test methodologies in ANSI publications. [Ref 1],[Ref 2] Figure 1 shows the test points in the Fibre Channel standard. X1 (TX output) and X5 (RX input) are standardized reference points used to certify component conformance. The electrical specifications of the physical medium dependent (PMD) service interface (X1 and X5) are not system compliance points. The specifications are not readily testable in a system implementation. The test specifications in this report refer to X1 and X5. The tests performed do not include an optical module described in the specification. The signal path is confined to the electrical domain and detailed test setups are described in the individual sections. The measurement setup contains additional PCB traces, connectors, and cables that can add additional jitter to the measurement. The GTP transceiver is an electrical, differential driver. Therefore, the test targeted the 100/200-DF-EL-S specification [Ref 1],[Ref 2], where:

- 100/200: 100 Mb/s (1.0625 Gb/s) or 200 Mb/s (2.125 Gb/s)
- DF: balanced copper
- EL: electrical
- S: short distance (< 100m)



Notes:

1. Termination can be placed in the coupling circuit or in the transmitter/receiver devices.
2. X*n* = Points of interest (X1 = β_T and X5 = β_R).

Figure 1: **Characterization Test Points**

Setup and Test Conditions

The following sections describe the equipment setup and test conditions in this characterization.

Lab Board Setup

A Xilinx ML523 evaluation board with an Oztek socket hosting the FF1136 package was used to test devices. A Xilinx bit error rate tester (XBERT), a GUI-based internal application, was used for dynamic reconfiguration port (DRP) loadings. The ChipScope™ analyzer was used to configure the device. Relevant attributes and/or port settings that were modified from their default values are listed in Table 1. For a complete listing of all the equipment used in this characterization, refer to "Appendix B: Test Equipment," page 23.

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Table 1: **Relevant Test Settings**

Attribute/Port Setting	200-DF-EL-S	100-DF-EL-S
AC_CAP_DIS (DC/AC)	TRUE	
Clock Source	Agilent 81130A	
Line Rates	2.125 Gb/s	1.0625 Gb/s
Loopback Mode	Far-end PMA (PMA Repeater Mode)	
PLL_DIVSEL_FB	2	
PLL_DIVSEL_REF	1	
PLL_RXDIVSEL_OUT	2	1
PLL_TXDIVSEL_COMM_OUT	1	
PLL_TXDIVSEL_OUT	1	
RCV_TERM_GND	FALSE	
RCV_TERM_MID	FALSE	
RCV_TERM_VTTX	FALSE	
REFCLK Frequency	106.25 MHz	106.25 MHz
RXEQ (on/off)	On	
RXEQMIX	`2'b11`	
Termination Scheme	External AC coupling	
VCO Frequency	1.0625 GHz	

Test Setup

Jitter tolerance measurements using a backplane, external random noise source, and sinusoidal modulation were performed using the test setup shown in Figure 2.

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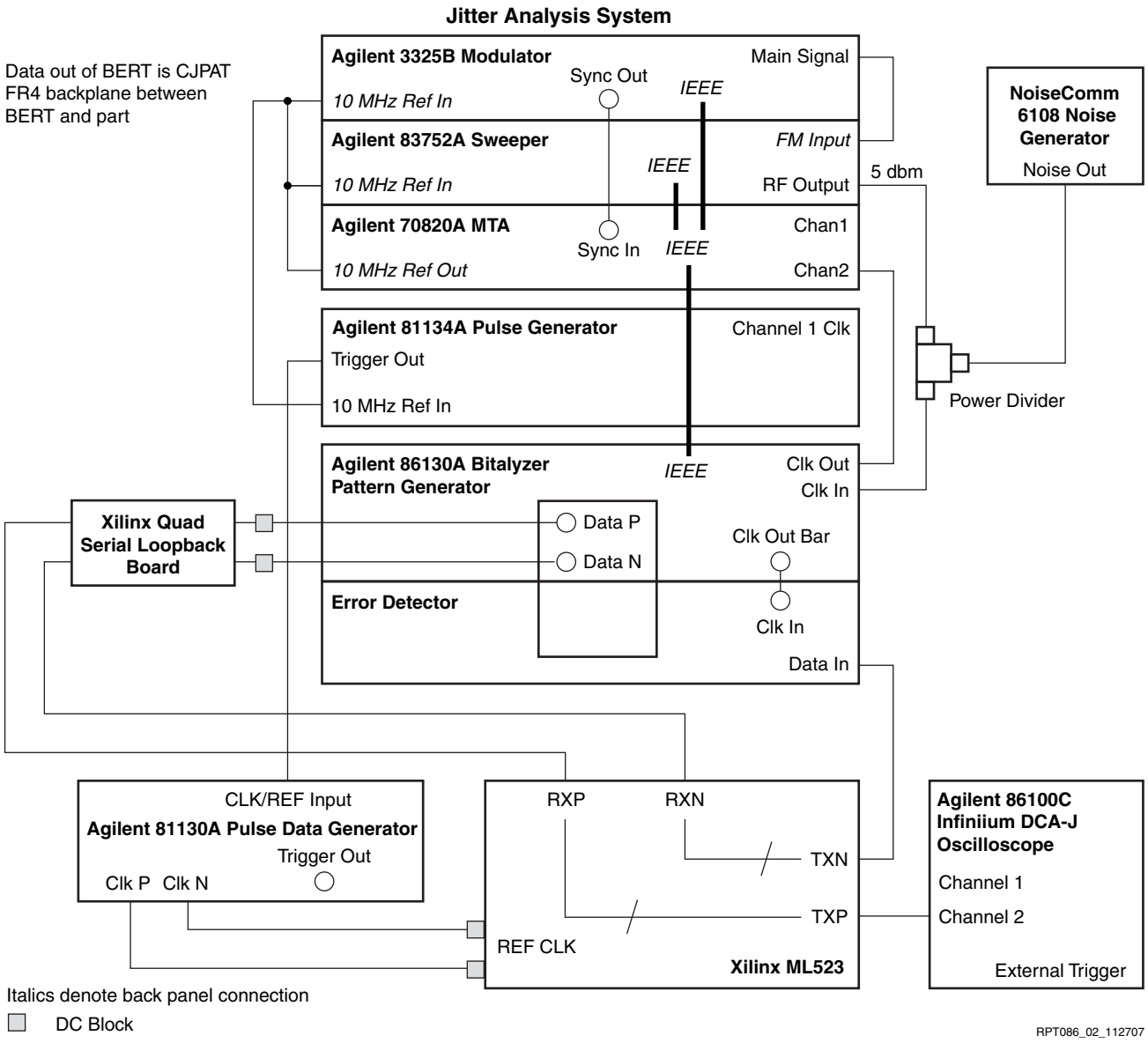

Figure 2: **Jitter Tolerance Setup of Virtex-5 FPGA GTP Transceiver with Media**

Jitter Test Components

For jitter tolerance tests at the bench level, the following test conditions were applied to add jitter components to the input datapath.

- The deterministic jitter (DJ) component was generated by passing the receive path data through the Xilinx quad serial loopback board before attaching to the DUT. The data-dependent deterministic jitter (DDJ or inter-symbol interference) was produced by the varying densities of High and Low bits of NRZ data as signals traveled through the bandwidth-limited backplane traces. FR4 trace boards with multiple trace length options were placed in the receive datapath for this purpose. The DJ through the backplane was measured using the CJPAT test pattern and the jitter decomposition function of the Agilent 86100C Infiniium DCA-J oscilloscope. The measurement with a backplane reflected the performance of both the receiver

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equalization and clock and data recovery (CDR) tracking capabilities because the equalization was turned on for these measurements.

- The random jitter (RJ) component was added to the pattern generator clock through a power splitter. The random noise was sourced from the NoiseCom random noise generator. The random noise was measured as the RMS value of signal jitter decomposition using the Agilent Infiniium DCA-J oscilloscope.
- The Agilent jitter analysis system was used for sinusoidal jitter modulation requirements.

Test Conditions

Table 2 and Table 3 show the operating supply voltages and operating temperatures, respectively.

Table 2: **Operating Supply Voltages**

Condition	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTRX (V)	MGTAVTTTX (V)
V_{MIN}	0.95	1.14	1.14	1.14
V_{NOM}	1.0	1.2	1.2	1.2
V_{MAX}	1.05	1.26	1.26	1.26

Notes:

1. Other FPGA voltages stay at their nominal values.

Table 3: **Operating Temperatures**

Condition	Temperature(1) (°C)
T_{MAX}	100
T_{ROOM}	25
T_{MIN}	–40

Notes:

1. Case temperature for bench measurements.

Summary of Results

Table 4 shows a summary of the results. Jitter tolerance was tested with a high amount of random jitter, which is the difference between deterministic jitter and total jitter (TJ). The jitter parameters were measured in unit intervals (UI).

Table 4: **Summary of Test Results for 1.0625 Gb/s and 2.125 Gb/s Specifications**

Parameter		FC 1.0625 Gb/s Specification	FC 2.125 Gb/s Specification	Test Results (1.0625 Gb/s)	Test Results (2.125 Gb/s)	Compliant
Jitter Output (UI)	TX DJ	0.11	0.2	0.077	0.125	Y
	TX TJ	0.23	0.33	0.159	0.27	Y
Jitter Tolerance (UI)	RX DJ	0.37	0.33	0.4	0.42	Y
	RX TJ	0.58	0.52	0.73	0.74	Y

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Receiver Electrical Tests

Total Jitter Tolerance at 200-DF-EL-S

Jitter tolerance measurements for the 200-DF-EL-S (2.125 Gb/s) Fibre Channel 2X line rate were performed using all three required jitter components: DJ, RJ, and sinusoidal jitter (SJ) added to the input datapath. Based on channel calibration, DJ and RJ components were fixed, and SJ modulation of a minimum of 0.1 UI was swept as a function of frequency.

Specification

Jitter tolerance specifications, which are defined in FC-PI-2, are shown in Table 5.

Table 5: **Jitter Tolerance Specification**

Interoperability Point(1)	Sinusoidal Jitter (UI Peak-to-Peak)	Deterministic Jitter (UI Peak-to-Peak)	Total (UI Peak-to-Peak)
β_R	0.1	0.33	0.52

Notes:

1. β_R is shown in Figure 1, page 4.

DJ and RJ Components

The DJ component was generated by passing the CJPAT test pattern through 60 inches of a standard FR4 trace board. The RJ component from the NoiseCom random noise source was added to the pattern generator clock source using a power splitter. With these two jitter sources in place, the jitter decomposition measurements were made using the Agilent Infiniium DCA-J oscilloscope, as shown in Figure 3. The 60 inches of trace board introduced 0.42 UI of DJ for this line rate. The random noise source was calibrated to add another 0.22 UI of peak-to-peak RJ. The sum of the DJ and RJ components was thus 0.64 UI.

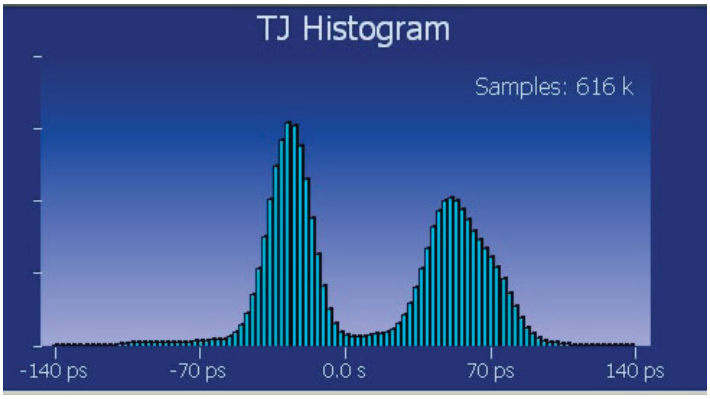

Figure 3: **Jitter Decomposition at 2.125 Gb/s over 60-inch FR4 Backplane Trace**

Passing Input with DJ and RJ Components

Figure 4 and Figure 5 show the passing signal on the Agilent Infiniium DCA-J oscilloscope and Agilent N4901B serial BERT 13.5 Gb/s, respectively.

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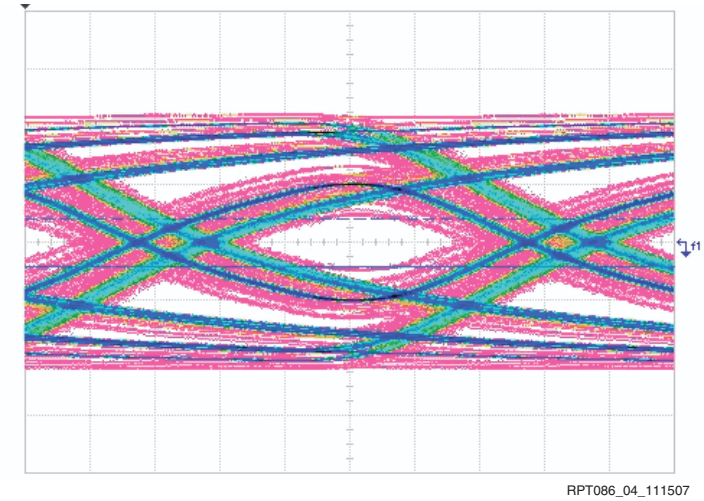

Figure 4: **Passing Input Eye with DJ and RJ Components**

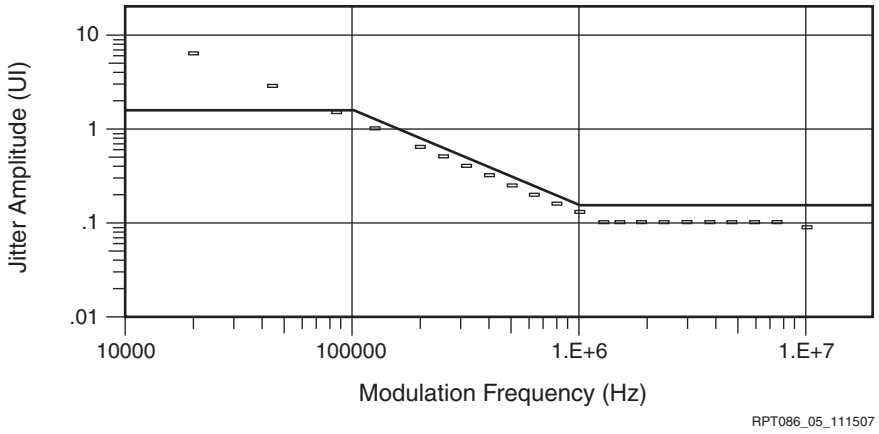

Figure 5: **Passing Sinusoidal Sweep over DJ and RJ Components**

Test Results

The test conditions and results in Table 6 show the minimum tolerance results for each test case. The decomposed DJ and RJ values were added to the minimum 0.1 UI of SJ for total jitter tolerance results.

Table 6: **Total Jitter Tolerance Test Conditions and Results at 2.125 Gb/s**

Device(1)	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	DJ (UI)	RJ (UI)	SJ (UI)	TJ (UI)
Typ-1, Typ-2, FF-1, FF-2, SS-1, SS-2	0.9	1.08	1.08	1.08	100	0.420	0.220	0.1	0.74
	1.0	1.2	1.2	1.2	25	0.420	0.220	0.1	0.74
	1.1	1.32	1.32	1.32	–40	0.420	0.220	0.1	0.74

Notes:

1. For all devices, data rate = 2.125 Gb/s, F_{REF} = 106.25 MHz, RXEQMIX = `2'b11`, pattern = CJPAT, and backplane = FR4 60 inches.

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Total Jitter Tolerance at 100-DF-EL-S

Jitter tolerance measurements of the 100-DF-EL-S (1.0625 Gb/s) Fibre Channel 1X line rate were performed using all three required jitter components (DJ, RJ, and SJ) added to the input datapath. Based on channel calibration, the DJ and RJ components were fixed, and SJ modulation of a minimum of 0.1 UI was swept as a function of frequency.

Specification

Jitter tolerance specifications, which are defined in FC-PI-2, are shown in Table 7.

Table 7: **Jitter Tolerance Specification**

Interoperability Point(1)	Sinusoidal Jitter (UI Peak-to-Peak)	Deterministic Jitter (UI Peak-to-Peak)	Total (UI Peak-to-Peak)
β_R	0.1	0.37	0.58

Notes:

1. β_R is shown in Figure 1, page 4.

DJ and RJ Components

The deterministic jitter component was generated by passing the CJPAT test pattern through 100 inches of a standard FR4 trace board. The random jitter component from the NoiseCom random noise source was added to the pattern generator clock source using a power splitter. With these two jitter sources in place, the jitter decomposition measurement were made using the Agilent Infiniium DCA-J oscilloscope, as shown in Figure 6. The 100 inches of trace board introduced 0.40 UI of DJ for this line rate. The random noise source was calibrated to add another 0.23 UI of peak-to-peak RJ. The sum of the DJ and RJ components was thus 0.63 UI.

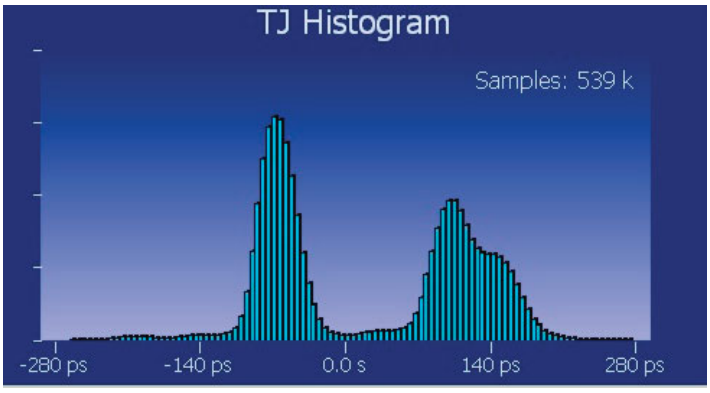

Figure 6: **Jitter Decomposition at 1.0625 Gb/s over 100-inch FR4 Backplane Trace**

Passing Input with DJ and RJ Components

Figure 7 and Figure 8 show the passing signal on the Agilent Infiniium DCA-J oscilloscope and Agilent N4901B serial BERT, respectively.

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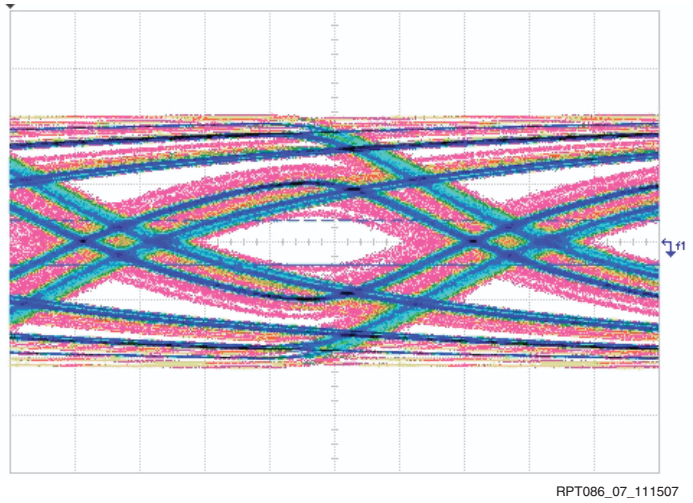

Figure 7: **Passing Input Eye with DJ and RJ Components**

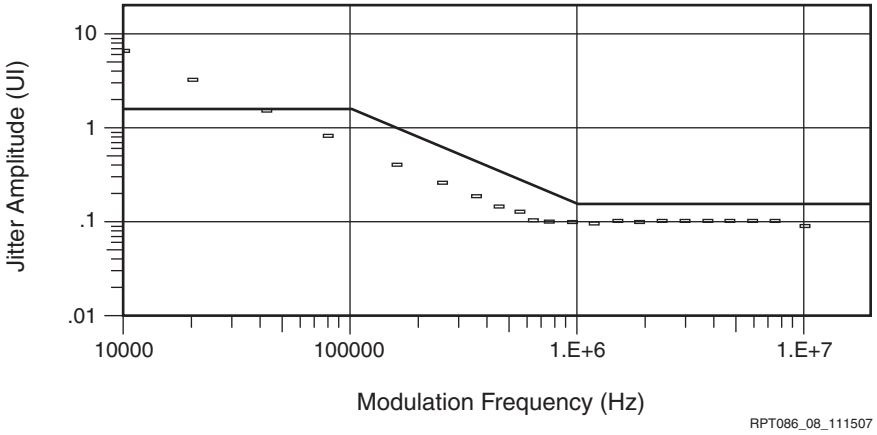

Figure 8: **Passing Sinusoidal Sweep over DJ and RJ Components**

Test Results

The test conditions and results in Table 8 show the minimum tolerance results for each test case. The decomposed DJ and RJ values were added to the minimum 0.1 UI of SJ for total jitter tolerance results.

Table 8: **Total Jitter Tolerance Test Conditions and Results at 1.0625 Gb/s**

Device(1)	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	DJ (UI)	RJ (UI)	SJ (UI)	TJ (UI)
Typ-1, Typ-2, FF-1, FF-2, SS-1, SS-2	0.9	1.08	1.08	1.08	100	0.420	0.220	0.1	0.74
	1.0	1.2	1.2	1.2	25	0.420	0.220	0.1	0.74
	1.1	1.32	1.32	1.32	–40	0.420	0.220	0.1	0.74

Notes:

1. For all devices, data rate = 2.125 Gb/s, F_{REF} = 106.25 MHz, RXEQMIX = `2'b11`, pattern = CJPAT, and backplane = FR4 60 inches.

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Lab Board Setup

An ML523 characterization platform with an Oztek socket hosting the FF1136 package was used to test the Virtex-5 XC5VLX50T device. XBERT was used to configure the GTP transceiver with Fibre Channel settings through the DRP. The ChipScope Pro analyzer was used to load the bit file to the XC5VLX50T device.

Test Setup

This set of tests used the same setup described in "Test Setup," page 5.

Receiver Input Sensitivity

Test Description

For each Fibre Channel line rate, a variable input voltage to the RX signal was applied to the GTP transceiver RX pins from the Agilent 13.5 Gb/s ParBERT generator. The BER test was performed to determine whether or not the test passed at a specific input voltage. RX input sensitivity is defined as the last passing input voltage before the pattern checker starts to indicate errors in the data received.

Test Equipment and Setup

Characterization of the Virtex-5 FPGA GTP transceiver was performed using HVC hardware. The HVC system comprises a 12-channel, 13.5 Gb/s ParBERT system with integrated signal generators, power supplies, and removable test fixture interface. Temperature control was achieved through forced air cooling/heating using a Thermonics unit. A test fixture was developed for the FF1136 package to use for both XC5VLX50T and XC5VLX110T devices. Twelve GTP transceiver channels were characterized in a single pass.

Results

The data measured from the RX input sensitivity test is provided for each Fibre Channel line rate in this section. Table 9 shows the test conditions and results summary.

Table 9: **RX Sensitivity Test Conditions and Results Summary**

	Description
Test Case	RX sensitivity, differential peak-to-peak (mV).
Conditions	V_{CC} = NOM ± 5%, Temperature = –40°C to 100°C (I-grade).
Method	RX input voltage was programmed from 400 mV to 0 mV in 5 mV steps until the pattern checker indicated errors in the data received.
Data Rates Tested	2.125 Gb/s and 1.0625 Gb/s.

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Table 9: **RX Sensitivity Test Conditions and Results Summary *(Continued)***

	Description		
	Parameter	RX Sensitivity (mVppd)	
		2.125 Gb/s	1.0625 Gb/s
Results	Median	75.00	75.00
	Average	79.75	73.84
	Standard Deviation	15.19	15.56
	Minimum	45.00	30.00
	Maximum	135.00	120.00

In Figure 9 and Figure 10, the RX sensitivity data distributions from the test results are plotted as histograms across process, temperature, and voltage for both Fibre Channel line rates.

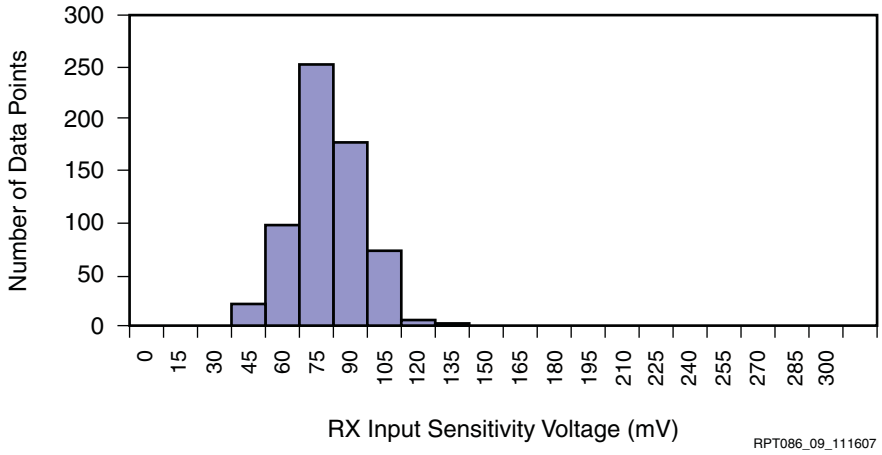

Figure 9: **RX Sensitivity Histogram at 2.125 Gb/s**

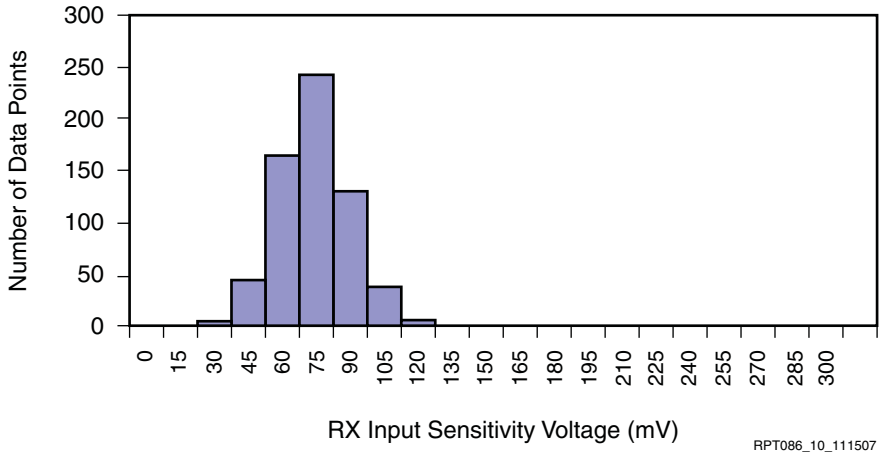

Figure 10: **RX Sensitivity Histogram at 1.0625 Gb/s**

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Transmitter Electrical Tests

Output Jitter Tests for 100-DF-EL-S and 200-DF-EL-S

Specification

Jitter tolerance specifications, which are defined in FC-PI-2, are shown in Table 10.

Table 10: **Output Jitter Specification**

FC Line Rate	Interoperability Points(1)	Deterministic Jitter (UI Peak-to-Peak)	Total (UI Peak-to-Peak)
100-DF-EL-S	β_T	0.11	0.23
200-DF-EL-S	β_T	0.20	0.33

Notes:

1. β_T is shown in Figure 1, page 4.

Test Description

Jitter generation measurements of the GTP transmitter output were performed at the two Fibre Channel line rates of 2.125 Gb/s and 1.0625 Gb/s by the bathtub curve (BTC) method whereas the random jitter component was extrapolated to 10^{-12} BER to determine the transmitter's total output jitter.

Test Equipment and Setup

Characterization of the Virtex-5 FPGA GTP transceiver was performed using HVC hardware. The HVC system comprises a 12-channel, 13.5 Gb/s ParBERT system with integrated signal generators, power supplies, and removable test fixture interface. Temperature control was achieved through forced air cooling/heating using a Thermonics unit. A test fixture was developed for the FF1136 package to use for both XC5VLX50T and XC5VLX110T. Twelve GTP transceiver channels were characterized in a single pass.

Board Setup and Clock Connections

The device was configured using ChipScope analyzer. Power was supplied from eight programmable power supplies through connectors on the side of the fixture. High-speed connections from the device to the ParBERT system were made through SMP and SMA coaxial connectors. Blind-mate connectors were used to permit quick removal of the test fixture. A low-profile, high-speed Altanova socket was used to collect the data. Two pairs of reference clock inputs were used to clock the six GTP_DUAL tiles in two groups of three GTP_DUAL tiles each.

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Test Conditions

Table 11 and Table 12 show the dynamic and static test conditions, respectively.

Table 11: **Dynamic Test Conditions**

Temp (°C)	Voltage
–40	–5%
	NOM
	+5%
0	–5%
	NOM
	+5%
100	–5%
	NOM
	+5%

Notes:

1. All supply voltages were adjusted together. Nominal voltages are as shown in Table 2, page 7.

Table 12: **Static Test Conditions**

Supply	Use	Nominal Voltage (V)
MGTAVCC	GTP transceiver main supply.	1.0
MGTAVCCPLL	GTP transceiver supply for the PLL, low noise.	1.2
MGTAVTTRX	GTP RX supply.	1.2
MGTAVTTRXC	GTP RX supply used to maintain termination resistor calibration when the GTP transceiver is powered down. Always on.	1.2
MGTAVTTTX	GTP TX supply.	1.2
V_{CCAUX}	FPGA auxiliary supply voltage relative to GND, low noise.	2.5
V_{CCINT}	FPGA main supply voltage relative to GND. Also used for the PCS of the GTP transceiver.	1.0
V_{CCO}	FPGA I/O drivers supply voltage relative to GND.	2.5

Notes:

1. All GTP transceiver supplies use L/C passive filtering. See the *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for details. [Ref 4]

Test Setup and Details

Characterization was performed using HVC over process, voltage, and temperature corners. All 12 GTP transceivers on each unit were tested. The numbers of test case instances are shown in the data collection plots. The test designs use loopback in 1-byte mode with both TXUSRCLK/TXUSRCLK2 and RXUSRCLK/RXUSRCLK2 clocked from

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TXOUTCLK. The configuration provides connections to GTPRESET, RXCDRRESET, and the DRP signals.

The data flow through the GTP transceiver is shown in Figure 11. Serial data to the RX was provided by the Agilent 13.5 Gb/s ParBERT generator. This data was converted to 10-bit data at the PMA deserializer and passed through the PCS. The RX parallel data port was connected to the TX parallel data port in the FPGA logic. The 10-bit parallel data was then sent through the TX PCS and converted back to serial data at the TX PMA. The TX serial data was connected to the 13.5 Gb/s ParBERT analyzer.

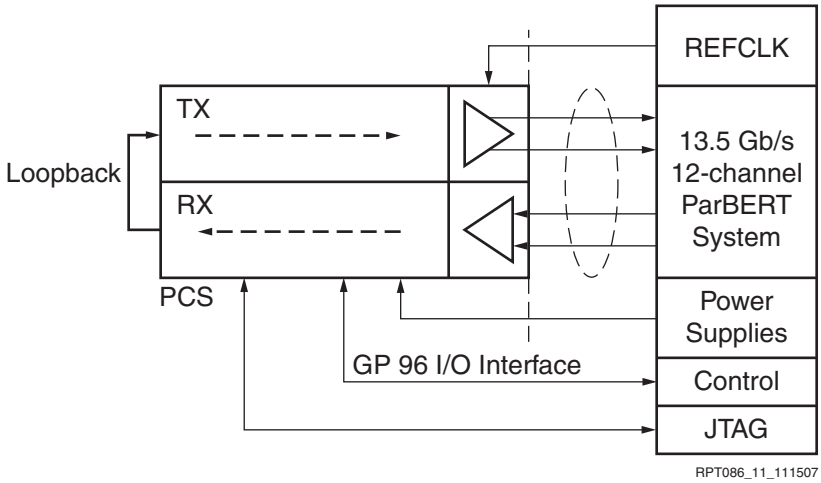

Figure 11: **Test Setup**

Characterization Data

This section provides characterization data for each Fibre Channel line rate. Table 13 shows the test conditions and results summary for the 2.125 Gb/s line rate.

Table 13: **Test Conditions and Results of Output Jitter for 200-DF-EL-S**

	Description
Test Case	Output jitter in UI.
Conditions	V_{CC} = NOM ± 5%, Temperature = –40°C to +100°C (I-grade).
Method	BTC method. Eye step = 0.005 UI. Number of bits collected = 10^8. A BER test was performed at each step in the eye, and the BER rate was calculated. The Dual Dirac method was used to extrapolate the eye opening at BER = 10^{-12}. A BTC functional call reported TJ (TJ = 1 – eye opening) and an estimate for RJ.
Configuration/Standard	DATARATE = 2.125 Gb/s REFCLK = 106.25 MHz Target standard = Fibre Channel PLL = N/M/P(1) = 10/1/1 VCO = 1.0625 GHz

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Table 13: **Test Conditions and Results of Output Jitter for 200-DF-EL-S *(Continued)***

	Description		
	Parameter	**TJ (UI)**	**DJ (UI)**
Results	Median	0.207	0.050
	Average	0.208	0.049
	Maximum	0.27	0.125
	Standard Deviation	0.018	0.018

Notes:

1. While N/M/P are not directly mapped into attributes of the GTP transceiver, they do represent what is happening with the shared PMA PLL:
   - N = PLL_DIVSEL_FB x DIV (DIV = 5, indicating 10-bit mode)
   - M = PLL_DIVSEL_REF
   - P = PLL_TXDIVSEL_OUT_0

Figure 12 and Figure 13 show the total jitter and deterministic jitter histograms, respectively, at the 2.125 Gb/s line rate.

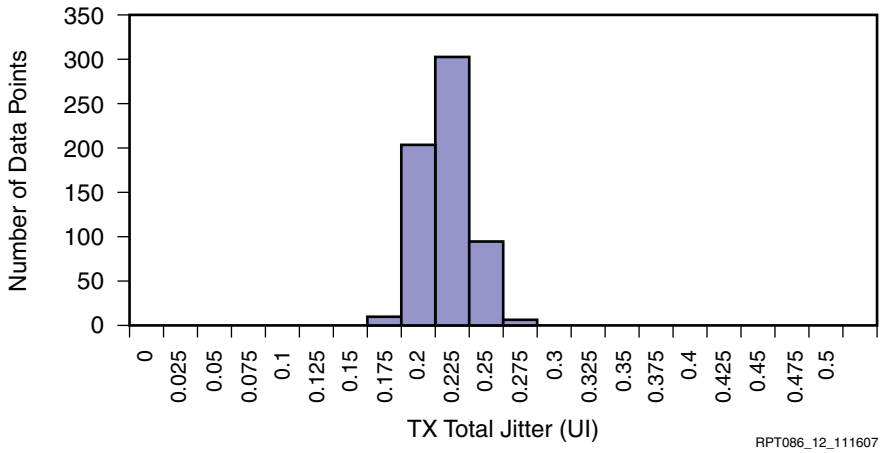

Figure 12: **Total Jitter Histogram at 2.125 Gb/s**

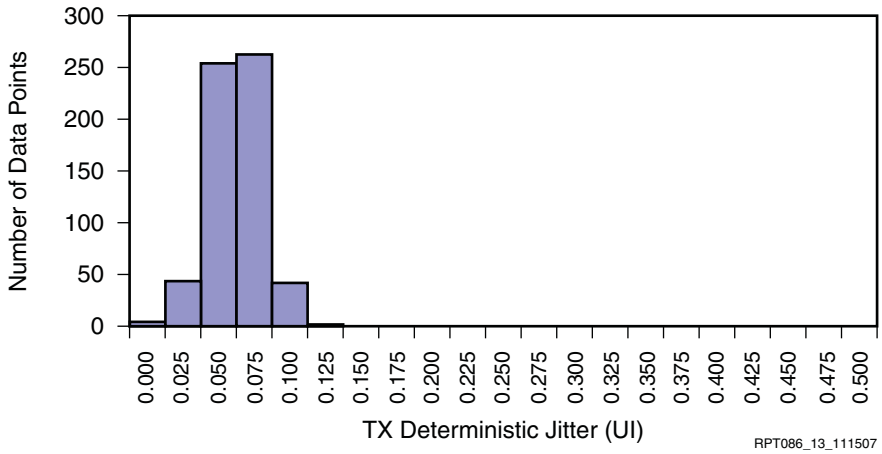

Figure 13: **Deterministic Jitter Histogram at 2.125 Gb/s**

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Table 14 shows the test conditions and results summary for the 1.0625 Gb/s line rate.

Table 14: **Test Conditions and Results of Output Jitter for 100-DF-EL-S**

	Description		
Test Case	Output jitter in UI.		
Conditions	V_{CC} = NOM ± 5%, Temperature = –40°C to +100°C (I-grade).		
Method	BTC method. Eye step = 0.005. Number of bits collected = 10^8. A BER test was performed at each step in the eye, and the BER rate was calculated. The Dual Dirac method was used to extrapolate the eye opening at BER = 10^{-12}. BTC functional call reported TJ (TJ = 1 – eye opening) and an estimate for RJ.		
Configuration/Standard	DATARATE = 1.0625 Gb/s REFCLK = 106.25 MHz Target STD = Fibre Channel PLL = N/M/P(1) = 10/1/2 VCO = 1.0625 GHz		
Results	**Parameter**	**TJ (UI)**	**DJ (UI)**
	Median	0.114	0.034
	Average	0.113	0.035
	Maximum	0.159	0.077
	Standard Deviation	0.011	0.014

Notes:

1. While N/M/P are not directly mapped into attributes of the GTP transceiver, they do represent what is happening with the shared PMA PLL:
   - N = PLL_DIVSEL_FB x DIV (DIV = 5, indicating 10-bit mode)
   - M = PLL_DIVSEL_REF
   - P = PLL_TXDIVSEL_OUT_0

Figure 14 and Figure 15 show the total jitter and deterministic jitter histograms, respectively, at the 1.0625 Gb/s line rate.

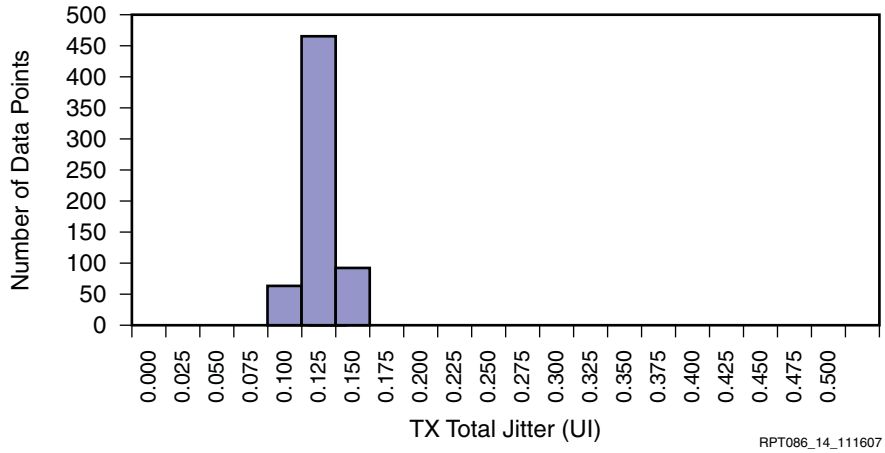

Figure 14: **Total Jitter Histogram at 1.0625 Gb/s**

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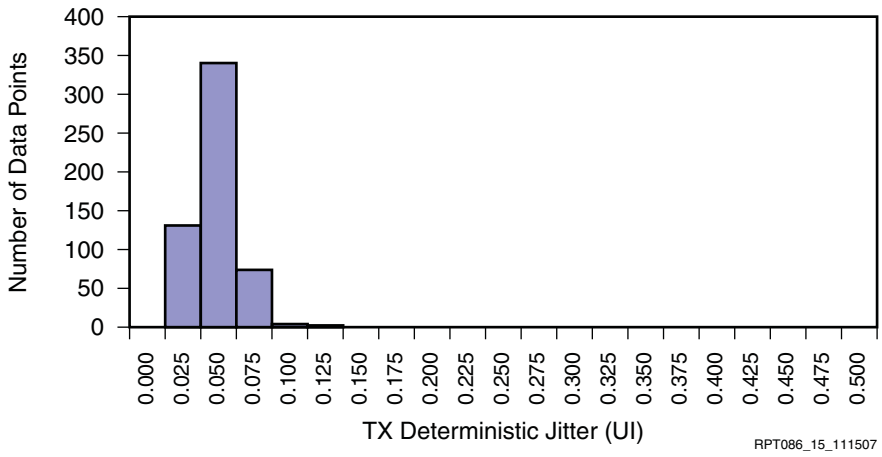

Figure 15: **Deterministic Jitter Histogram at 1.0625 Gb/s**

Transmitter Amplitude, Rise/Fall Times, and Differential Skew Measurements

Test Description

The Agilent N4901B serial BERT generated data and drove four channels of the high-speed multiplexer. The high-speed multiplexer drove data to four different GTP transceivers of the FPGA. The device operated in Far-end PMA loopback mode in which the received data was looped back to the transmitter at the FPGA logic interface. The TX tests were performed at both Fibre Channel data rates of 2.125 Gb/s and 1.0625 Gb/s using an Agilent 86100A Infiniium DCA wide-bandwidth oscilloscope.

Lab Setup

The XC5VLX50T device characterization bench setup consisted of several components such as a host PC with GUI, ML523 characterization board, and test equipment. The entire system was controlled by a PC with a GUI interface. The GUI was written with the Agilent VEE software tool and interfaced with the FPGA's internal controller through a 32-bit parallel cable. The GUI set the Agilent 6624A system SC power supply voltage and the Agilent N4901B serial BERT data rate and pattern based on the various test conditions.

The Agilent 6624A system SC power supply provided a separate voltage to each of the following onboard regulators: 5V, MGTAVTTTX, MGTAVTTRX, MGTAVCCPLL, and MGTAVCC. Other onboard regulators provided voltage for V_{CCO}, V_{CCINT}, and V_{CCAUX}.

The Agilent N4901B serial BERT internal clock was used as a master clock source for the entire system. The pattern generator differential output signals drove the RX inputs of the FPGA. The pattern generator's trigger output signal drove the Agilent 81134A pulse generator's external clock input. The Agilent 81134A pulse generator generated differential clock signals for GTP receivers. After setting up this equipment, the system configured the FPGA and changed the TXDIFFCTRL setting. After configuring the FPGA, the system began to collect data using the Agilent 86100A Infiniium DCA wide-bandwidth oscilloscope. This process of changing the TXDIFFCTRL setting and collecting data using the oscilloscope continued until all test conditions were covered.

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Environmental Conditions

The operating supply voltages are shown in Table 15. The operating temperatures at the junction were –40°C, 0°C, and 100°C.

Table 15: **Operating Supply Voltages**

Supply	Level (V)
MGTAVCCPLL	1.2
MGTAVTTRX	1.2
MGTAVTTTX	1.14, 1.26
MGTAVCC	1.0
V_{CCAUX}	2.5
V_{CCIN}	1.0
V_{CCO}	2.5

Amplitude Tests

Specification

The specification requires the differential output amplitude of the driver to be less than 1600 mV_{pp}, including any transmit equalization. DC-referenced logic levels are not defined because the receiver is AC coupled. The absolute driver output voltage is between –0.4V and 2.3V with respect to ground. Figure 16 illustrates the absolute driver output voltage limits and the definition of differential peak-to-peak amplitude.

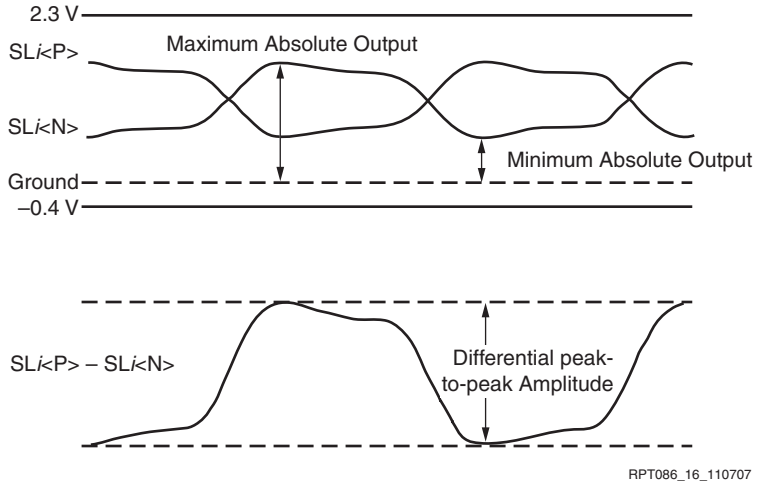

Figure 16: **Transmitted Output Voltage Limits and Definitions**

Transmitter output amplitude tests were conducted at both Fibre Channel line rates of 2.125 Gb/s and 1.0625 Gb/s, and for the two swing control settings of `000` and `011`. The internal swing control port signals TXDIFFCTRL[2:0] (= TXBUFDIFFCTRL[2:0]) were set to `000` or `011` for each test case.

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Characterization Data

Figure 17 shows the transmitter peak-to-peak output amplitude for TXDIFFCTRL = 000 at both Fibre Channel line rates.

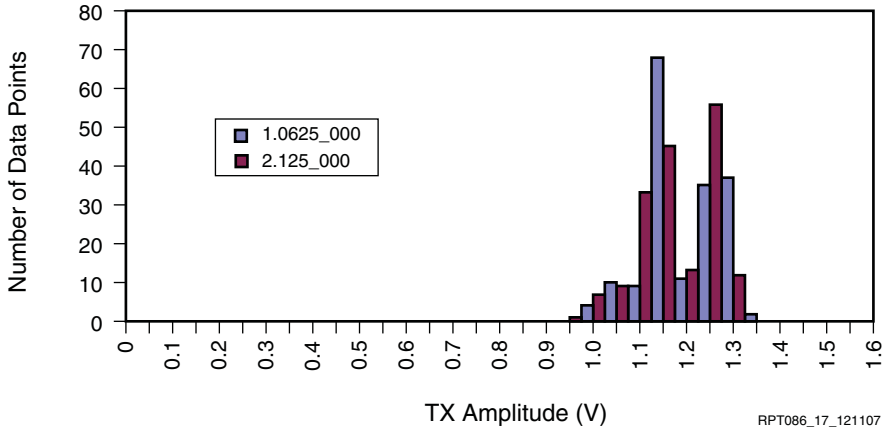

Figure 17: **TX Amplitude Histogram (TXDIFFCTRL = 000)**

Table 16 lists the base values for the operating corner coefficients for Figure 17.

Table 16: **TX Amplitude Statistics (TXDIFFCTRL = 000)**

Temp (°C)	Voltage (V)	TX Amplitude				Units
		Mean	Standard Deviation	Max	Min	
ALL	ALL	1.14	0.08	1.32	0.95	mV

Figure 18 shows the transmitter peak-to-peak output amplitude for TXDIFFCTRL = 011 at both Fibre Channel line rates.

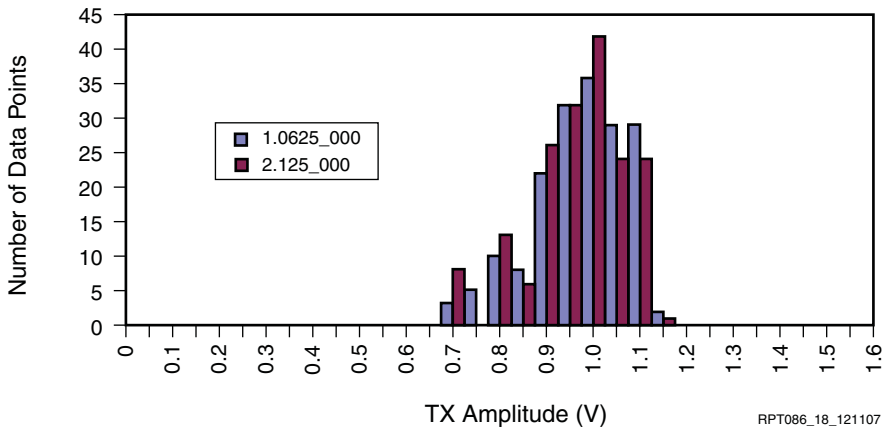

Figure 18: **TX Amplitude Histogram (TXDIFFCTRL = 011)**

Table 17 lists the base values for the operating corner coefficients for Figure 18.

Table 17: **TX Amplitude Statistics (TXDIFFCTRL = 011)**

Temp (°C)	Voltage (V)	TX Amplitude				Units
		Mean	Standard Deviation	Max	Min	
ALL	ALL	0.93	0.10	1.15	0.67	mV

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Rise/Fall Time Measurements

The GTP TX output rise/fall time measurements were made at both Fibre Channel specific data rates of 2.125 Gb/s and 1.0625 Gb/s. The resulting trends are plotted in the following data plots and tables.

Characterization Data

Figure 19 shows the transmitter output rise time measurement trends for both Fibre Channel data rates.

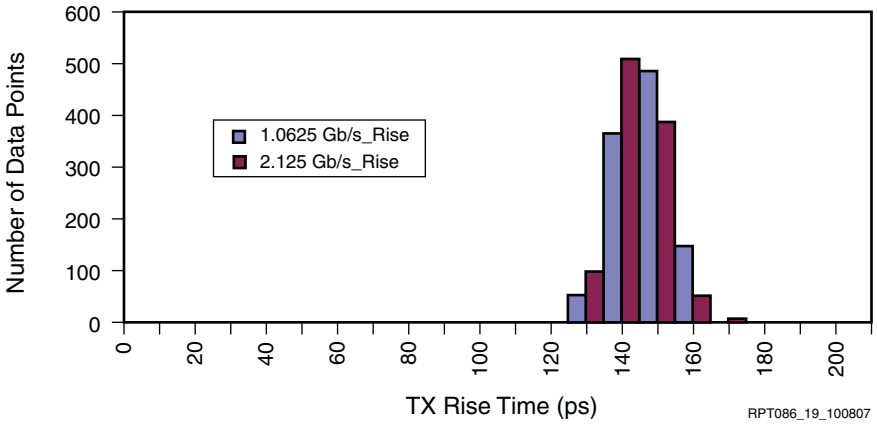

Figure 19: **TX Rise Time Histogram**

Table 18 lists the base values for the operating corner coefficients for Figure 19.

Table 18: **TX Rise Time Statistics**

Temp (°C)	Voltage (V)	TX Rise Time				Units
		Mean	Standard Deviation	Max	Min	
ALL	ALL	148.05	12.40	165.20	130.00	ps

Figure 20 shows the transmitter output fall time measurement trends for both Fibre Channel data rates.

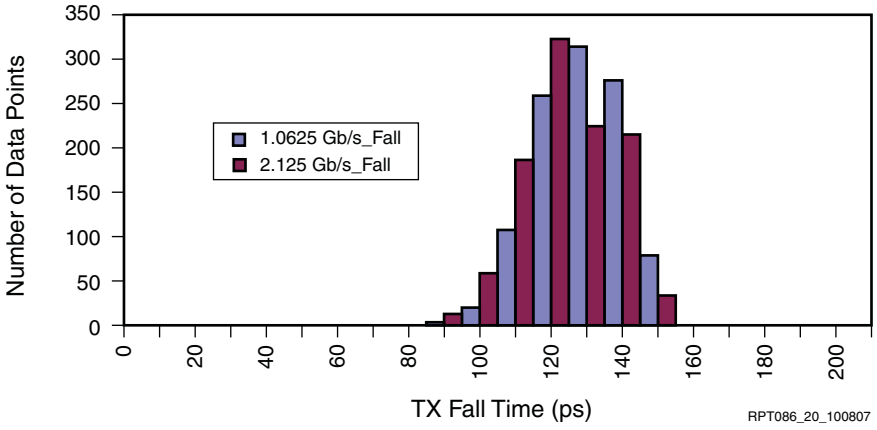

Figure 20: **TX Fall Time Histogram**

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Table 19 lists the base values for the operating corner coefficients for Figure 20.

Table 19: **TX Fall Time Statistics**

Temp (°C)	Voltage (V)	TX Fall Time				Units
		Mean	Standard Deviation	Max	Min	
ALL	ALL	127.11	15.80	154.34	87.69	ps

TX Differential Skew Measurements

The GTP TX output differential skew between the TXP and TXN signals is measured in this test.

Characterization Data

Figure 21 shows the transmitter output skew between the TXP and TXN signals.

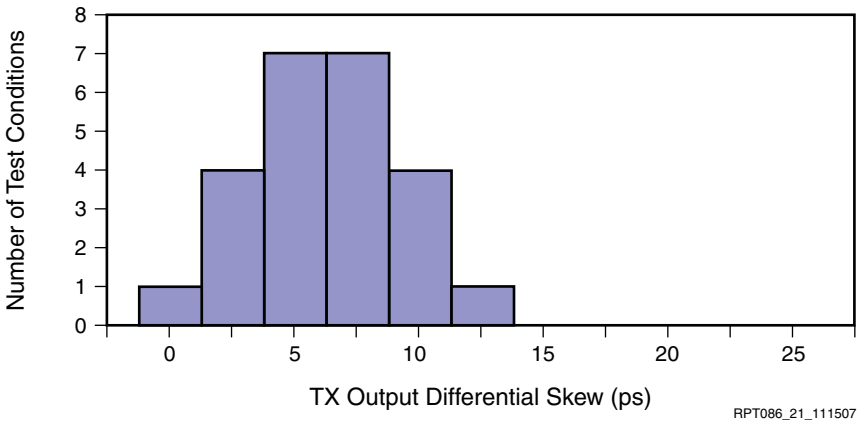

Figure 21: **TX Output Differential Skew Data Plot**

Appendix A: References

The following references were used in this characterization report:

1. FC-PI-2 ANSI INCITS 404-2006 American National Standard for Information Technology - Fibre Channel - Physical Interfaces-2.
2. FC-MJSQ ANSI INCITS TR-35-2004 Information Technology - Fibre Channel - Methodologies for Jitter and Signal Quality Specification.
3. FC-FS ANSI INCITS 373-2003 Information Technology - Fibre Channel - Framing and Signaling.
4. UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*.

Appendix B: Test Equipment

This appendix lists the lab equipment used in this characterization report.

Equipment

The following equipment was used in this characterization:

- Agilent 86130A BitAlyzer error performance analyzer with PRBS test patterns

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- HP 81130A pulse data generator
- HP 81134A pulse pattern generator
- Agilent 3325B synthesizer
- Agilent 83752A synthesized sweeper
- Agilent 70820A microwave transition analyzer
- Agilent 86100A Infiniium DCA wide-bandwidth oscilloscope
- Agilent 86100C Infiniium DCA-J oscilloscope
- NoiseCom 6108 noise generator
- Agilent 71501C jitter analysis system
- Agilent 81134A pulse pattern generator
- Agilent N4901B serial BERT 13.5 Gb/s
- Agilent E8403A 13-slot, C-size, VXI mainframe
- Agilent N4872A 13.5 Gb/s ParBERT generator module
- Agilent N4873A 13.5 Gb/s ParBERT analyzer module
- Agilent 6624A system power supply

Test Fixtures

The following test fixtures were used:

- Xilinx ML523 characterization board, revision A with ML52X power module, revision B
- Xilinx quad serial loop board, revision B

Accessories

The following accessories were used:

- Inmet DC blocks, part number 8037
- Inmet attenuators, part numbers 26AH-20db and 26AH-6db
- Low-loss SMA coaxial cables

Software

The following software was used:

- ChipScope analyzer, version 8.2i and later
- Agilent VEE software tool
- XBERT software GUI, version 1.1.2 (Xilinx internal)
- XBERT hardware, version 1.1 (Xilinx internal)

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