

# **Xilinx Spartan-3A/-3AN FT/FTG 256 2-Layer Substrate**

## ***Qualification Report***

RPT112 (v1.0) October 20, 2008



[www.BDTIC.com/XILINX](http://www.BDTIC.com/XILINX)



Xilinx is disclosing this Document and Intellectual Property (hereinafter "the Design") to you for use in the development of designs to operate on, or interface with Xilinx FPGAs. Except as stated herein, none of the Design may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Any unauthorized use of the Design may violate copyright laws, trademark laws, the laws of privacy and publicity, and communications regulations and statutes.

Xilinx does not assume any liability arising out of the application or use of the Design; nor does Xilinx convey any license under its patents, copyrights, or any rights of others. You are responsible for obtaining any rights you may require for your use or implementation of the Design. Xilinx reserves the right to make changes, at any time, to the Design as deemed desirable in the sole discretion of Xilinx. Xilinx assumes no obligation to correct any errors contained herein or to advise you of any correction if such be made. Xilinx will not assume any liability for the accuracy or correctness of any engineering or technical support or assistance provided to you in connection with the Design.

THE DESIGN IS PROVIDED "AS IS" WITH ALL FAULTS, AND THE ENTIRE RISK AS TO ITS FUNCTION AND IMPLEMENTATION IS WITH YOU. YOU ACKNOWLEDGE AND AGREE THAT YOU HAVE NOT RELIED ON ANY ORAL OR WRITTEN INFORMATION OR ADVICE, WHETHER GIVEN BY XILINX, OR ITS AGENTS OR EMPLOYEES. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DESIGN, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOST DATA AND LOST PROFITS, ARISING FROM OR RELATING TO YOUR USE OF THE DESIGN, EVEN IF YOU HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE TOTAL CUMULATIVE LIABILITY OF XILINX IN CONNECTION WITH YOUR USE OF THE DESIGN, WHETHER IN CONTRACT OR TORT OR OTHERWISE, WILL IN NO EVENT EXCEED THE AMOUNT OF FEES PAID BY YOU TO XILINX HEREUNDER FOR USE OF THE DESIGN. YOU ACKNOWLEDGE THAT THE FEES, IF ANY, REFLECT THE ALLOCATION OF RISK SET FORTH IN THIS AGREEMENT AND THAT XILINX WOULD NOT MAKE AVAILABLE THE DESIGN TO YOU WITHOUT THESE LIMITATIONS OF LIABILITY.

**CRITICAL APPLICATIONS DISCLAIMER:** XILINX PRODUCTS (INCLUDING HARDWARE, SOFTWARE AND/OR IP CORES) ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, "CRITICAL APPLICATIONS"). FURTHERMORE, XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR. CUSTOMER AGREES, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE XILINX PRODUCTS, TO THOROUGHLY TEST THE SAME FOR SAFETY PURPOSES. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN CRITICAL APPLICATIONS, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

© 2008 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/20/08	1.0	Initial release.

# Table of Contents

---

**Overview** .....4  
**Package Qualifications**.....4  
**Major Package Information Used in This Qualification**.....4  
**Reliability Test Conditions and Results**.....5  
**ESD and LU Test Results**.....6  
**Reliability Test Data** .....6

## Overview

This qualification report summarizes the results of the reliability tests that were performed to qualify the 90nm Spartan®-3A FPGA product family in the 2-layer FT256 substrate.

## Package Qualifications

A full package qualification was run on XA3S400A-FTG256. Since XA qualification is more stringent (since it includes passing electrical read points at room, -40 and 125°C), this qualification testing covers by extension XC3S400A-FT/FTG256. This qualification also covers XC3S50A-FT/FTG256, XC3S200A-FT/FTG256, and XC3S200AN-FT/FTG256 by similarity (including smaller die size) per Table 1.

**Table 1: Qualification Matrix**

Part Number	FT/FTG 256
XC3S50A	X
XC3S200A	X
XC3S200AN	X
XC3S400A	X
XA3S400A	X

	= Package qualification vehicle
	= Qualified by similarity
X	= Available product

## Major Package Information Used in This Qualification

**Table 2: Package Information**

Die Attach	Ablestik 2300 Series
Wire Material	Au
Mold Compound	Nitto GE100 Series
Substrate Type	BT
# of Substrate Layers	2
MSL Level	3

## Reliability Test Conditions and Results

**Table 3: Reliability Stress Tests**

**Note: The Electrical Readpoint for each test is tested at room, -40 and 125°C.**

Stress Test	ABV	Test Methods	Test Conditions	Requirements		Results
				Sample	# Lots	
Preconditioning	PC <sup>(1)</sup>	JESD22-A113 JEDEC J-STD-020	MSL 3; 192hrs, 30°C/60%RH; 3X Reflow <sup>(2)</sup> , 250/260°C+0,-5°C	77	9	Pass
Temperature Humidity Bias	THB	JESD22-A101	85°C, 85%RH, V <sub>CCMAX</sub> * 1000hrs	77	3	Pass
Biased HAST	HAST	JESD22-A110	130°C, 85%RH, V <sub>CCMAX</sub> * 96hrs	77	3	Pass
Unbiased HAST	UHST	JESD22-A118	130°C, 85%RH, 96hrs	77	3	Pass
Temperature Cycle	TC	JESD22-A104	-55°C, 125°C, 1000cyc	77	3	Pass
High Temperature Storage Life	HTSL <sup>(3)</sup>	JESD22-A103	150°C, 1000hrs	45	1	Pass
High Temperature Operating Life	HTOL <sup>(4)</sup>	JESD22-A108	125°C, V <sub>CCMAX</sub> * 1000hrs	77	3	Pass
Early Life Failure Rate	ELFR <sup>(5)</sup>	AEC Q100-008	125°C, V <sub>CCMAX</sub> * 48hrs	800	3	Pass
Wire Bond Pull Strength	WBP	MIL-STD-883-2011	Post 1000cyc of TC	5	1	Pass
ESD-HBM	HBM	AEC Q100-002	500V, 1000V, 1500V, 2000V, etc.	3	1	Pass
ESD-CDM	CDM	AEC Q100-011	250V, 500V, 750V, 1000V	3	1	Pass
Latch-Up	LU	AEC Q100-004	125°C, ±200mA (I-test) 150% of V <sub>CCMAX</sub> (Vsupply test)	6	1	Pass

**Notes:**

- (1) Preconditioning was done prior to the THB, HAST, UHST and TC tests.
- (2) Reflow was run at either 250°C or 260°C depending on package volume.
- (3) A 3X reflow was done prior to the HTSL test.
- (4) HTOL was run on Spartan-3 and Spartan-3E families.
- (5) ELFR was run on Spartan-3 family.

## ESD and LU Test Results

Table 4: ESD and LU Results

Product	Highest Passing Voltage		Latch-Up
	ESD-HBM	ESD-CDM	
XA3S200A-FTG256	>2kV	750V	Pass
XA3S400A-FTG256	>2kV	750V	Pass

## Reliability Test Data

Qualification Vehicle: XA3S400A-FTG256

Table 5: Test Results

Stress Test	Product	Fab Lot#	Assy Lot#	Assy Loc	Duration	Sample	Result
HAST	XA3S400A-FTG256	KMQ53.06	17988	SPIL	96	77	Pass
HAST	XA3S400A-FTG256	KRS34	18046	SPIL	96	77	Pass
HAST	XA3S400A-FTG256	KMN45	18094	SPIL	96	77	Pass

UHST	XA3S400A-FTG256	KMQ53.06	17988	SPIL	96	77	Pass
UHST	XA3S400A-FTG256	KRS34	18046	SPIL	96	77	Pass
UHST	XA3S400A-FTG256	KMN45	18094	SPIL	96	77	Pass

TC	XA3S400A-FTG356	KMQ53.06	17988	SPIL	1000	77	Pass
TC	XA3S400A-FTG256	KRS34	18046	SPIL	1000	77	Pass
TC	XA3S400A-FTG256	KMN45	18094	SPIL	1000	77	Pass

HTSL	XA3S400A-FTG356	KMQ53.06	17988	SPIL	1000	45	Pass
------	-----------------	----------	-------	------	------	----	------

WBP	XA3S400A-FTG356	KMQ53.06	17988	SPIL	N/A	5	Pass
		KRS34	18046				
		KMN45	18094				