ML505/ML506/ML507 Reference Design

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/16/07	1.0	Initial Xilinx release.
01/17/07	1.0.1	Minor typographical edit.
05/07/07	2.0	Added support for ML506 boards.
07/24/07	2.1	Updated "EDK Design" section.
09/25/07	2.2	Added "Memory Interface Generator (MIG) Design" section and updated "References" section.
04/04/08	2.3	Removed SGMII design. Added lwIP demonstration.
05/19/07	3.0	Added support for ML507 boards.

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ML505/ML506/ML507 Reference Design

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About This Guide

This user guide introduces several designs that demonstrate Virtex®-5 FPGA features using the ML505 (LXT), ML506 (SXT), and ML507 (FXT) Evaluation Platforms (referred to collectively as the ML50*x* boards in this guide). The provided designs include processing systems based on the embedded PowerPC® 440 processor block, the MicroBlaze™ soft processor, the integrated Tri-mode Ethernet MAC, and the RocketIO™ GTP or GTX transceiver.

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  Chapters in this user guide cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO GTP transceivers available in the Virtex-5 LXT and SXT platforms.

- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.

- Embedded Processor Block in Virtex-5 FPGAs Reference Guide

  This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.

- Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the Virtex-5 *FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details. Refer to "System Monitor Primitive" for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML505/ML506/ML507 Reference Design

Introduction

The Virtex-5 family of FPGAs [Ref 1] offers designers multiple platforms with an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing resources. All members of the Virtex-5 family are built using the second generation Advanced Silicon Modular Block (ASMBL™) technology and a state-of-the-art 65 nm copper process to produce the industry's highest performance FPGAs. In addition to the embedded PowerPC 440 processor block, integrated system-level hard-IP blocks for PCI Express® (PCIe®), Tri-mode Ethernet, and advanced high-speed RocketIO GTP and GTX serial transceivers are also provided through the Virtex-5 FPGA family.

Along with capabilities offered directly through an integrated IP block implemented in silicon, the Xilinx LogiCORE™ IP catalog and the embedded processing IP catalog are available to system level designers. For designers utilizing the RocketIO GTP/GTX transceivers, the Chipscope™ Pro Serial IO Toolkit offers the fastest way to setup and begin using the high speed serial IO channels. A design using the Xilinx Memory Interface Generator (MIG) tool is also provided to show an easy way to design, implement, and verify external memory interfaces. [Ref 22]

Offered as general purpose development boards, the ML505, ML506, and ML507 platforms are useful for exercising the new architectural features of Virtex-5 FPGAs and as platforms to create user designs. Sharing a common printed circuit board (PCB) the only difference between the boards is the FPGA:

- ML505 is populated with the Virtex-5 XC5VLX50T device
- ML506 is populated with the Virtex-5 XC5VSX50T device
- ML507 is populated with the Virtex-5 XC5VFX70T device

The Virtex-5 FXT platform contains an embedded PowerPC 440 processor block with integrated DMA engines and a multi-port crossbar switch that offers designers unparalleled FPGA processing power through the ML507. In addressing the common features of the ML505, ML506, or ML507, this guide refers to the boards as the ML50x.

Users can obtain a quick understanding of the features offered by the ML50x boards by running the demonstration content provided on the CompactFlash (CF) card included with each board. *ML505/ML506/ML507 Getting Started Tutorial* [Ref 17] shows how to configure the ML50x from the ACE files pre-loaded on the CF card and describes what to observe for expected output.

Reference Designs

EDK Design

The ML50*x* platforms utilize the Embedded Development Kit (EDK) and the Base System Builder (BSB) wizard to create embedded processing systems. The BSB wizard helps designers quickly create a working embedded system using a point-and-click graphical user interface (GUI) to select a Xilinx processor and an associated set of peripherals. Processing systems using either the MicroBlaze soft processor or the embedded PowerPC 440 block can be generated by BSB. BSB designs can be further customized within the Xilinx Platform Studio (XPS) environment by leveraging the extensive set of peripherals offered through the EDK IP catalog.

BSB generated designs for the ML50*x* boards are available at:

- http://www.xilinx.com/products/boards/ml505/reference_designs.htm#bsb_design
- http://www.xilinx.com/products/boards/ml506/reference_designs.htm#bsb_design
- http://www.xilinx.com/products/boards/ml507/reference_designs.htm#bsb_design

MicroBlaze Processor

All the ML50*x* platforms support a common set of software applications and hardware designs that utilize the MicroBlaze soft processor. The BSB design Web page lists multiple MicroBlaze reference designs along with documentation on how to use the BSB wizard and XPS to create these designs.

- **ML505 EDK BSB base design** (ml505_bsb_design.zip)

  The base design is an out-of-the-box BSB design which demonstrates many of the features offered on the board.

- **ML505 EDK BSB design with standard IP addition** (ml505_bsb_std_ip.zip)

  This design is derived from the base design by using XPS to add standard supported EDK peripherals. The additional EDK peripherals are used to access more of the GPIO and IIC devices on the board.

- **ML505 EDK standard IP design with USB addition** (ml505_bsb_std_ip_usb.zip)

  This design is also derived from the base design by using XPS to add standard supported EDK peripherals. The additional EDK peripherals are used to provide USB capabilities.

- **ML505 EDK standard IP design with pcores addition** (ml505_std_ip_pcores.zip)

  This design adds a frame-buffer-based video output port to the base design. The PLB v4.6 DVI/VGA pcore that drives the video port was created by using EDK's Create and Import Peripheral wizard as a template.

  An application demonstrating the EDK port of the open source Lightweight IP (lwIP) networking library is also provided. The Xilinx Ethernet xps_ll_temac MAC is used to demonstrate GMII and SGMII PHY interfaces with lwIP's *raw* and *sockets* modes Application Program Interface (API). Previous designs used LogiCORE IP to demonstrate SGMII capability that is now available through an EDK peripheral. The EDK *OS and Libraries Document Collection* provides additional details on using the lwIP networking library. [Ref 16]

PowerPC 440 Processor

In addition to supporting MicroBlaze soft processor designs, the ML507 supports PowerPC 440 processor designs. ML507 reference designs that use the Virtex-5 FXT integrated PowerPC 440 processor block are labeled with the *_ppc440* suffix in their names. These designs are functionally equivalent to the MicroBlaze designs and use the same set of PLBv46 peripherals offered by the EDK IP catalog. The descriptions are the same as those listed for the "MicroBlaze Processor," page 10.

- **ML507 EDK BSB base design** (ml507_bsb_design_ppc440.zip)
- **ML507 EDK BSB design with standard IP addition** (ml507_bsb_std_ip_ppc440.zip)
- **ML507 EDK standard IP design with USB addition** (ml507_bsb_std_ip_usb_ppc440.zip)
- **ML505 EDK standard IP design with pcores addition** (ml507_std_ip_pcores_ppc440.zip)

The strategy of beginning with a known good BSB design and deriving new designs with additional capabilities offers a quick way to generate a variety of designs and the ability to debug designs using incremental changes.

Stand-Alone Software Applications

Stand-alone software applications (Table 1) are provided to verify board functionality. These applications can be compiled within EDK and downloaded to the ML50*x* over a JTAG download cable. Pre-built bitstreams, ELF and ACE files, and readme.txt files that explain how to run each of the applications for the ML50*x* boards are available at:

- http://www.xilinx.com/products/boards/ml505/standalone_apps.htm
- http://www.xilinx.com/products/boards/ml506/standalone_apps.htm
- http://www.xilinx.com/products/boards/ml507/standalone_apps.htm

Table 1: **Software Applications (ML505 Example)**

ML505 Designs	Description
ml505_mb_standalone_apps_bit_elf_ace.zip	Complete collection of stand-alone applications and board test BIT, ELF, and ACE files. To run each application individually, select one of the ACE files below and replace the system_my_ace.ace in configuration address 6 of the production ML505 CF card.
BSB Designs	
ML505 EDK BSB Design	Design source files and tutorials.
ml505_bsb_bootloop.bit ml505_bsb_testapp_mem.elf ml505_bsb_testapp_mem.ace testapp_memory_readme.txt	Tests SRAM and DDR2 memory.

Table 1: **Software Applications (ML505 Example)** *(Cont'd)*

ML505 Designs	Description
ml505_bsb_bootloop.bit ml505_bsb_testapp_periph.elf ml505_bsb_testapp_periph.ace testapp_peripheral_readme.txt	Tests the following peripherals: • RS232_Uart_2 • LEDs_8Bit • LEDs_Positions • Push_Buttons_5Bit • DIP_Switches_8Bit • IIC_EEPROM • Ethernet_MAC • SysACE_CompactFlash • debug_module
BSB Plus Standard IP Designs	
ML505 BSB Design IP Addition	Design source files and tutorials.
ml505_std_ip_bootloop.bit bootload_lcd.elf bootload_lcd.ace bootload_lcd_readme.txt	Main menu to load and launch ACE file demonstrations.
ml505_std_ip_bootloop.bit button_led_test.elf button_led_test.ace button_led_test_readme.txt	Verifies functionality of GPIO DIP switches, GPIO LEDs, N-E-S-W buttons, and LEDs.
ml505_std_ip_bootloop.bit xflash.elf xflash.ace xflash_readme.txt	Tests linear flash memory.
ml505_std_ip_bootloop.bit hello.elf hello.ace hello_readme.txt	Exercises serial port output and input functionality using `libc` routines.
ml505_std_ip_bootloop.bit hello_uart.elf hello_uart.ace hello_uart_readme.txt	Exercises serial port output and input functionality using low-level UART driver routines on UART #1.
ml505_std_ip_bootloop.bit hello_uart_1.elf hello_uart_1.ace hello_uart_1_readme.txt	Exercises serial port output and input functionality using low-level UART driver routines on UART #2.
ml505_std_ip_bootloop.bit iic_clock.elf iic_clock.ace iic_clock_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the clock generator chip.
ml505_std_ip_bootloop.bit iic_ddr2.elf iic_ddr2.ace iic_ddr2_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the DDR2 SPD EEPROM.

Table 1: **Software Applications (ML505 Example)** *(Cont'd)*

ML505 Designs	Description
ml505_std_ip_bootloop.bit iic_dvi_connector.elf iic_dvi_connector.ace iic_dvi_connector_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the DVI connector's IIC pins.
ml505_std_ip_bootloop.bit iic_dvi_controller.elf iic_dvi_controller.ace iic_dvi_controller_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the DVI controller.
ml505_std_ip_bootloop.bit iic_eeprom.elf iic_eeprom.ace iic_eeprom_readme.txt	IIC Dynamic mode EEPROM access example.
ml505_std_ip_bootloop.bit iic_fan.elf iic_fan.ace iic_fan_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the fan controller.
ml505_std_ip_bootloop.bit iic_sfp.elf iic_sfp.ace iic_sfp_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access a user-supplied SFP module.
ml505_std_ip_bootloop.bit iic_vga_in_controller.elf iic_vga_in_controller.ace iic_vga_in_controller_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the VGA input controller.
ml505_std_ip_bootloop.bit piezo.elf piezo.ace ringtones.zip piezo_readme.txt	Demonstrates audio output to the onboard piezo speaker using the ringtone RTTTL files.
ml505_std_ip_bootloop.bit testfatfs.elf testfatfs.ace testfatfs.zip testfatfs_readme.txt	Write and read test of the FAT file system on the CompactFlash card.
ml505_std_ip_bootloop.bit sysace_rebooter.elf sysace_rebooter.ace sysace_rebooter_readme.txt	User-selectable loading of ACE files utilizing the System ACE CF controller.
BSB Plus Standard IP Plus USB Designs	
ML505 STD IP Design USB Addition	Design source files and tutorials.
ml505_std_ip_usb_bootloop.bit usb_hpi_test.elf usb_hpi_test.ace demo.bin usb_hpi_test_readme.txt	Tests the USB host interface utilizing a USB keyboard.

Table 1: **Software Applications (ML505 Example)** *(Cont'd)*

ML505 Designs	Description
BSB Plus Standard IP Plus PCORE Designs	
ML505 STD IP Design Pcore Addition	Design source files and tutorials.
ml505_pcores_bootloop.bit bootload_video.elf bootload_video.ace bootload_video_readme.txt	Video bootload application.
ml505_pcores_bootloop.bit flash_hello.elf flash_hello_readme.txt	Placeholder application for a user-generated Linear Flash design. Loaded from Linear Flash.
ml505_pcores_bootloop.bit my_ace.elf my_ace.ace my_ace_readme.txt	Placeholder application for a user-generated ACE file. Loaded from CompactFlash.
ml505_pcores_bootloop.bit my_plat_flash.elf my_plat_flash_readme.txt	Placeholder application for a user-generated Platform Flash design. Loaded from Platform Flash.
ml505_pcores_bootloop.bit slideshow.elf slideshow.ace slides.zip slideshow_readme.txt	A self-running audio and video presentation highlighting features of the ML505 and Virtex-5 FPGA technology.
ml505_pcores_bootloop.bit simon.elf simon.ace simon_readme.txt	Interactive game using N-E-S-W buttons, LEDs, and the LCD panel.
ml505_pcores_bootloop.bit spi_hello.elf spi_hello_readme.txt	Placeholder application for a user-generated SPI Flash design. Loaded from SPI Flash.
ml505_pcores_bootloop.bit test_ac97.elf test_ac97.ace test_ac97_readme.txt	Records and plays back audio using the AC97 controller.
ml505_pcores_bootloop.bit xrom.elf xrom.ace xrom_readme.txt	Board tests/diagnostics.
ml505_pcores_bootloop.bit lwipdemo.elf lwipdemo.ace lwipdemo_readme.txt	Demonstrates networking functionality using lwIP in sockets mode.
ml505_pcores_bootloop.bit webserver.elf webserver.ace webserver_readme.txt	Web browser based control of GPIO LEDs and display of GPIO DIP switch status over Ethernet. Uses LWIP in raw mode for a webserver.

Table 1: **Software Applications (ML505 Example)** *(Cont'd)*

ML505 Designs	Description
BSB Plus Standard IP Plus PCORE Plus SGMII Designs	
ML505 STD IP Pcores Design SGMII Addition	Design source files and tutorials.
ml505_pcores_sgmii_bootloop.bit lwipdemo_sgmii.elf lwipdemo_sgmii.ace lwipdemo_sgmii_readme.txt	Uses LWIP in sockets mode for a webserver.
ml505_pcores_sgmii_bootloop.bit webserver_sgmii.elf webserver_sgmii.ace webserver_sgmii_readme.txt	Uses LWIP in raw mode for a webserver.

Operating System Software Applications

Along with the ability to run stand-alone software applications, the ML507 can demonstrate embedded operating system (OS) based applications. By using the EDK board support package (BSP) generation process as described in the *OS and Libraries Document Collection* [Ref 16], a software developer can create a BSP for a supported third-party OS. After a BSP is generated, the customer-provided third-party tools can be used to create the OS based software application that runs on the embedded development platform. A link to a tutorial and an example design for generating a VxWorks BSP and system image is provided on the ML507 reference designs page.

ML507 referernce design Web page:

- http://www.xilinx.com/products/boards/ml507/reference_designs.htm

ML507 VxWorks example:

- http://www.xilinx.com/products/boards/ml507/vxworks.htm

ChipScope Pro Serial I/O Toolkit IBERT Design

The ChipScope Pro Serial I/O Toolkit [Ref 19] provides the ability to generate a hardware design to exercise the Virtex-5 RocketIO GTP/GTX transceivers. Refer to the respective RocketIO transceiver user guides for further information [Ref 5] [Ref 6]. After querying the user for the device part and package, the location of a system clock pin, the dedicated RocketIO GTP/GTX clock pins, and the expected transceiver line rates, the ChipScope Pro software generates a bitstream that implements an Integrated Bit Error Ratio Tester (IBERT). The IBERT design is easily scalable to user board designs. A pre-built IBERT design and tutorial is available for the ML50*x* boards at:

- http://www.xilinx.com/products/boards/ml505/reference_designs.htm#ibert_design
- http://www.xilinx.com/products/boards/ml506/reference_designs.htm#ibert_design
- http://www.xilinx.com/products/boards/ml507/reference_designs.htm#ibert_design

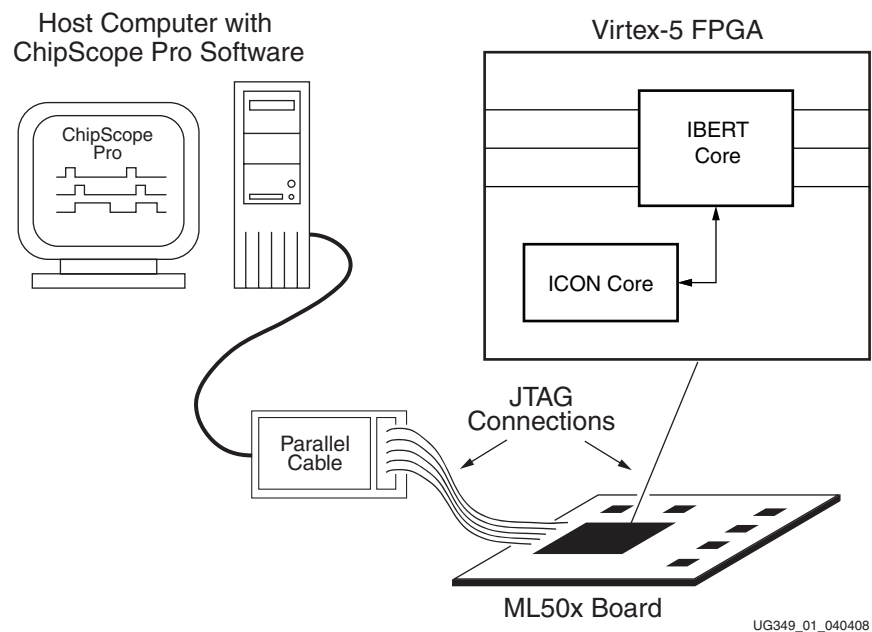Figure 1 shows an overview of the IBERT core in an ML50*x* system.

Figure 1: **IBERT Core Generated Using ChipScope Pro Software**

The IBERT design (ml505_ibert_4gtps.zip, ml506_ibert_4gtps.zip, ml507_ibert_4gtxs.zip) (Figure 2, page 17) verifies loopback connections over the following interfaces that use the GTP/GTX transceivers:

- SATA
- SFP
- SMA
- Ethernet SGMII
- PCIe
- Onboard Loopback

A SATA cross-over cable is included with the ML50x platform. Refer to the posted tutorials for a description of equipment available from third-party vendors to test these interfaces.
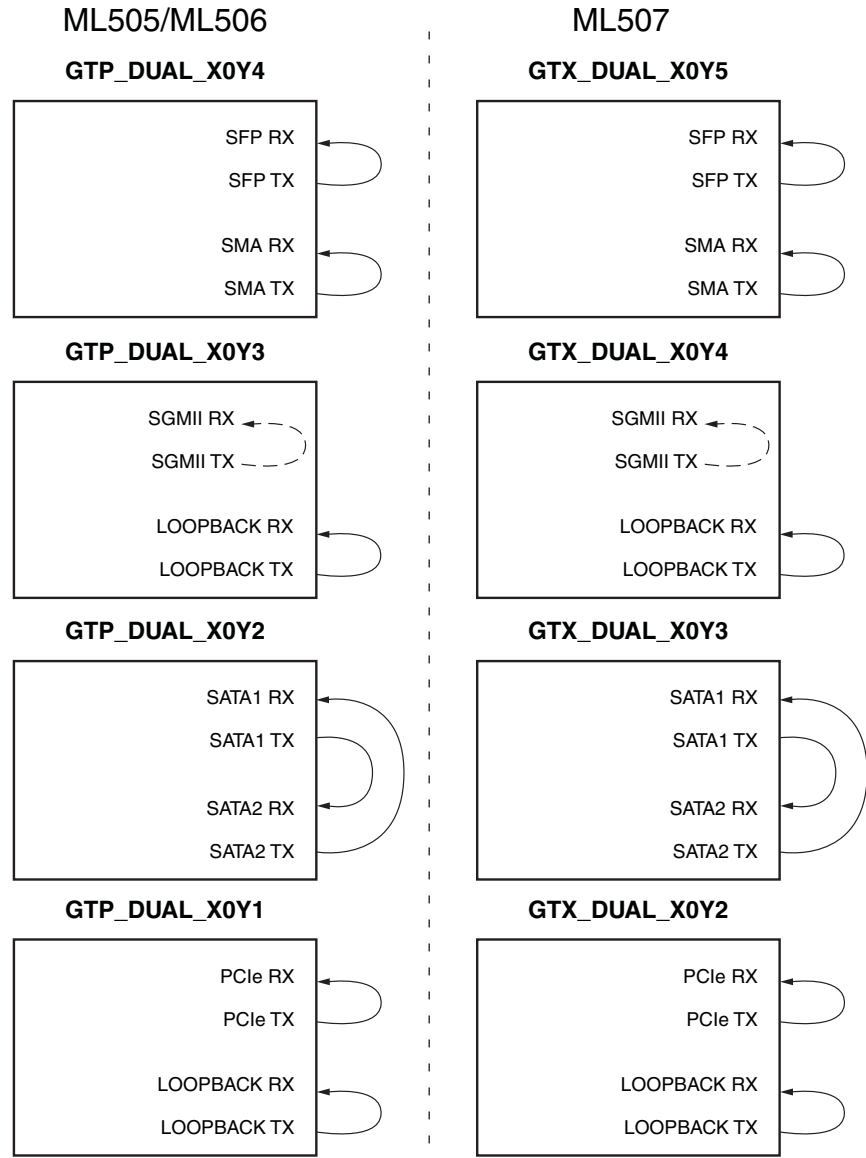
Figure 2: **IBERT Design**

Note: An internal RocketIO GTP/GTX loopback is used with the SGMII interface.
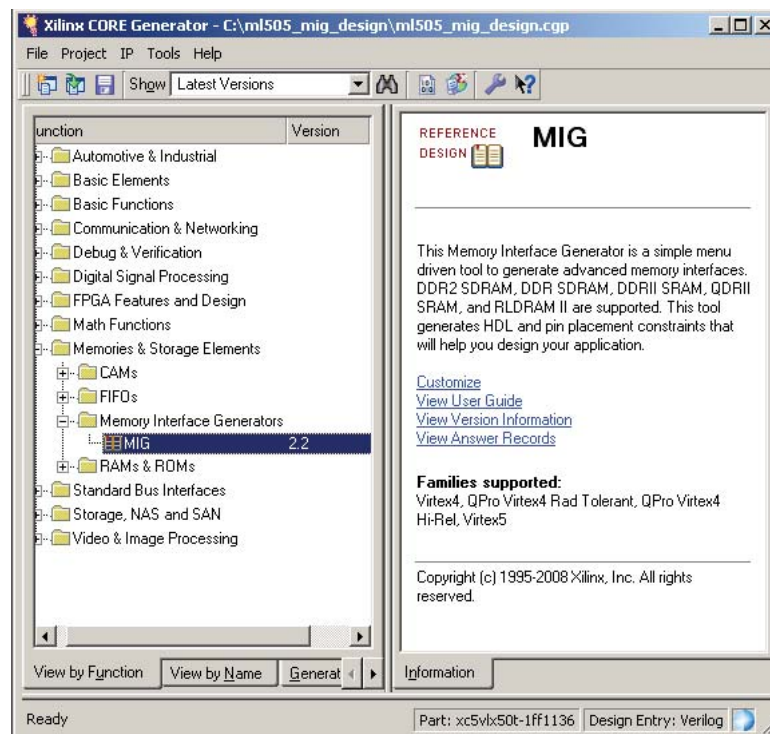
Memory Interface Generator (MIG) Design

The MIG tool can generate DDR SDRAM, DDR2 SDRAM, and QDRII SRAM interfaces for Virtex-5 FPGAs. The tool takes inputs such as the memory interface type, FPGA family, FPGA devices, frequencies, data width, memory mode register values, and so forth, from the user through a GUI. The tool generates RTL, SDC, UCF, and document files as output. RTL or EDIF (EDIF is created after running a script file, where the script file is a tool output) files can be integrated with other design files.

Refer to the *Xilinx Memory Interface Generator User Guide* [Ref 22] for information on how to download the tool, how to use the tool, and how to implement the memory controllers. The user guide also contains information on recommended pin constraints, PCB trace matching, terminations schemes, clock capable I/O rules, bank recommendations, DCI and ODT suggestions, loopback trace signals, and more. Consult this guide before implementing a PCB with an external memory interface.

The Web pages for the ML50*x* MIG design are located at:

- http://www.xilinx.com/products/boards/ml505/mig.htm
- http://www.xilinx.com/products/boards/ml506/mig.htm
- http://www.xilinx.com/products/boards/ml507/mig.htm

Figure 3, page 18 shows an example view of the MIG user interface. See the "References" section for additional MIG resources.

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Figure 3: **Memory Interface Generator**

LogiCORE Endpoint Block Plus for PCI Express (x1) Design

LogiCORE IP provides designers access to standard supported FPGA cores that can be scaled across user board designs. The ML50*x* reference design Web pages contain tutorials and an example pre-built Endpoint Block Plus wrapper that implements a single-lane Endpoint block for PCIe. The Web pages for the ML50*x* PCIe design are located at:

- http://www.xilinx.com/products/boards/ml505/reference_designs.htm#pcie_design
- http://www.xilinx.com/products/boards/ml506/reference_designs.htm#pcie_design
- http://www.xilinx.com/products/boards/ml507/reference_designs.htm#pcie_design

The tutorials describe how to verify the Programmed Input Output (PIO) example design included with the generated PCIe core by using a host PC with PCIe capability and a shareware PCIe software utility. Details on the PIO example design are available in the *LogiCORE Endpoint Block Plus for PCI Express User Guide* [Ref 26].

The Endpoint Block Plus wrapper automatically connects the block RAMs, GTP/GTX transceivers, and reset and clock modules. The user can customize and generate the wrapper using a simple set of menu options in the CORE Generator GUI. The options available determine the correct attribute settings and tie off any unneeded ports.

The Endpoint Block Plus solution offers the most common, easy-to-use features to simplify the design process:

- Pre-implemented optimal buffering for high-bandwidth applications
- LocalLink User Interface for easy bridging to other Xilinx IP
- Pre-implemented PCIe Endpoint spec required features:
    - ♦ Memory BAR checking, filtering, BAR hit indication to user
    - ♦ Non-memory TLP ID checking
    - ♦ Error message generation for misrouted non-memory TLP
    - ♦ Error message generation for memory TLP BAR miss
    - ♦ Message Signaling Interrupt (MSI) controller

Figure 4, page 20 illustrates the sub-systems instantiated within the Endpoint block used by the example design. Refer to the Endpoint Block Plus Wrapper for PCI Express product page for additional information on the Endpoint solution.
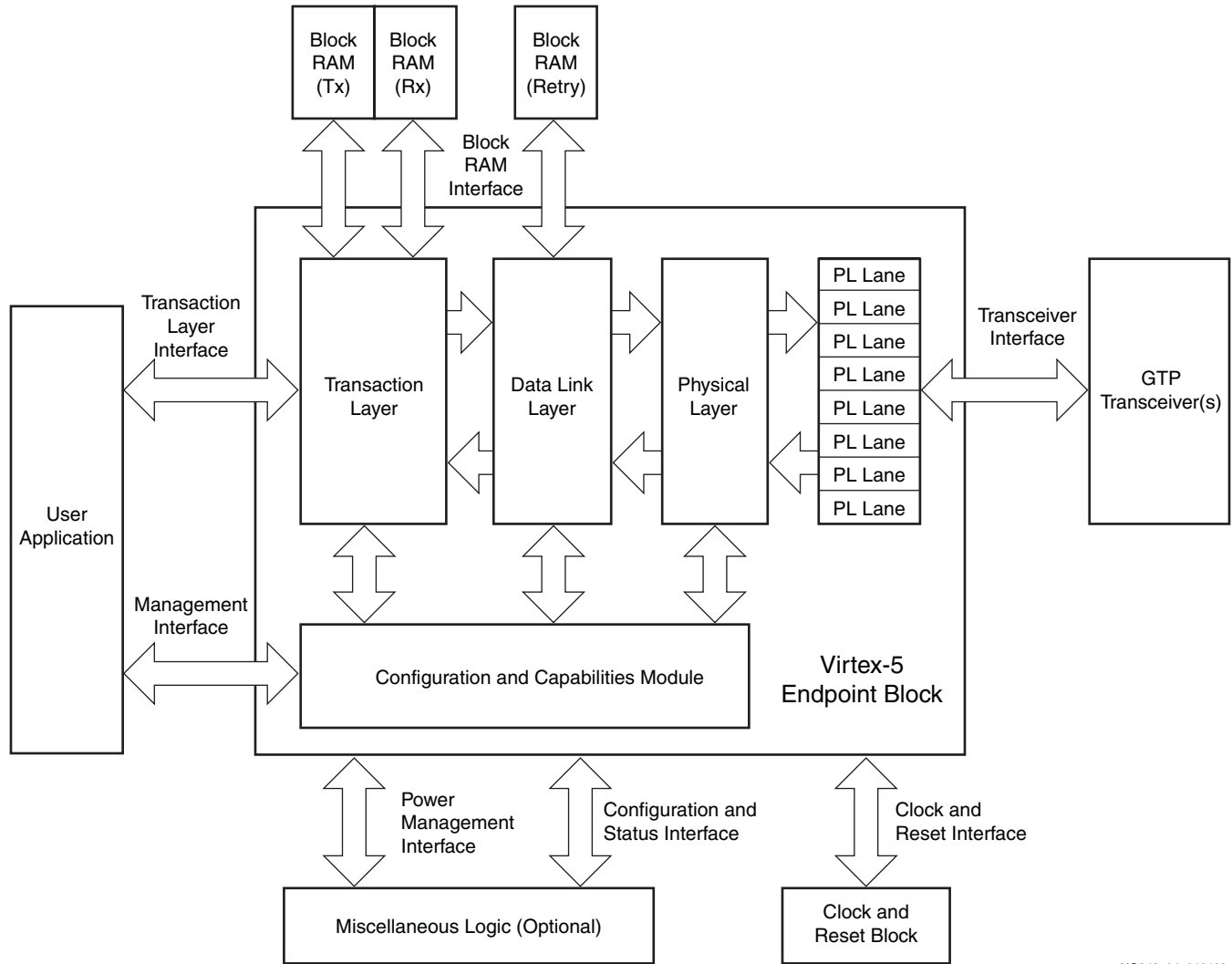
Figure 4: **Virtex-5 Endpoint Block Plus for PCIe Diagram**

System Generator for DSP Design (ML506)

The *Xilinx System Generator™ for DSP User Guide* [Ref 31] is a comprehensive document that presents designers with a methodology for performing signal processing algorithm exploration, design prototyping, and model analysis from within the high-level Simulink simulation environment. System Generator extends Simulink by allowing designs to be translated into FPGA hardware. In addition, the hardware co-simulation capability of System Generator provides the ability to run designs on a hardware development platform under the control of Simulink, while offering access to data analysis and visualization tools within MATLAB.

Numerous example designs are shown in the *Xilinx System Generator for DSP User Guide* and are available in System Generator. An example hardware co-simulation FIR filter design (Figure 5) that is available in System Generator is presented on the ML506 reference design page at:

- http://www.xilinx.com/products/boards/ml506/reference_designs.htm#sysgen_dsp
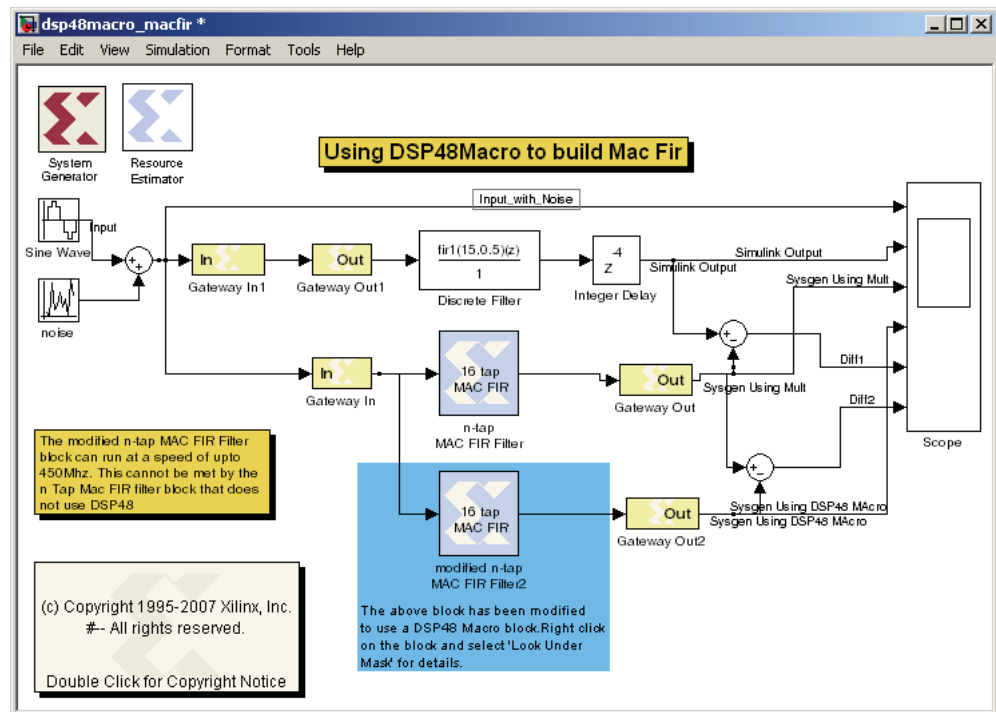
UG349_05_040408

Figure 5:   **System Generator Example Design for the ML506 Platform**

References

This section provides references to documentation supporting Virtex-5 devices, tools, and IP. For additional information, see www.xilinx.com/support/documentation/index.htm.

Documents supporting Virtex-5 FPGAs:

1. DS100, *Virtex-5 Family Overview.*
2. DS202, *Virtex-5 Data Sheet: DC and Switching Characteristics.*
3. UG190, *Virtex-5 User Guide.*
4. UG200, *Embedded Processor Block in Virtex-5 FPGAs Reference Guide.*
5. UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide.*
6. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide.*
7. UG194, *Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide.*
8. UG197, *Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs.*
9. UG193, *XtremeDSP Design Considerations.*
10. UG191, *Virtex-5 Configuration User Guide.*
11. UG192, *Virtex-5 System Monitor User Guide.*
12. UG195, *Virtex-5 Packaging and Pinout Specification.*

Documents supporting Xilinx Platform Studio (XPS):

13. UG111, *Embedded System Tools Reference Manual*
14. XTP013, *EDK Concepts, Tools, and Techniques.*
15. UG081, *MicroBlaze Processor Reference Guide.*
16. OS and Libraries Document Collection.

Documents specific to the ML50*x* Evaluation Platform:

17. UG348, *ML505/ML506/ML507 Getting Started Tutorial.*
18. UG347, *ML505/ML506/ML507 Evaluation Platform User Guide.*

Documents supporting IBERT:

19. UG213, *ChipScope Pro Serial I/O Toolkit.*
20. UG029, *ChipScope Pro Software and Cores User Guide.*

The Xilinx Memory Solutions Web page offers the following material supporting the Memory Interface Generator (MIG) tool:

21. WP260, *Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator.*
22. UG086, *Xilinx Memory Interface Generator (MIG) User Guide* (for registered users).
23. Demos on Demand, *Memory Interface Solutions with Xilinx FPGAs.*
24. Xilinx Support - Memory Interface Resources (for registered users).

Documents supporting the LogiCORE Endpoint block for PCIe solutions:

25. DS551, *LogiCORE Endpoint Block Plus for PCI Express Data Sheet.*
26. UG341, *LogiCORE Endpoint Block Plus for PCI Express User Guide.*
27. UG343, *LogiCORE Endpoint Block Plus for PCI Express Getting Started Guide.*

Documents supporting the LogiCORE SGMII solution:

28. DS550, *LogiCORE Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet.*
29. UG340, *LogiCORE Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide.*

The Xilinx DSP Resources Web page includes documents supporting the System Generator for DSP:

30. *System Generator for DSP Getting Started Guide*,
http://www.xilinx.com/support/sw_manuals/sysgen_gs.pdf

31. *System Generator for DSP User Guide,*
http://www.xilinx.com/support/sw_manuals/sysgen_ug.pdf

32. *System Generator for DSP Reference Guide*,
http://www.xilinx.com/support/sw_manuals/sysgen_ref.pdf

Documents supporting additional embedded processor and LogiCORE IP cores:

33. DS537, *XPS_LL_TEMAC (v1.00a) Data Sheet.*
   ♦ XAPP1026, *LightWeight IP (lwIP) Application Examples Application Note.*

34. DS581, *XPS External Peripheral Controller (EPC) (v1.00a) Data Sheet.*
   ♦ XAPP925, *Reference System: Using the OPB EPC with the Cypress CY7C67300 USB Controller Application Note.*

35. DS531, *Processor Local Bus (PLB) v4.6 (v1.00a) Data Sheet.*

36. DS402, *Device Control Register Bus (DCR) v2.9 (v1.00a) Data Sheet.*

37. DS577, *XPS 16550 UART (v1.00a) Data Sheet.*

38. DS606, *XPS IIC Bus Interface (v1.00a) Data Sheet.*

39. DS578, *PLBV46 to DCR Bridge (v1.00a) Data Sheet.*

40. DS444, *Block RAM Block Data Sheet.*

41. DS445, *Local Memory Bus (LMB) v1.0 (v1.00a) Data Sheet.*

42. DS641, *Microprocessor Debug Module (MDM) (v1.00a) Data Sheet.*

43. DS452, *LMB Block RAM Interface Controller Data Sheet.*

44. DS583, *XPS System ACE Interface Controller (v1.00a) Data Sheet.*

45. DS573, *XPS Timer/Counter (v1.00a) Data Sheet.*

46. DS569, *XPS General Purpose Input/Output (GPIO) (v1.00a) Data Sheet.*

47. DS572, *XPS Interrupt Controller (v1.00a) Data Sheet.*
   ♦ XAPP778, *Using and Creating Interrupt-Based Systems Application Note.*

48. DS481, *Util Vector Logic Data Sheet.*

49. DS484, *Util Bus Split Operation Data Sheet.*

50. DS575, *XPS Multi-CHannel External Memory Controller (XPS MCH EMC) (v1.00a) Data Sheet.*

51. UG081, *MicroBlaze Processor Reference Guide: MicroBlaze (v7.00a).*

52. DS614, *Clock Generator (v1.00a) Data Sheet.*

53. DS406, *Processor System Reset Module (v2.00a) Data Sheet.*

54. DS616, *PLBV46 PCI Full Bridge (v1.00a) Data Sheet.*

55. DS643, *Multi-Port Memory Controller (MPMC) Data Sheet.*