XILINX®

WP202 (v1.3) January 10, 2005

The Advantages of Migrating from Discrete 7400 Logic Devices to CPLDs

How often do you hear that the typical PC system is more powerful than the supercomputer of only two decades ago? While this is an amazing testament to the advances of computing technology over the last 20 years, you hear very little about another less visible, yet equally remarkable trend: one complex programmable logic device (CPLD) and a little code can replace literally hundreds of discrete logic components.

Discrete logic devices, long considered the workhorses of the semiconductor industry, held a unit cost advantage over programmable logic devices for several decades. However, times have changed significantly. Advances in semiconductor process technology for CPLDs have driven the costs of these devices down to a point where they now offer a highly compelling discrete logic replacement alternative.

Background

Driven by greatly compressed product development cycles, rapidly changing standards, and feature explosion, the prevailing trend in digital design over the last

decade has been to continue to move away from discrete logic devices in favor of CPLDs. Not only will this trend continue, but also it will accelerate.

The purpose of this paper is to bring to light the reasons why it makes sense today—both cost-wise and strategically—to migrate from discrete logic devices to CPLDs. To accomplish this, we provide a side-by-side comparison of discrete logic devices with CPLDs. Our comparison considers production costs, board area savings, operating performance, reliability, time to market, programmability, electromagnetic interference, and design security. We also provide a brief overview of how Xilinx programmable logic device technology addresses these issues.

TTL Logic Comes of Age

Discrete TTL logic technology gained almost universal acceptance after Texas Instruments introduced their TTL 74XX family of integrated circuits in 1962 to support NASA's lunar-landing and space exploration programs. That family included logic gates, such as the 7400 quad NAND, flip-flops, the 7474 twin D-type flops, the 74160 decade counter, binary adders, and other simple subfunctions, all of which were available in 14- or 16-pin integrated circuit packages.

Advances in discrete logic component packaging and the introduction of devices with ever-increasing levels of integration enabled designers to minimize board space and the number of components while providing them with almost "Lego Block" like simplicity. New families were continually introduced to address the need for higher performance, lower power, and reduced cost. The result is more than 33 different 7400 families, each offering its own unique permutation of power, performance, price, and features.

Through the 1970s, TTL variations came rapidly. However, along with the rampant proliferation of multiple 7400 series came complexity. By the early '80s, a veritable alphabet soup of logic family variants had been released—TTL, S, LS, AS, F, ALS, CD4000, HC, HCT, BCT, AC, ACT, FCT, ABT, LVT-A, AHC, AHCT—forcing designers to require a scorecard to keep track of which family best fit each application.

Not only were there many different types of 7400 families to choose from, but the number of members within a family and the different speed grades, plus the package and feature options proliferated to the point where today there are well over 500,000 unique 7400 devices.

The Emergence of CPLDs

While there were many 7400 devices to choose from—perhaps far too many—a revolutionary trend began to appear in the form of programmable logic devices (PLDs). Delivering user programmability, the first generations of these chips replaced five to ten logic devices. As logic integration improved, PLDs were able to replace more and more standard logic functions. Today, the highest-density CPLDs contain 10,000 gates and are capable of integrating large numbers of 7400-series logic devices.

However, consistent with higher levels of integration, first-generation CPLDs came at a higher price. The culprit: the die costs associated with the inherent overhead associated with CPLD programmability. Calculating cost is fairly straightforward: the device price is directly proportional to the number of devices (or dice) that can be yielded from a single silicon wafer. As the example in Figure 1 shows, if you were to

assume a wafer cost of $3000 and a yield of 300 dice per wafer, the cost of each device is $10.

$3000/wafer
3000 devices/wafer
$1/device
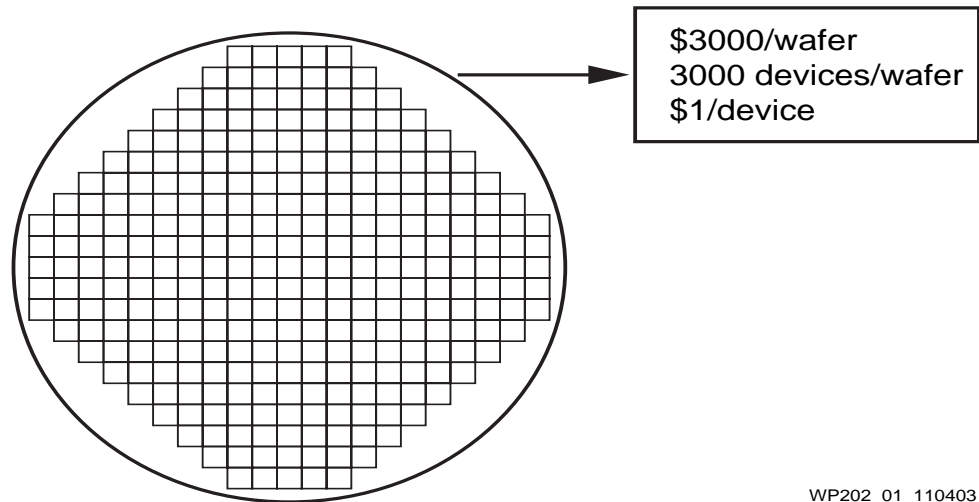
WP202_01_110403

Figure 1: **Basic Semiconductor Cost Model**

For larger die sizes, cost becomes a major concern based on the fact that silicon wafers are not perfect, and, in fact, they have defects. The probability that a die will not yield due to a defect on the die increases exponentially as the die size increases. Thus, the cost of a larger die increases exponentially beyond a certain point. These factors, in the past, led to higher CPLD product costs when compared to discrete TTL devices.
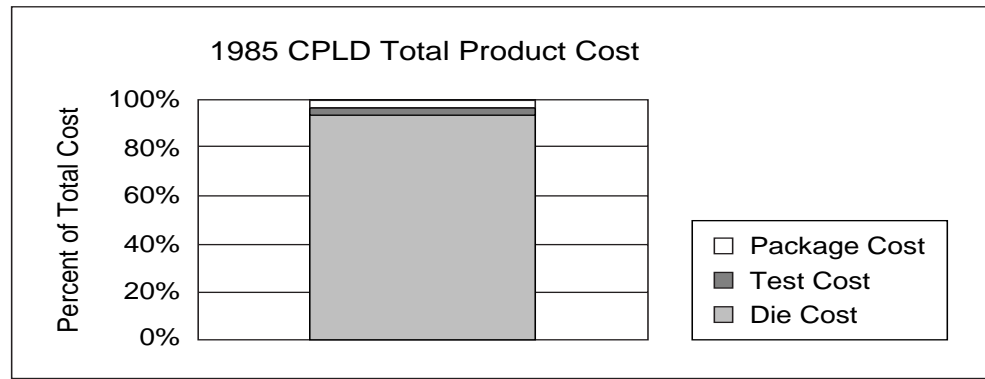
Die Size vs. Cost
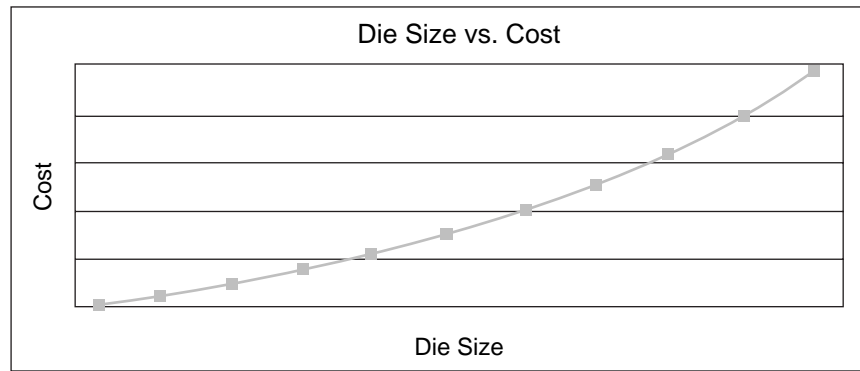
Cost

Die Size

Die cost as a function of die size

WP202_02_110403

Figure 2: **Die Cost As a Function of Die Size**

In addition to die cost, other costs, including device packaging and product testing add together to form the total product cost as shown in the chart in Figure 3.

Total product cost = die cost + test cost + package cost

WP202_03_110403

Figure 3: **IC Total Product Cost**

Traditionally, this high cost structure restricted the use of CPLDs primarily for pre-production prototyping or other limited-volume applications. Today, this situation has changed dramatically.

CPLD: The Clear Discrete Logic Replacement Choice

When the 7400 series was first introduced, there was a significant premium to be paid for integration. In 1963, the average price for a single 7400 device was $1000 (in 1963 dollars!). While the situation improved over the years, in 1968 the average price for a 7400 device had dropped to only $25 (in 1968 dollars). The concept that an integrated circuit would eventually be cheaper than the same circuit constructed from discrete transistors and resistors would have been thought highly unlikely.

Through the years, however, improvements in semiconductor process and packaging technologies leveled the playing field to where it was actually cheaper to use the highly integrated 7400 series device over the discrete transistor implementation. In effect, integration was free!

Historically, 7400-series devices had low unit costs relative to CPLDs. However, once again, technology improvements have rewritten the cost equation, allowing CPLDs to gain equal, if not better, footing against TTL devices. That is, the unit costs of CPLDs have been driven down to the point where they are equal to or even below those of discrete logic devices. In addition, as the diagram in Figure 4 shows, if you compare

the cost of a logic circuit implemented using discrete 7400 devices to one using CPLDs, time and again the CPLD wins, hands down.
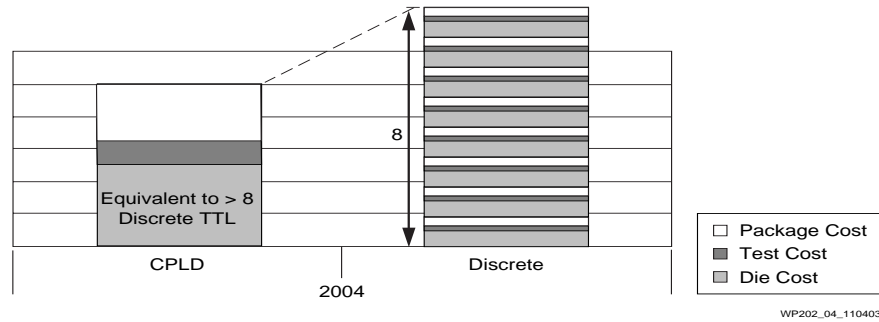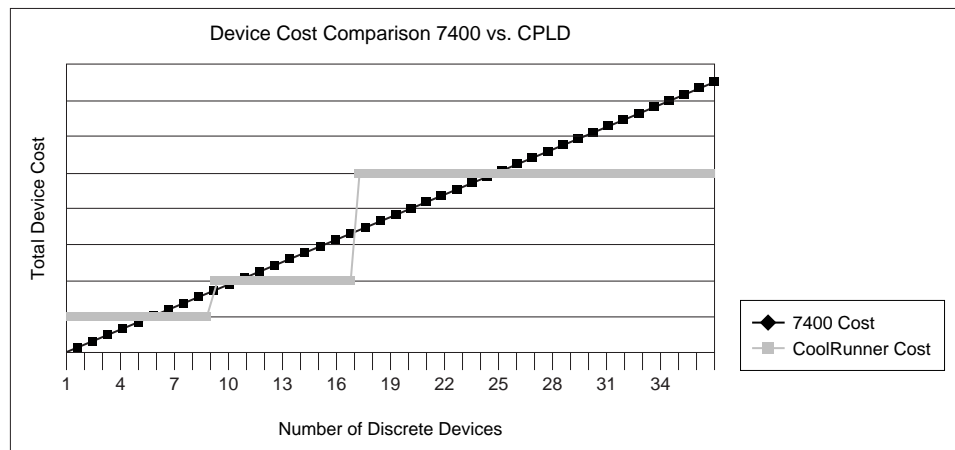

Equivalent to > 8 Discrete TTL

CPLD

Discrete

2004

□ Package Cost
■ Test Cost
■ Die Cost

WP202_04_110403

Figure 4: **7400 vs. CPLD Device Cost Comparison**

Further, factoring in the high hidden costs underlying discrete logic devices—which include increased inventory, low reliability, high power consumption and EMI, prolonged time to market, and higher maintenance—makes CPLDs the clear, superior alternative to discrete 7400 series devices.

Device Cost Comparison 7400 vs. CPLD

Total Device Cost

Number of Discrete Devices

1 4 7 10 13 16 19 22 25 28 31 34

◆ 7400 Cost
■ CoolRunner Cost

Cost comparison: 7400 discrete pricing versus CPLDs

WP202_05_110403

Figure 5: **Basic Discrete 7400 vs. CPLD Comparison**

The remainder of this paper presents a comparison of discrete logic devices to CPLDs, based on the following:

- Total system costs
- Time to market
- Programmability
- Reliability
- Electromagnetic interference

- Design security capabilities

Discrete Logic versus CPLD Devices

Closing the Cost/Performance Gap

To support the premise that CPLDs provide a lower total cost alternative, in this section we compare the costs of a discrete logic component-based circuit with those of a Xilinx CPLD. The discrete logic circuit used for comparison (shown in Figure 6) is a straightforward memory controller that provides equal functionality as one Xilinx 32-macrocell XC2C32 CoolRunner-II CPLD. To make the comparison as complete as possible, we cover both DIP and SMT packaging for the discrete circuit, and compare these against the Xilinx CPLD in a VQ44 package.
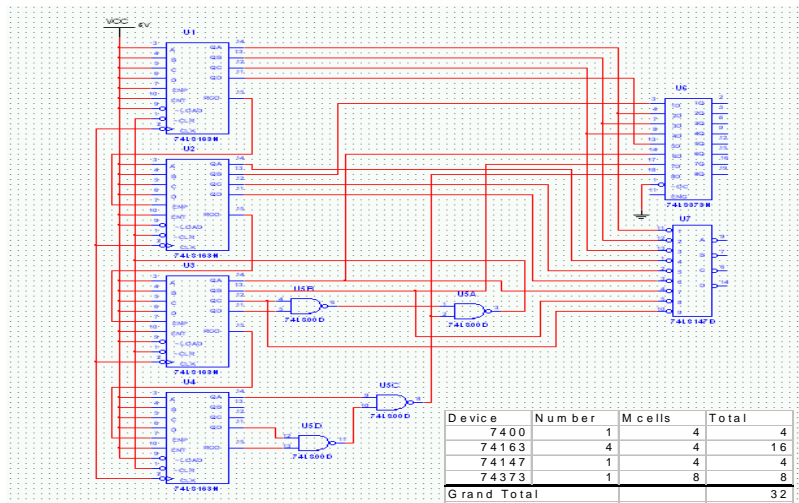

Device	Number	Mcells	Total
7400	1	4	4
74163	4	4	16
74147	1	4	4
74373	1	8	8
Grand Total			32

Figure 6: **Sample Circuit for Cost Analysis**

When comparing costs between technology alternatives, it is important to consider the total system costs, that is, the *real* cost of the solution. Accordingly, our analysis provides a detailed breakdown of all costs, starting with production costs, and then comparing the costs associated with total PC board area, power consumption, and the number of board layers.

Production Costs

Production costs are broken down by logic component unit costs, discrete resistor/capacitor costs, PCB board area cost, assembly/insertion, and inventory.

Table 1: **Production Cost Comparison**

Cost/Packaging	Discrete Circuit		Xilinx CPLD, XC2C32
	DIP	SMT	VQ44
Logic component costs	$1.36	$1.93	$0.90
Discrete resistors & capacitors	$0.66	$0.66	$0.18
PCB material[1]	$3.62	$3.77	$2.12
Assembly/Insertion[2]	$0.72	$0.75	$0.42

www.xilinx.com
1-800-255-7778

Table 1: **Production Cost Comparison** *(Continued)*

	Discrete Circuit		Xilinx CPLD, XC2C32
Cost/Packaging	**DIP**	**SMT**	**VQ44**
Inventory[3]	$1.75	$1.93	$0.75
TOTAL	**$8.11**	**$9.04**	**$4.37**

1. Cost derived from quotes from multiple PCB vendors for 4-layer discrete boards and 2-layer CPLD boards. Size of board: 3 x 3 inches. Quantity: 1,000/month, 2-week lead time.
2. Assembly/insertion costs are 20 percent of PCB material costs.
3. Inventory costs are 25 percent of total material costs.

As Table 1 shows, for the circuit used in this analysis, the total cost for one Xilinx CPLD is much less than one-half of the cost of the same circuit using 7400 series devices. Besides lower unit production costs, additional savings for CPLD-based designs are realized through reduced component count, including interfacing resistors, decoupling capacitors, additional PCB real estate, and assembly/insertion costs.

Although not quantified in this analysis, CPLDs gain an additional cost advantage through:

- Ability to inventory one line of CPLDs for multiple applications. This reduces the number of individual part numbers to be traced and handled.
- Lower availability risks and low minimum order quantities (MOQ)
- Reduced expediting costs and production delays incurred by parts shortages.
- Avoiding lost revenues because of lack of component availability or down production lines

Board Area Savings

When compared with discrete logic components, CPLDs require fewer components and thus less board area and fewer layers. As the Table 2 shows, the total board area costs alone are a fraction of those for the discrete circuit. Further, the fewer devices required for the CPLD leads to lower power consumption and improved reliability. In addition, lower heat dissipation avoids the need for cooling fans and heat sinks. The table provides the details behind these factors, comparing and quantifying the cost impact.

Table 2: **Board Area Comparison**

	Discrete Circuit		Xilinx CPLD
Function/Pkg	**DIP**	**SMT**	**VQ44**
Component area (in^2)	1.298	0.760	0.150
PCB area (in^2) consumed by components[1]	1.6874	0.988	0.195
Cost of board area[2]	1.6874 in^2 x $0.40/ in^2 = $0.67	0.988 in^2 x $0.42/ in^2 = $0.41	0.195 in^2 x $0.24/ in^2 = $0.05
Cost/layer differential ($0.75 per layer)	4 layers x $0.75 = $3.00 total	4 layers x $0.75 = $3.00 total	2 layers x $0.75 = $1.50 total

Table 2: **Board Area Comparison** *(Continued)*

Function/Pkg	Discrete Circuit				Xilinx CPLD	
	DIP		SMT		VQ44	
Power consumption (Quiescent vs. Active)	150mW	1750mW	150mW	1750mW	.029 mW	1.6 mW
Total cost of power usage (@ $0.40/watt)[3]	$0.06	$0.07	$0.06	$0.07	1.16×10^{-5}	6.4×10^{-4}
Reliability	29.951 FIT		29.951 FIT		1.000 FIT	

1. This is the total PC board area consumed by only the components, which was calculated to be equal to the total component area plus 30 percent.
2. Cost derived by dividing board unit costs (from Production Cost chart) by 9 square inches (3x3 board): $3.62/9 for DIP, $3.77/9 for SMT, and $2.12/9 for CPLD.
3. The power cost of $0.40 per watt is considered by experts to be an industry standard cost.

Other CPLD Cost Advantages

As discussed in the remainder of this document, CPLDs further drive down the total cost of ownership and deliver key advantages through:

- **Fast time-to-market** – Being first to market counts. In fact, every four weeks of delay results in 14 percent loss of market share.[1] 7400 device availability and design changes that occur late in the product development or manufacturing cycle can significantly impact market share.

- **Reprogrammability** – CPLDs cannot only get to market faster, they stay in the market longer, enabling an expanded revenue stream. In addition they enable:
  - Remote bug fixes and feature upgrades that avoid costly hardware changes
  - Shorter development cycles thus avoiding board re-spins resulting from "features creep" or unnoticed bugs
  - Reduced development time being spent on reworking and maintaining old designs

- **Reliability** – By employing a lower number of devices over the discrete TTL equivalent circuits, CPLDs provide a significantly improved FIT rate, indicating a remarkable high level of reliability.

- **Electromagnetic interference** – CPLDs lower EMI levels, thus reducing the high cost and high risk of meeting EMI compliance.

- **Design security** – CPLDs offer a significant security advantage over TTL devices as they can employ bit-stream protection, preventing design read-back and reverse engineering.

---

1. John Chambers, Cisco

Additional assumptions:
- Logic density: 32 macrocell
- Discrete circuit consists of:
  - (1) electrolytic capacitor (power)
  - (7) ceramic capacitors (decouple)
  - (6) ¼-watt pull-up resistors
- Standard commercial operating environment
- Power consumption data assumes frequency of 25 MHz

www.xilinx.com
1-800-255-7778

Time-to-Market Benefits

The proliferation of electronic wireless, industrial and communication devices, as well as ever-shrinking product life cycles continue to put pressure on companies to get their designs from concept to production as soon as possible. When you look at the cost of being late, it's easy to see the motivation behind being first on the market.

As the graph in Figure 7 illustrates, late market entry has a larger affect on profits than development cost overruns or a product price that is too high. This is especially true in highly competitive markets and those that have short market windows. According to Mckinsey & Co., even if within budget, products that are six months late earn 33 percent less profit over five years.
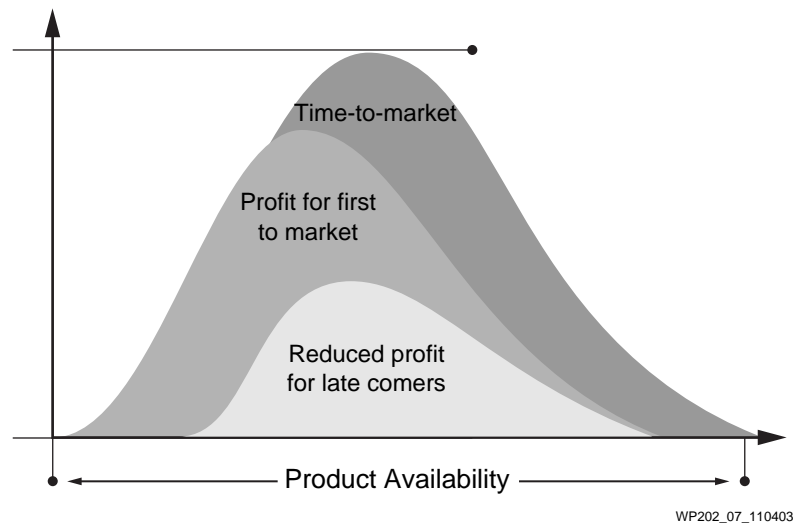

WP202_07_110403

Figure 7: **Xilinx CPLD Time-to-Market Benefits**

Unfortunately, designs that employ discrete 7400 devices are at the mercy of several barriers that not only prolong time to market, but add complexity and costs, and reduce reliability. These barriers include:

- A long manufacturing, assembly, test, and debug cycle that is susceptible to delays and multiple design decisions that can directly impact board layout.
- The lack of easy-to-use design tools makes debugging and maintenance tedious chores.
- The high number of TTL components required in discrete designs introduces availability risk. In many cases, components might be out of stock or even obsolete.

CPLDs, on the other hand, provide designers with numerous advantages that enable designers to react to last-minute design changes and compress time to market. These include component inventory reduction, faster production cycles, efficient device and board testability, and the ability to modify designs during all phases of design and production.

Programmability: The Real Advantage

While time to market is a major benefit, the ability to program and reprogram devices as designs change is equally important. Unlike CPLDs, once a PCB using discrete TTL devices is laid out and goes into production, typically it cannot be altered or upgraded without ripping out components and going through board re-spins.

Another major advantage of CPLDs is quick system upgrades and bug fixes in the field. As a result, designers can easily integrate exactly the logic functionality needed

without adding "cuts and jumps" on the PCB. For example, imagine a scenario where automobile manufacturers can add new functions to in-car systems by allowing consumers to dial up and purchase upgrades over the phone to reconfigure the system. In addition, CPLDs help avoid board redesigns and scrapped parts when specific programs are cancelled.

The reconfigurable nature of CPLDs also enables a single product footprint to implement multiple product personalities. That means manufacturers can standardize on a single PCB footprint and package, and thus quickly leverage economies of scale through reduced inventory overhead. Further, reprogrammability reduces the deployment of design resources for maintaining old designs, which allows engineers to focus on introducing new products and features.

Reliability

Reliability is another area that should not be overlooked when analyzing total system costs, especially since 7400-based systems introduce higher complexity with more components, interconnects, layers, handling—and thus, lower overall reliability. In addition, because discrete components are typically larger and require more board real estate, and have a significant number of external chip-to-chip interconnects, they increase power consumption and EMI which further heightens failure risks.

In contrast, CPLD-based systems require fewer components and layers. The reduction in components and layers reduces PC board layout density, lowers heat dissipation, reduces EMI levels, and thus greatly decreases Failures In Time (FIT).

Electromagnetic Interference

Electromagnetic interference (EMI) refers to any type of interference that can potentially disrupt, degrade, or otherwise interfere with authorized electronic emissions over approved portions of the electromagnetic spectrum. EMI problems are often complex, and their solutions illusive. Ideally, EMI compliance should be an integral part of the board design. Unfortunately, resolution of EMI problems is often ignored until it's too late.

EMI Causes

EMI originates from the switching of digital circuits. Two factors are necessary for EMI to exist: a noise source or transmitter, and a propagation path or antenna. On a PCB, noise can come from frequency-generating circuits, component radiation, ground bounce, poor impedance control, or cable interconnects. The propagation path is the medium that carries the energy, such as free space or metallic interconnects. Antennae are the elements that both transmit and receive unwanted interference.

Impact of EMI

Concern over EMI continues to grow as the FCC and international compliance regulations clamp down harder on pollution of the electromagnetic spectrum, thus making it is an issue that requires system designers' attention.

To system designers, EMI compliance carries a cost and high risk, as it can easily prolong the product introduction. Typically, various techniques are employed to minimize radiated emissions, including use of ferrite beads, shielded enclosures, or series-terminating resistors—all of which drive up costs and reduce board yield and reliability. EMI analysis is tedious and involves numerous variables, making problems difficult and expensive to fix once the board is moved into production (FCC compliance testing alone is $400 per hour). The effectiveness of EMI emissions reduction strategies can be determined only once the product is in the lab. In addition,

10
www.BDTIC.com/XILINX
www.xilinx.com
1-800-255-7778
WP202 (v1.3) January 10, 2005

what might appear to be a good solution to one problem may cause a new problem to occur. In fact, it's not uncommon to take several passes to achieve EMI compliance.

Given the large number of components, traces, and board layers, TTL-based designs are more susceptible to high EMI, compared to CPLDs. By contrast, CPLDs significantly reduce EMI through fewer external components, and other "free" features including: programmable I/O slew rate, programmable ground, programmable I/O signaling, and phase-locked loops. These free features provide a marked improvement in reducing EMI emissions.

Design Security Issues

Given the explosion of new applications in the competitive electronics market, the need to protect designs from unscrupulous competitors has never been greater. CPLDs offer several unique advantages that safeguard system designers against code theft.

Unlike discrete logic devices which are extremely susceptible to reverse engineering—which is as simple as reading the part number directly from the device—CPLDs inherently require a user-defined bit stream which easily prevents customer read-back.

More elaborate security schemes that exploit reprogrammable capabilities of CPLDs to keep attackers at bay are also possible. For example, the CPLD design or password can be altered on a regular basis—hourly, if necessary—to seriously hamper an attacker's ability to reverse engineer the design. Exploiting the reprogramming features of CPLDs is thus a logical and efficient way to defend against design theft.

Xilinx CPLD Advantages

The Xilinx CoolRunner-II CPLD family utilizes second-generation RealDigital™ technology to provide high performance, advanced features, and low power consumption, all at a very low price. Featuring a 100 percent digital core, up to 385 MHz performance, and low standby current, CoolRunner-II CPLDs offer a wide range of densities, as well as abundant I/O, the flexibility to move from one density to another in the same package, and the lowest cost per I/O pin in the industry.

The advanced system features in CoolRunner-II devices allow you to integrate multiple discrete functions, reduce costs, lower power consumption, increase reliability, reduce EMI, and shrink your time to market through:

- **Advanced I/O technology** – Support for multiple I/O standards allows you to easily create standard chip-to-chip and chip-to-memory interfaces and thus remove discrete devices from your system, saving you money and increasing system reliability.

- **Superior clock management** – the Clock Doubler enhances performance by doubling the internal clock speed up to 400 MHz. The Clock Divider improves power savings by providing clock division at standard values. CoolCLOCK combines the Clock Divider and Clock Doubler and is a key feature in reducing EMI.

- **Comprehensive design security** – Designs can be secured during programming to prevent either overwriting or pattern theft via readback. Electrical or visual detection of configuration patterns is eliminated with four levels of on-chip security. Electrical or laser tampering causes the device to lock down automatically. Protection is buried deep within the device, making it virtually undetectable.

- **DataGATE** – DataGATE reduces power consumption by eliminating unnecessary toggling during times of irrelevant data on the input pin.

- **Advanced packaging** – The small footprint Chip Scale Package (CSP) is ideal for space-constrained applications. For cost sensitive applications, the TQFP, PQFP, VQFP, and PLCC packages offer the ultimate packing solution. Fine line BGA packages are optimal for applications that demand high performance.

The combination of advanced I/Os, superior clock management, comprehensive security options, and advanced packing choices provides real world interfaces at 7400 price points that allow designers to meet any challenge.

Summary

Since their introduction in the late '70s, programmable logic devices have proven to be very popular. In fact, they are now one of the fastest growing sectors in the semiconductor industry. The migration to PLDs, and eventually CPLDs, has been an intriguing, four-decade evolution, starting with discrete logic circuits that were constructed from transistors and resistors to the introduction of the 7400 series first-generation TTL technology.

However, just as the 7400 series replaced early generation discrete transistor-based logic designs, advances in semiconductor process technology are enabling CPLDs to offer a clear, cost-effective alternative to 7400-based logic systems. No longer held hostage to low densities and high die costs, CPLDs pack more functionality into ever-shrinking die geometries, offering compelling benefits of low-cost on-the-spot reprogrammability, short lead times, higher performance, expanded densities, and unmatched flexibility.

Xilinx CoolRunner CPLDs consume less power and offer reprogrammable flexibility with unprecedented design security – without a price premium. The result is a scalable technology that gives you a superior solution for a wide range of high-volume applications, such as PDAs, cell phones, routers, and high-speed Internet modems.

For more information about CPLDs as well as the programmable devices solutions from Xilinx, visit www.xilinx.com.

Additional Information

For information on how much 7400 logic can be placed on a Xilinx CPLD, see **White Paper 214**, *TTL "Burn Rate" for Xilinx CPLDs.*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/14/03	1.0	Initial Xilinx release.
1/5/04	1.1	Updates to Table 1 on page 7.
9/1/04	1.2	Addition of appendix clarifying macrocell usage.
01/10/05	1.3	Added link to White Paper 214.