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Using Non-standard I/O Voltages with CoolRunner-II CPLDs

By: CPLD Applications

Xilinx CoolRunner™-II CPLDs support the EIA/JEDEC LVTTL 3.3V and LVCMOS 3.3V, 2.5V, 1.8V and 1.5V I/O standards(1). This document addresses questions concerning the use of 2.8V (+/- 5%) and 3.0V (+/- 5%) I/O levels with the Xilinx CoolRunner-II CPLDs. The document also provides guidance in the operation of Xilinx CoolRunner-II CPLDs at non-standard voltages. *The I/Os are designed such that they will not physically break by applying voltages not specified in the data sheet, but because we do not test the parts at these levels during production, Xilinx cannot make guarantees.*

1. 1.5V I/O (LVCMOS15) is supported with Schmitt Trigger inputs only.

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Leakage

How will leakage current be affected at these voltage levels?

Leakage current will remain as per the device specification as long as the input makes a full rail to rail swing, from GND to the applicable V_{CCIO} voltage.

AC Timing

What AC Timing parameters should be used for these two voltages?

The I/O voltages in question lie between the LVCMOS25 and LVCMOS33 specification; therefore, the worst case between these two should be used. An example would be:

Table 1: **AC Timing Parameters**

Symbol	Parameter	Speed Grade		Unit
		-6	-7	
T_{IN}	Standard Input Adder	0.6	0.7	ns
T_{HYS}	Hysteresis Input Adder	1.5	3.0	ns
T_{OUT}	Output Adder	1.2	1.4	ns
T_{SLEW}	Output Slew Rate Adder	3.0	4.0	ns

V_{IL} and V_{IH}

What V_{IL} and V_{IH} specifications should be used for these two voltages?

The I/O voltages in question are between the LVCMOS25 and LVCMOS33 specification; therefore, the worst case between these two should be used, which would be:

V_{IH} (Min.) = 2.0V; V_{IL} (Max.) = 0.8V.

Figure 1 shows the I_{OH} and I_{OL} curves at V_{CCIO} = 2.85V.

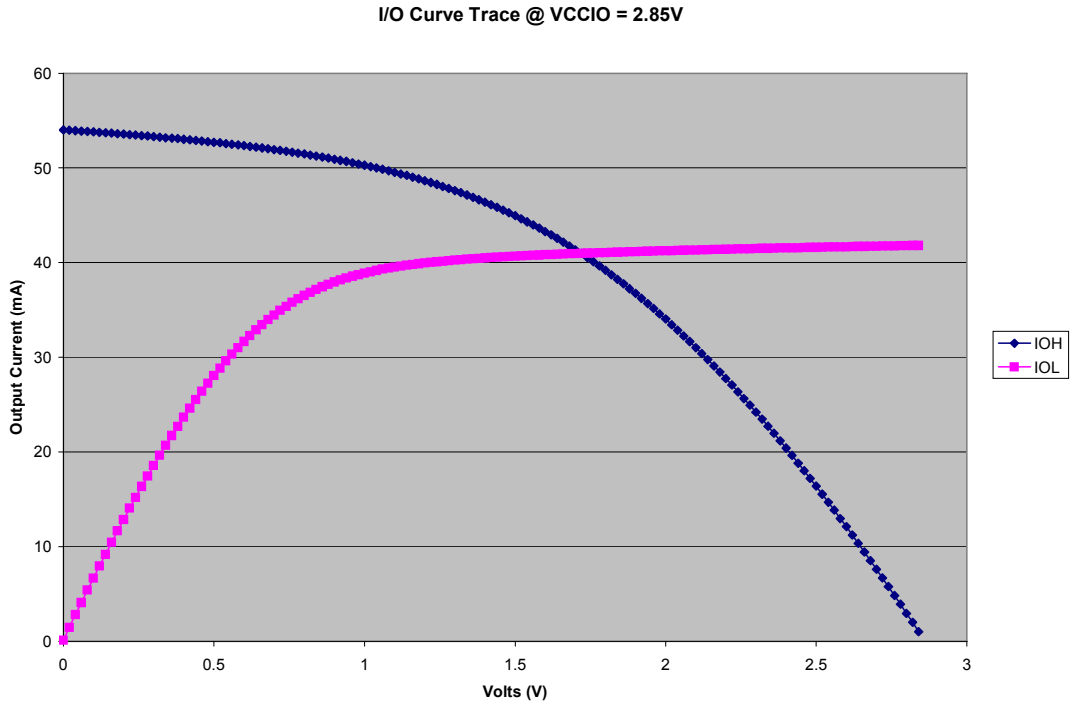

Figure 1: **I_{OH} and I_{OL} Curves at 2.85V (typical, room temperature)**

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I/O Standard

Which I/O standard should be specified in the software?

Either LVCMOS25 or LVCMOS33 will work.

Conclusion

While you can use 2.8V (+/-5%) and 3.0V (+/-5%) I/O with a CoolRunner-II device as shown in the guidance given in this white paper, our devices are not tested at these voltages during production, and so Xilinx cannot make any guarantees.

Additional Information

CoolRunner-II Data Sheets, Application Notes, and White Papers

XAPP382, CoolRunner-II I/O Characteristics

XAPP785, Level Translation using Xilinx CoolRunner-II CPLDs

Device Packages

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/07	1.0	Initial Xilinx web release.
04/13/07	1.1	Change to introduction, page 1. Change to conclusion, page 3.

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