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Virtex-5 Family Advanced Packaging

By: Panch Chandrasekaran

The exacting technological demands created by increasing bandwidth requirements have given rise to significant advances in FPGA technology that enable engineers to successfully incorporate high-speed I/O interfaces in their designs. One aspect of design that plays an increasingly important role is that of the FPGA package. As the interfaces get faster and wider, choosing the right package has become one of the key considerations for the system designer.

This white paper discusses some of the advantages made available to the application design engineer by the Virtex™-5 family's advanced approach to FPGA packaging.

Introduction

There are a few key considerations that come into play while designing high-bandwidth interfaces:

- Hundreds of I/Os toggling in tandem can result in Simultaneously Switching Output Noise (SSN).
- I/O placement plays an important role in determining the PCB signal trace design. Depending on the banking structure, more PCB layers could be required, complicating the design process.
- Hundreds of switching I/Os also stress the power supply distribution system. Extra care is needed to filter out the power supply noise in order to mitigate noise-related failures.

Virtex-5 Package for Simplified High-Performance Design

FPGA packaging today affects many more aspects of system design than in the past. This section describes some of the aspects of the Virtex-5 packaging and its impact on PCB design.

Sparse Chevron Pinout Pattern for Minimal Noise

The key to minimizing SSN is to lower the package inductance. The pinout pattern of the FPGA package determines the loop inductance. In a Virtex-5 package, every signal pin is adjacent to a GND/V_{CC} (return) pin, and the ratio of signal pins to a return pin is just 4:1. This abundance of return pins, along with pin distribution for small loop area, provides for desirable low-impedance return paths. This reduces the inductance of the signal path from 15.6 nH down to 4.9 nH, helping to maintain noise performance several times better than with traditional package designs. Figure 1 shows the pinout of a Virtex-5 package.

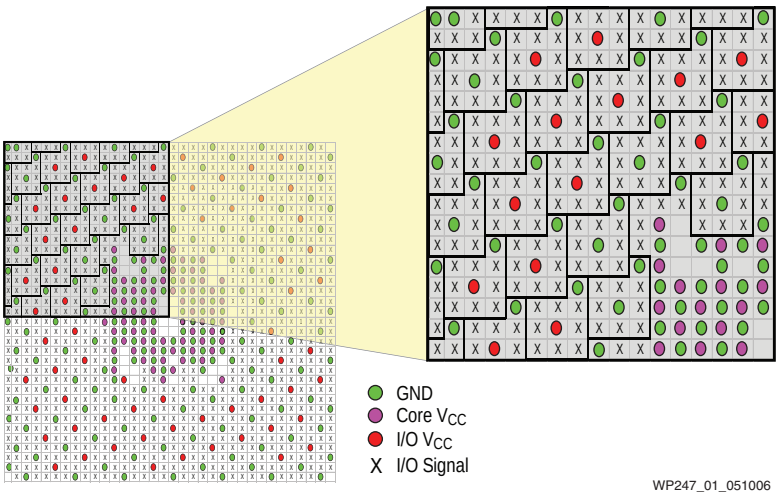

Figure 1: **Virtex-5 Package Pinout**

Narrow Banking Structure for Easy Signal Breakout

Figure 2 shows the difference between traditional banking structure and the improved Virtex-5 banking. In the past generations, I/O banks have typically been divided into quads or octets along the centre of the package. Using this banking scheme, two I/Os

within a bank can be physically far apart (one along the periphery of the package and another closer to the center). With this scheme, the different signals within a bus often have different trace components — different layers, additional vias, and so on. This has negative implications for PCB layout, layer stack-up, and signal integrity.

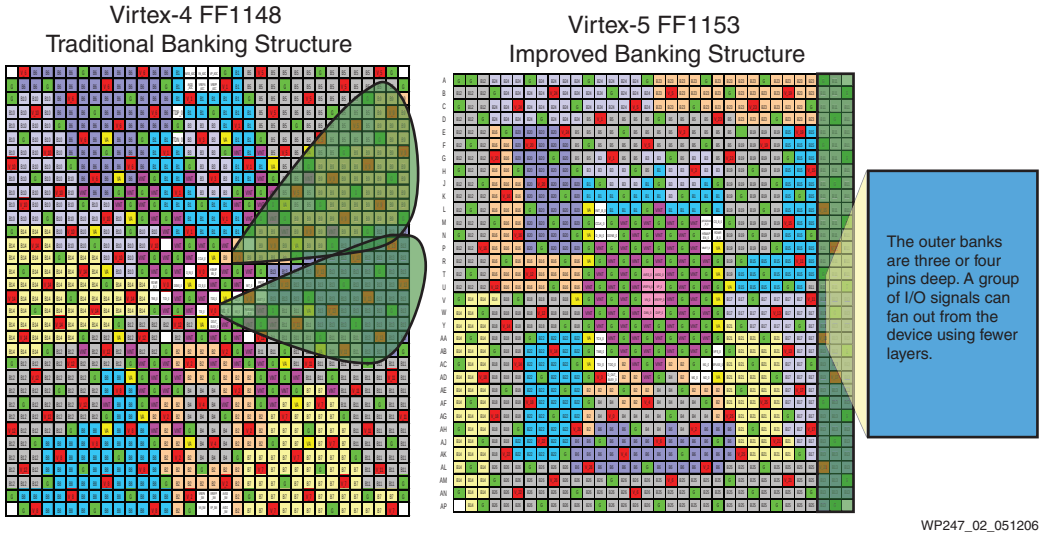

Figure 2: **Virtex-4 vs. Virtex-5 Banking Structure**

In the Virtex-5 package banking structure, the outer banks are three or four pins deep; up to eight banks can thus reside along the periphery of the package, enabling easy breakout into the PCB. This helps better control trace impedance characteristics, and offers potential savings in the number of PCB layers.

On-Chip Decoupling Capacitors for Cleaner Power Supplies

As bit periods and logic voltage levels shrink, noise on the power supply impacts the integrity of the link to a greater degree. When hundreds of I/Os are switching (common in a large FPGA system), care must be taken to maintain a clean power supply. This is usually done with an extensive decoupling network to cover the range of frequencies involved. But this also increases the component count and the PCB footprint, adding to the cost burden. Virtex-5 packages are equipped with on-package medium- and high-frequency decoupling capacitors for effective power filtering. This maximizes the performance of the interface and reduces the number of external decoupling capacitors on the PCB.

Grouping of Related V_{CC} Pins for Reduced PCB Layers

In the Virtex-5 package, related V_{CC} pins are not intermingled, as in traditional package designs. This new approach offers a few benefits. Different voltages can be laid out in the same PCB layer, as opposed to the three or four layers often required by a traditional pinout scheme. The impact of the V_{CC} pin partitioning on PCB design is illustrated in Figure 3. This also means less copper area is required to connect the V_{CC} vias to the regulator and PCB decoupling capacitors.

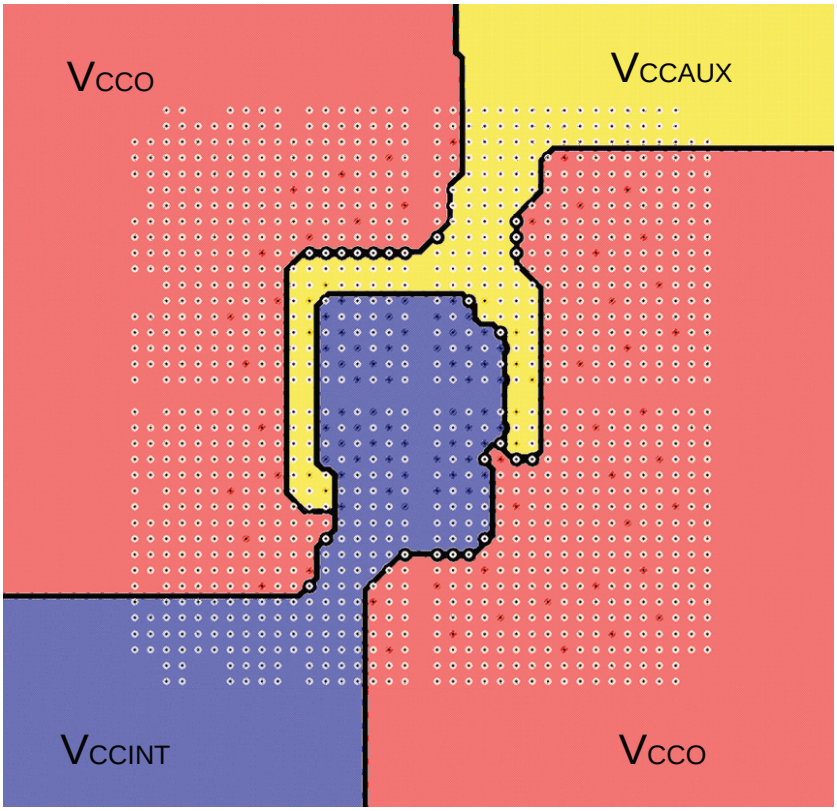

Figure 3: **Grouping of Related V_{CC} Pins in Virtex-5 Devices**

Conclusion

The package design of a high-performance FPGA affects more aspects of design than in the past. The Virtex-5 package has been designed for optimal system design, maximizing high-speed interface performance and simplifying PCB design.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/12/06	1.0	Initial Xilinx release.