XILINX®

WP264 (v1.0) May 4, 2007

Using CoolRunner-II CPLDs in Digital Video Applications

By: CPLD Applications

Everywhere one turns in the world today there are screens providing us with critical information. Whether in the home, the car, the train station or the grocery store, there is a need for a screen of some shape and size to display information of some kind. Production of Flat Panel displays earned revenue of approximately $65 billion in 2005 and is expected to rise aggressively to over $120 billion by 2012. As all these displays have different characteristics and are displaying information from different sources, there are a huge number of variables in this market. It is these variables that make programmable logic a perfect solution to the presented problems.

This White Paper aims to show how Xilinx CoolRunner^{TM}-II CPLDs can be used in various digital video applications. Because of the fast-paced market, new features are introduced quickly and being the first to be able to incorporate a new feature gains manufacturers a significant advantage over

www.BDTIC.com/XILINX

www.xilinx.com

their competitors. Xilinx programmable logic devices are a perfect fit in these systems due to their extremely low power consumption, ultra low cost and freedom from non recurring engineering costs (NRE) associated with ASIC design. They guarantee to reduce the BOM cost, improve the end product time to market and ensure flexibility throughout the product life cycle.

CPLD Architecture

The CoolRunner-II CPLD is a highly uniform family of fast, low-power devices. The underlying architecture is a traditional CPLD architecture, combining macrocells into function blocks interconnected with a global routing matrix, the Xilinx Advanced Interconnect Matrix (AIM). The function blocks use a PLA configuration that allows all product terms to be routed and shared among any of the macrocells of the function block.

Design software can efficiently synthesize and optimize logic that is subsequently fit to the function blocks and connected with the ability to utilize a very high percentage of device resources. The software easily and automatically manages design changes, exploiting the 100% routeability of the PLA within each function block. This extremely robust building block delivers the industry's highest pin-out retention under very broad design conditions.

The design software automatically manages device resources so that you can express your designs using completely generic constructs, without needing to know the architectural details. If you're more experienced, you can take advantage of these details to more thoroughly understand the software's choices and direct its results.
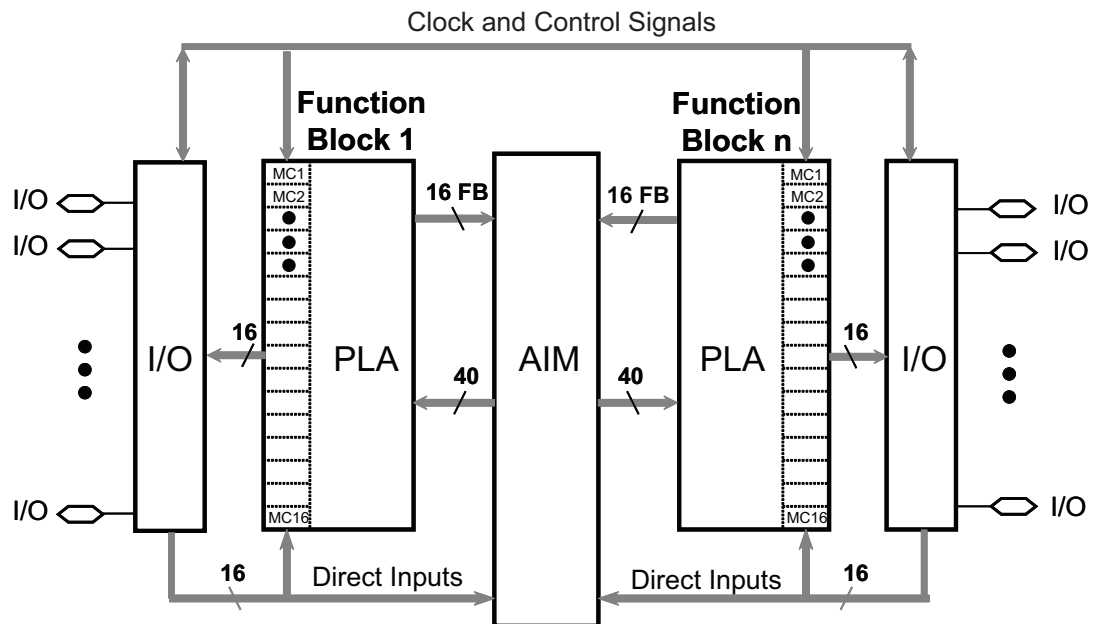

Figure 1: **CoolRunner-II Architecture**

Figure 1 shows the high-level architecture whereby function blocks attach to pins and connect to each other within the internal interconnect matrix. Each function block contains 16 macrocells.

CPLDs are widely used as voltage interface translators; thus, the I/O pins are grouped in large banks. The four smaller parts have two output banks. With two banks available, the outputs will switch to one of two selected output voltage levels, unless both banks are set to the same voltage. The larger parts (384 and 512 macrocell) support four output banks, split evenly. They can support groupings of one, two, three, or four separate output voltage levels. This kind of flexibility permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V in a single part.

CPLD Basic Display Generator

Digital component video is represented in two primary color spaces, RGB and YCbCr. The major difference between the two is the way they represent color. YCbCr comprises of two color difference signals and a brightness signal, whereas RGB comprises red, blue and green signals. The signals that make up the YCbCr color space are the brightness or luma, Y, the blue chroma, Cb, and the red chroma, Cr.

Different forms of YCbCr are used in industry for standard definition television and high definition television or HDTV. The specifications are governed by the International Telecommunications Union (ITU) Radiocommunication Sector. The standard ITU-R BT.601 is the form of YCbCr that was developed for standard definition television and ITU-R BT.709 for HDTV.

YCbCr is used everywhere that MPEG compressed data is found, for example, digital television, set top boxes and DVDs. The first example below will take an encoded YCbCr data stream and use a CoolRunner-II CPLD to perform additional functions on the data.

The first example shows how a CoolRunner-II CPLD can generate and display basic images onto a screen. The simplest pattern that can be displayed is a single color on the entire screen. Taking the VSYNC and HSYNC signals generated by an encoder IC, the CoolRunner-II CPLD can be both a YCbCr sequence generator and a color generator. See Figure 2 shows the block diagram.
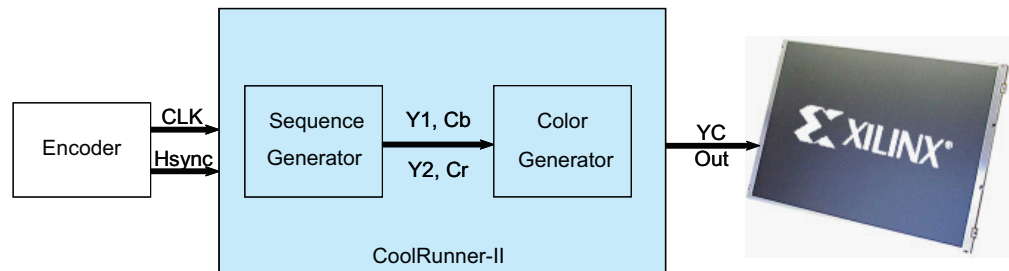

Figure 2:   **Sequence and Color Generator**

This color raster generator can be further enhanced by generating a window from the VSYNC and HSYNC signals. By counting the pixels and lines, a framed box can be generated and displayed on the screen. Figure 3 shows the block diagram.
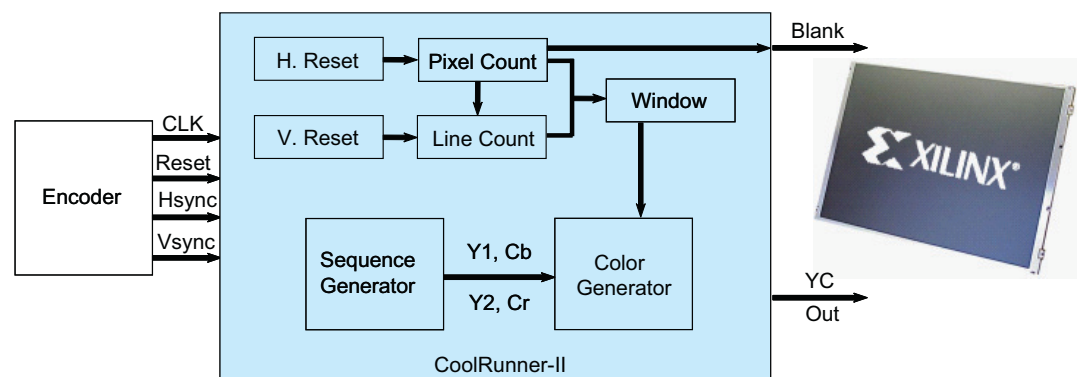

Figure 3:   **Enhanced with Window Generation**

This circuitry can easily fit inside a 256 Macrocell CoolRunner-II device (XC2C256) with space to spare. The remaining resources can be used to add further control logic to allow the user to change colors as well as modify the brightness and contrast of the screen.

Now that we have a feeling for the CPLD architecture and what can fit inside a device, we can see where else CPLDs can be used in digital video applications.

CPLDs in Digital TV System

The primary advantage of LCD or Plasma displays over traditional CRT displays is the reduction in size. Whereas a CRT occupied a whole corner of a room, an LCD can be hung on any wall able to take its weight. However, there are also an increasing number of features being incorporated into modern displays. For example, traditionally, there were only one or two sources providing data to a screen. With popularity of digital TV over various different media, it is common that a display could have three (digital terrestrial, cable and satellite), four (as above with two different satellite inputs) or more sources which need to be managed. Figure 4 shows a block diagram of a typical digital TV system. The blue blocks show where a Xilinx CPLD can be used to bind the system together and incorporate additional features. Each blue block represents a single application that can be implemented in a CPLD. Due to the flexible, programmable nature of the CPLD architecture, multiple applications can easily be incorporated into the same device.
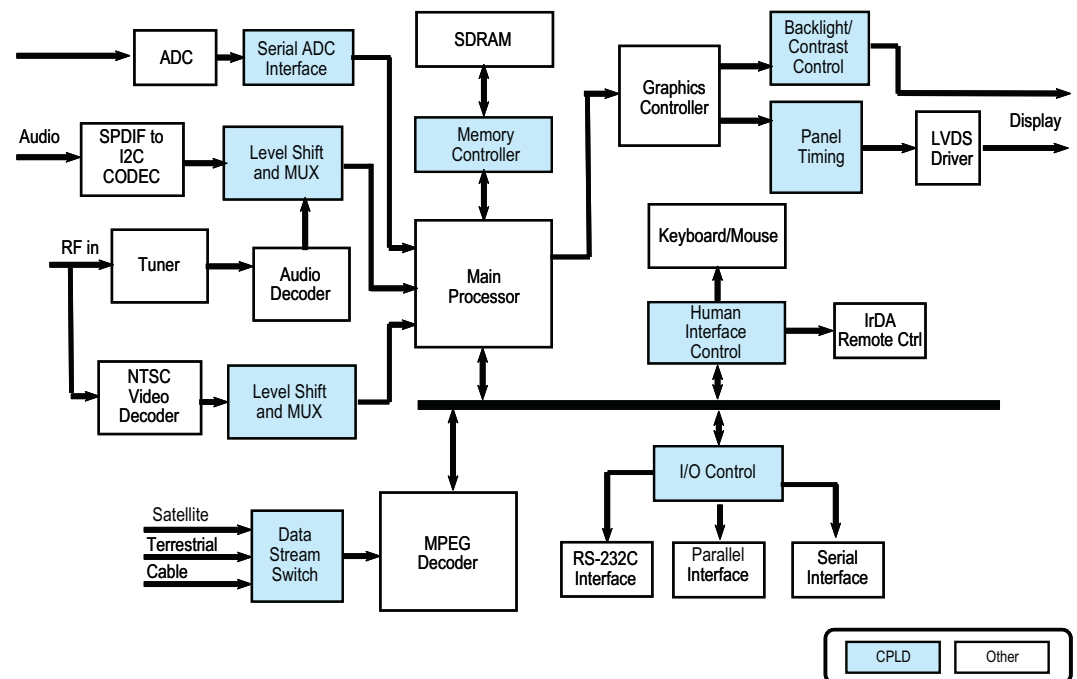
Figure 4: **CPLDs in Digital TV System**

Serial ADC Interface

Analog-to-digital converters (ADC) are used to transform analog information, such as audio signals or measurements of physical variables into a form suitable for digital handling. ADC are present in every system that uses both analog and digital signals.

They are available in a variety of resolutions from 8-bit through to 16-bit with various sampling rates and different interface on the digital side. It is because of this great variation in properties of the ADC that using a CPLD as the Serial ADC Interface is ideal. The design inside the CPLD can easily be modified to interface a different ADC to the main processor if a change is required. An example of using a Xilinx CPLD as a Serial ADC Interface can be seen in Xilinx Application Note **XAPP355**.

Memory Controller

SDRAM is essential in most processor based systems and is available in various data bus widths and clock speeds. Similarly to the ADC, the wealth of different types and sizes of SDRAM on the market makes a CPLD the perfect solution to interface to the memory as the CPLD contents can quickly and easily be modified to interface to a different memory. Application Notes **XAPP384** and **XAPP394** show how CoolRunner-II CPLDs can interface to DDR and Mobile SDRAM respectively, showing that the CoolRunner-II CPLD is capable of system frequencies of 100 MHz and above required by this type of memory.

Human Interface Control

TV sets are now as much functional items for watching images as they are fashionable items that must look good when hanging on a wall offering ease of use at the same time. Often all control will be performed through the remote control handset over IrDA, which is capable of data transfer rates from 2.3 kb per second up to 16 Mb per second. However, there are still sometimes buttons, jog wheels and various LEDs that need to be monitored and controlled. A Xilinx CPLD is perfect at performing these functions as outlined in **XAPP345** (IrDA Design in CoolRunner) and **XAPP805** (Driving LEDs with CPLDs).

Data Stream Switch

It is common for multiple sources, such as cable, satellite and digital terrestrial to provide data to a single display. This data is usually provided by a decoder in an MPEG2 Transport Stream, with a typical clock speed of 27MHz. The Transport Stream consists of 8 bits of data (TS_DATA) and 3 control bits (TS_CLK, TS_SYNC and TS_VAL). **XAPP944** shows how a Xilinx CoolRunner-II CPLD can quickly and easily switch between different Transport Streams with minimal loss.

Level Translation and System Integration

Whenever there are systems with multiple components, it is inevitable that there will be some issues getting all the components talking to each other. For this reason, it is common to find Xilinx CPLDs performing the appropriate translation between the different communication protocols. In the example of a digital television system, there are multiple protocols travelling at different frequencies around the system. Figure 4 shows the CPLD being used to integrate some of the audio circuitry over I^2C at 3.4 Mb per second as well 27 MHz NTSC decoder output to the main processor. The 27 MHz NTSC decoder clock is typically upscaled from a 14.318 MHz crystal, and the resulting 27 MHz clock can be shared with the clock for the MPEG2 portion of the system. **XAPP785** goes into further discussion about using Xilinx CPLDs to perform level translation.

Panel Timing and Backlight Control

Performing timing control for LCD panels is a common use for Xilinx CPLDs. This builds on the example earlier in this document in which a CPLD was acting as a basic display generator. Figure 5 shows a typical example of a CPLD acting as timing control for a panel. It is fed the HSYNC, VSYNC and RGB signals which it reformats into odd and even signals. The backlight control usually takes the form of a pulse width modulated (PWM) signal— a signal with modulated duty cycle. As the change in the brightness of backlight does not need to be a particularly fine grained, this portion of the design is unlikely to consume many resources within the CPLD.
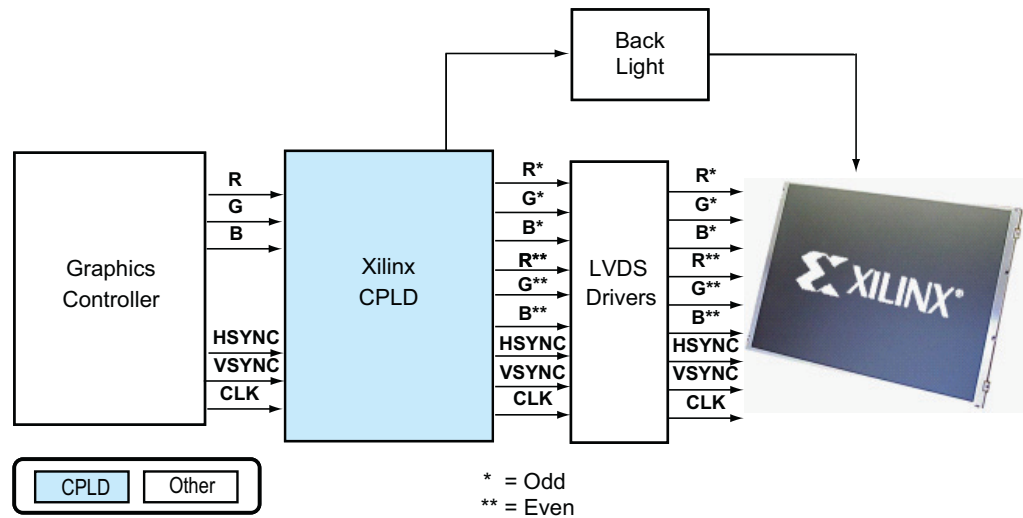

Figure 5:   **Timing Controller**

Of course the panel timing control and backlight control can be incorporated into the same design as the YCbCr sequence generator at the beginning of this document in order to provide a timing and display controller.

CPLDs in Set Top Box

A set top box is a device that enables an external signal source to be decoded and converted into a format that can be used by a display. Sometimes, these are embedded

www.BDTIC.com/XILINX

inside the TV display but it is still commonplace to require an external device to receive and decode signals. Figure 6 shows a set top box block diagram.
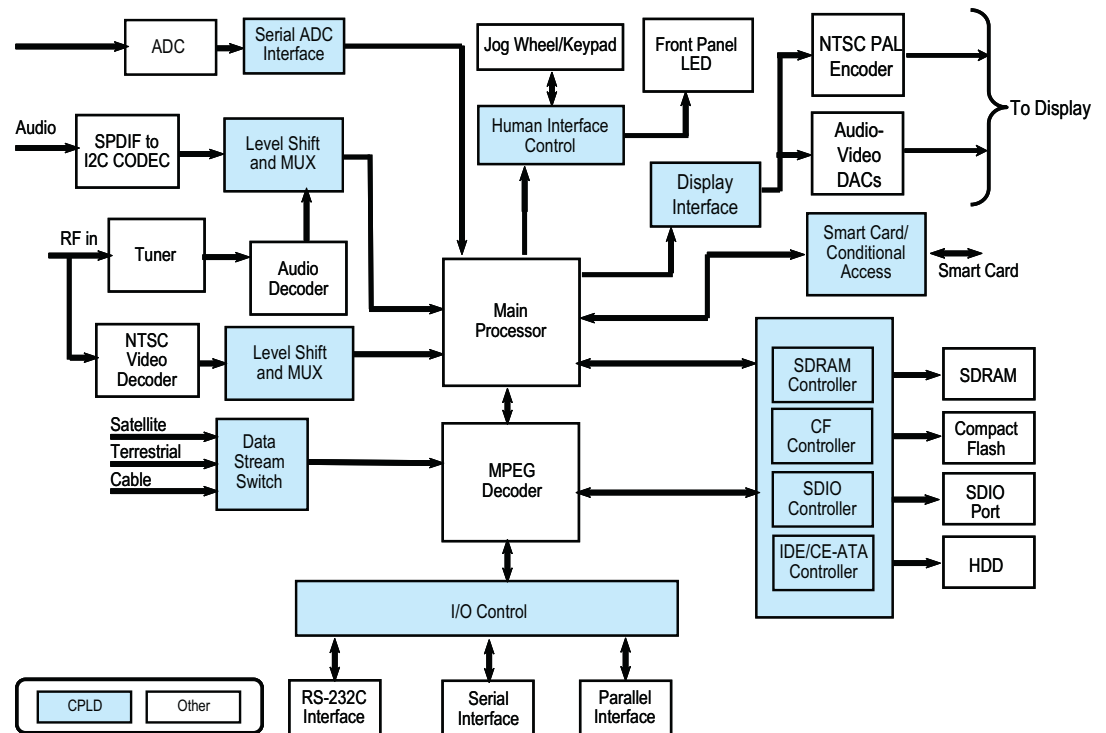

Figure 6: **Set Top Box Block Diagram**

In addition to some of the features present in a digital display, the set top box will likely have more human interface control, additional memory card interfaces, Hard Disk Drive interface and some sort of conditional access, usually a smart card. CPLDs can be used to perform a wealth of different memory interfaces as is shown in:

- **XAPP354 – NAND Flash Controller**
- **XAPP398 – Compact Flash Card Interface**
- **XAPP906 – Supporting Multiple SD Cards**

Often certain channels or features are enabled using a smart card; a credit card sized plastic card with an embedded microprocessor and memory. Acting like a mini-computer, smart cards allow money and information to be electronically stored and transferred in a secure but portable medium. When inserted into a reader or passed over a scanner, the smart card transfers data to and from a central computer. Overall, it is a replacement for old means of retaining data and transacting business. XAPP372 shows how Xilinx CPLDs can be used to read from Smart Cards. The typical clock speed in a Smart Card application depends on the television encoding system used. The two most popular encoding systems are NTSC, predominately used in North America, and PAL, predominately used in Europe and Asia. In both cases, the typical system speed is in the region of 4 to 5 MHz.

Other functions such as human interface and system integration may seem trivial but are essential to the system functioning correctly. Remember that one CPLD can be used to perform multiple independent functions so if there is already a CPLD performing a specific function in a system and there are resources available, then those resources can easily be used for another purpose such as scanning a keypad, driving

some LEDs or some other logical function. As all CoolRunner-II CPLDs have multiple IO banks that can be powered at different voltages, level translation is available free of charge. For more information see:

- **XAPP512 – Keypad Scanner**
- **XAPP785 – Level Translation**
- **XAPP805 – Driving LEDs with Xilinx CPLDs**

Digital Video in Mobile Phone Handsets

Television is available everywhere nowadays, so much so that many new mobile phone handsets are able to receive mobile TV broadcasts. There are several standards competing for acceptance in the market with the main two formats being DVB-H and DMT.
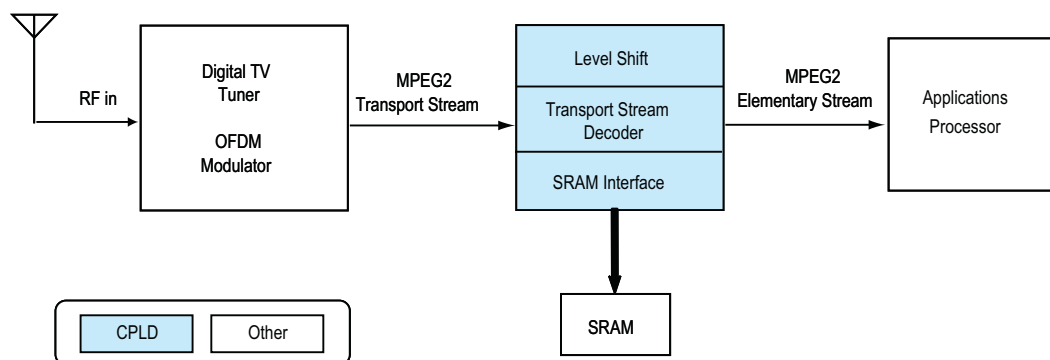

Figure 7: **CPLD in a Mobile Phone**

Mobile TV is broadcast using Orthogonal Frequency Division Multiplexing, a technique well suited to transmitting large amounts of digital data over radio waves. A Mobile TV enabled handset will incorporate a Digital TV Tuner that includes an OFDM modulator. The output of the Tuner/Modulator module is typically in the MPEG2 Transport Stream (TS) format. A CPLD is the ideal solution to perform the conversion from TS into the Elementary Stream (ES) that the applications processor requires to be able to use the data. There are plenty of resources available in the CPLD after implementing the decoding functionality that an SRAM interface, for caching the data, can be included. As the CoolRunner-II CPLD has two IO banks, the level shifting between the Tuner and the Applications Processor can be performed without adding extra overhead or extra cost. See Figure 7.

Conclusion

The demands of the digital consumer market are very tough. Consumers demand that manufacturers incorporate the newest features into their products for the lowest possible cost. Of course there are many potential solutions to the different problems that are presented to designers on a day to day basis. The advantage of programmable logic as a whole and specifically Xilinx CPLDs is that they can be used to incorporate a new feature into an application with minimal design effort. As they are completely reprogrammable throughout their lifetime, they also offer a great opportunity to upgrade the application in the field.

Due to their flexibility, Xilinx CoolRunner-II CPLDs are found in a variety of digital video products including Digital TV sets and Set Top Boxes and it is predicted that this success will continue to increase as the quantity of new features and different standards being released is rising rapidly. Offering extremely low power, extremely low cost and very high performance, CoolRunner-II is the market leading programmable logic product for the digital consumer market.

References

1. Digital Video Electronics, Andrei Cernasov
2. **International Telecommunication Union**
3. **White Paper 196: Xilinx Devices in Flat Panel Displays**
4. **Frost and Sullivan report**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/04/07	1.0	Initial Xilinx release.