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Slash Your Total Cost by up to 50% with Spartan-3 Generation FPGAs
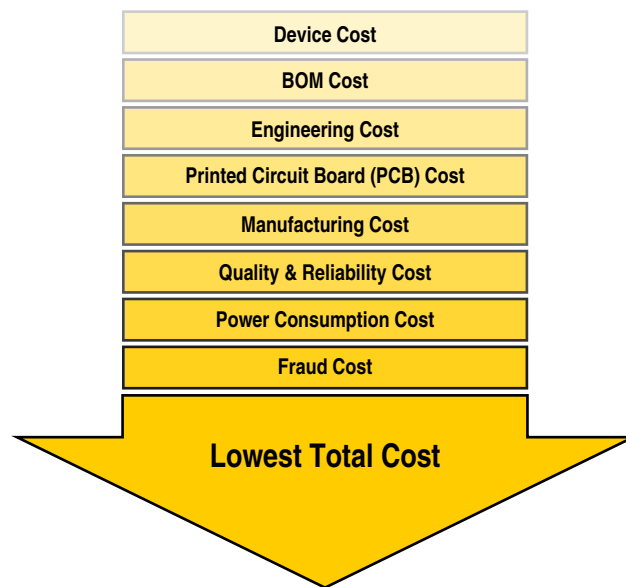
By: Vivek Sardana

Xilinx® Spartan®-3 generation FPGAs were conceived to deliver the lowest total cost for high volume applications. Those companies providing product in the high-volume application market space know that to thrive, they must have the ability to deliver feature-rich, high performance, and low power products while remaining extremely cost-competitive. As a supplier of over 50 million, 90 nm low-cost FPGAs to this market, Xilinx provides the industry's most widely adopted low-cost FPGAs. We understand that in addition to material costs, companies must also reduce engineering and manufacturing costs. Furthermore, time-to-market is extremely critical as any delay can seriously impact a product's success in the marketplace.

This white paper highlights the elements that enable Spartan-3 FPGAs to slash total cost by up to 50% compared to competing FPGAs.

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So What is "Total Cost" Anyway?

It is interesting to note that after driving a car for several years, the total cost of ownership is substantially more than what was paid to the dealer. Of course, the sticker price is important—it tells the buyer what price must be paid to drive the car off the lot. But that is not all. The buyer is also concerned, and rightfully so, with other cost factors as well: gas mileage, regular maintenance, repair costs, safety features, resale value, and other expenses. These are just some of the other factors that add to the car's *total cost of ownership*.

The costs associated with an FPGA in a high volume application are similar. In addition to low device cost, the designer will evaluate the FPGA's impact on other levels as well—the complexity of board design, the additional components required, engineering design cost, scalability across multiple product versions, manufacturing cost, quality, time-to-market, and protection from fraudulent manufacturing, among others (Figure 1). Total cost goes way beyond just the device cost or the cost of acquisition. Our customers demand a cost-structure that gives them the competitive edge to succeed in their business. The *total cost* in this context refers to the **total cost of doing business**.

<div align="center">

Device Cost
BOM Cost
Engineering Cost
Printed Circuit Board (PCB) Cost
Manufacturing Cost
Quality & Reliability Cost
Power Consumption Cost
Fraud Cost

Lowest Total Cost

</div>

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Figure 1:   **The Components of Total Cost**

# Spartan-3 Generation FPGAs Deliver Lowest Total Cost. Period.

The unique combination of integrated on-chip features and cost-effective process technology enable Spartan-3 generation FPGAs to deliver the *industry's lowest total cost*. Period.

Up to 50% Lower Total Cost

Lowest Cost Devices

At the heart of the Spartan-3 generation FPGA's lowest-total-cost model is a fundamental belief that one-size-fits-all solutions can't optimally address the diverse

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range of high-volume application requirements. To avoid resource waste, silicon solutions must have the right mix of on-chip attributes including logic, I/Os, DSP capabilities, non-volatile memory, security and power management for the targeted *domain* of applications.

Mainstream
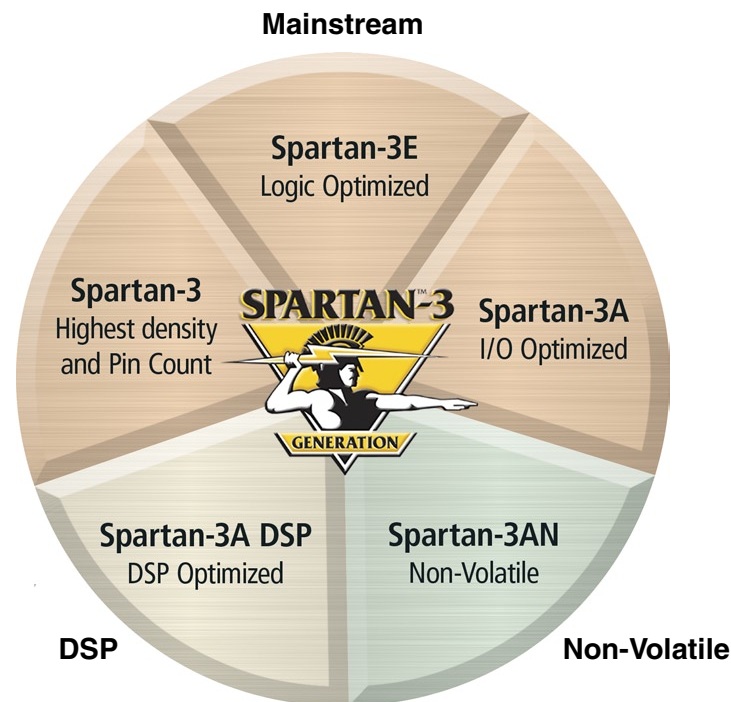
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*Figure 2:*   **Multiple Domain-optimized Platforms of Spartan-3 Generation**

With five domain-optimized platforms (Figure 2), the Spartan-3 generation boasts the industry's largest selection of devices and packages, ensuring an optimal match for every customer requirement. The advantage for designers is that they do not have to make compromises; they can choose the most cost-effective device that best serves their application.

Spartan-3 generation devices are fabricated using a mature, high-yield 90nm process technology offering excellent economies-of-scale. This benefits the customer by providing the lowest unit cost for the FPGA device.

Reduced Bill of Materials

With the objective of reducing the system design burden for our customers, Spartan-3 generation FPGAs integrate innovative features onto the chip to significantly reduce the number of external components required in a system (Figure 3). Several key attributes differentiate Spartan-3 generation devices from competitive solutions:

• Fewer power rails require fewer voltage regulators

• Tolerant VCC specifications allow use of inexpensive regulators

• Robust LVCMOS and LVTTL drivers eliminate the need for output buffers and line drivers

• Noise resistant circuits eliminate or minimize the need and expense of ferrite beads and decoupling capacitors
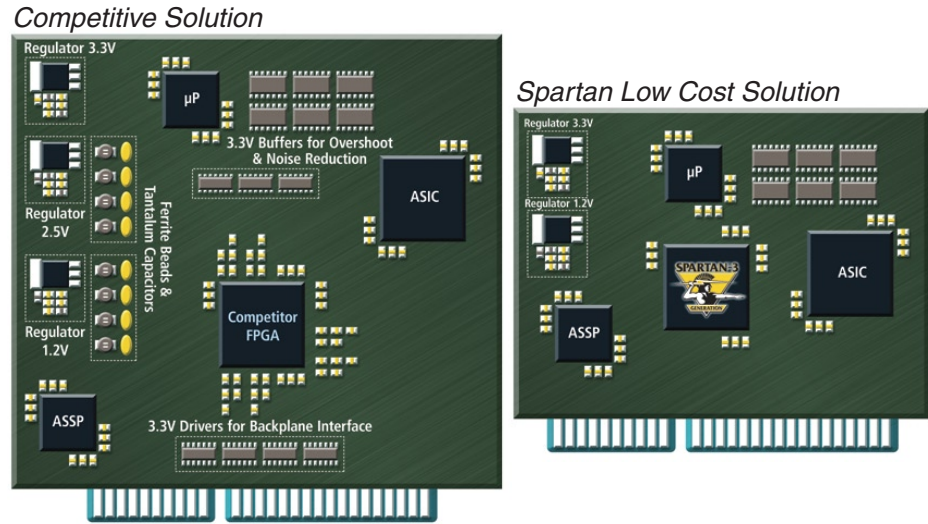
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Figure 3: **With Fewer External Components, Spartan-3 Generation FPGA Systems Significantly Lower The Bill Of Materials (BOM) Cost**

Component costs for embedded applications can be further reduced by using the MicroBlaze™ processor core in place of an external processor. The MicroBlaze processor core is easily integrated into the FPGA, and enables a wide range of flexible solutions. Inventory cost and complexity can also be reduced because this flexibility encourages the use of the MicroBlaze processor core as a common embedded architecture across multiple products.

Cost-effective Engineering Design

The thriving ecosystem of Spartan-3 generation FPGAs (Figure 4) helps designers to focus on their primary function—conceiving and designing successful products. This ecosystem includes:

Xilinx IP Library: Xilinx provides the industry's most comprehensive IP library—8 times larger than the nearest competitor. Xilinx IP blocks are pre-tested and can easily be "dropped" into a design. They are available for a variety of functions including communications and networking, DSP, storage, math, microprocessors and peripherals, audio/video image processing, and memory, among others. Using this library, designers can significantly reduce time-to-market.

Development kits and boards: These are available for all Spartan-3 generation platforms and can give system designers a head-start for evaluation and prototyping.

Development Tools: A comprehensive tool suite is also available to support all phases of the design cycle. This includes the industry's only free, fully-featured FPGA design solution, ISE® WebPACK™ software.

Services and Support: Engineers can also benefit from Xilinx world class service and support when addressing their unique application requirements.

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Figure 4: **Spartan-3 Generation FPGA's Thriving Ecosystem Reduces Time-to-market**

Simpler and Smaller Board Designs

Spartan-3 generation FPGA based boards are much simpler than competitive offerings because they need fewer external components for the system design (Figure 5). Board layout and routing is less complicated, allowing customers to considerably shorten their development cycle. Boards can be smaller, with less complicated routing, and fewer layers—a big benefit for reducing costs.
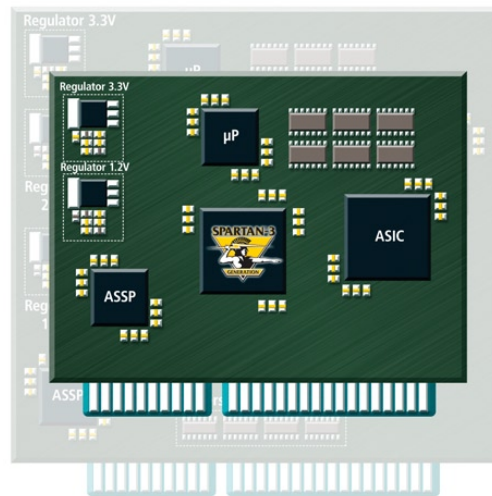
Figure 5: **Spartan-3 Generation FPGA-based Boards are Simpler and Smaller than Competitive Solutions**

The density-migration option, enabled through a wide range of supported packages, is yet another cost-saving perk available to system designers. Because the same package is available with different device densities, designers can easily "scale-up" or "scale-down" their designs for multiple product models/generations without having to re-spin their boards.

Reduced Manufacturing Cost

When products are associated with a high volume manufacturing environment, the entire manufacturing flow has to be efficient with respect to time and cost. Fewer

components in Spartan-3 generation FPGA-based systems simplify the logistics of ordering and material holding costs. Fewer components also increase production throughput by reducing rework and RMA costs. Simpler boards with fewer components can also compress manufacturing setup time.

Because standard tolerance components can be used (for example 5% and 10% voltage regulators), customers can use surplus inventory from other projects and minimize write-offs. They can also avoid the long lead-times associated with higher precision components.

Improved Quality and Reliability

With only two power rails required in Spartan-3A/3AN/3A DSP platforms, the need for additional voltage regulators and other expensive components is eliminated. The decreased PCB complexity, resulting from fewer components, lower layer count and improved signal integrity (Figure 6), plays a significant role in improving the quality and reliability of products.

Reduced device count also decreases the failures from misalignment and cold solder joint failures.
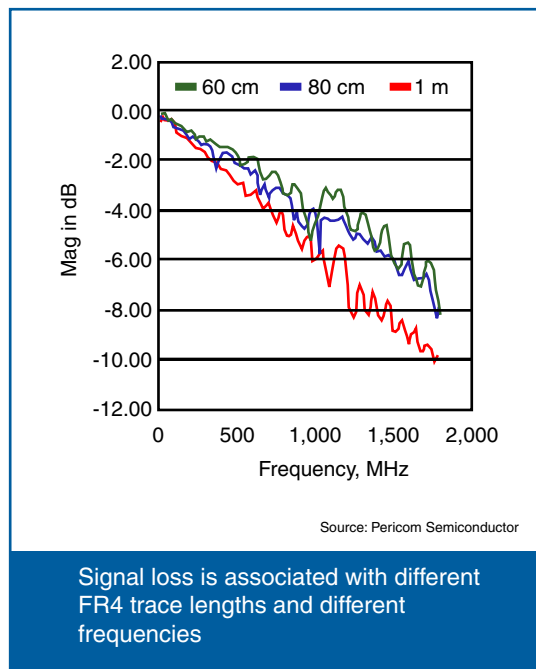
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Figure 6: **Spartan FPGA's Fewer Traces Improve Signal Integrity**

Lower Power, Lower Cost
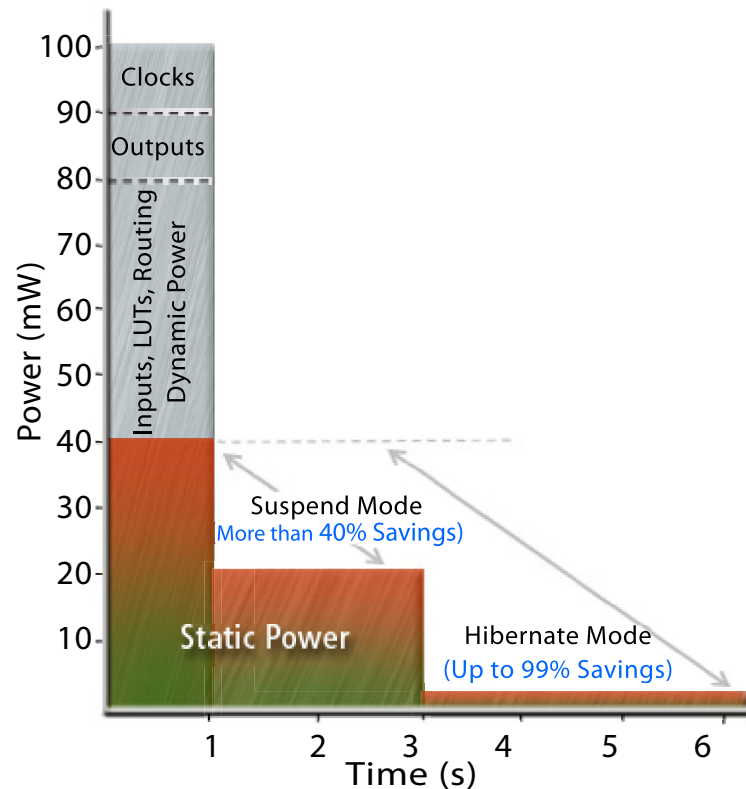
On-chip Power Management

The power-saving approach in Spartan-3 generation FPGAs is similar to the way you save power in your own home. A prudent saver will use energy-efficient light bulbs and switch off lights that are not being used. Likewise, in addition to power-efficient transistors, Spartan-3A/3AN/3A DSP platforms incorporate on-chip dual power management modes that switch off unused circuits when not in operation. In fact, Spartan FPGAs are the only high volume FPGAs in the industry that have built-in power management modes. Unlike competitive solutions that require external

components to save power, the dual power management modes in Spartan FPGAs are natively supported and have no complex design requirements.

Each mode can be easily invoked using a single FPGA pin, and the modes offer substantial power savings in real-world applications (Figure 7). The dual power-management modes are:

Suspend mode: Lowers static power by more than 40%. The internal state of the FPGA is saved for a quick wake-up, and the I/Os switch to a predetermined state.

Hibernate mode: Offers maximum power savings by lowering static power by up to 99%. The I/Os switch to 3-state, and it is safe to switch off all power in this mode.

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Figure 7: **Power Management Modes Significantly Reduce Power in Real-world Applications**

To take the power savings to the next level, Xilinx provides industry-leading power management tools for power evaluation and optimization. The ISE 10.1 software delivers automatic dynamic power reduction, while the XPower Analyzer helps designers with full environment voltage and worst-case evaluations. In fact, for its unique power-saving features, the Spartan-3A platform was awarded the 2008 Portable Design Editor's Choice Award for portable applications (Figure 8).

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Figure 8: **Portable Design Editor's Choice Award for Portable Applications**

The power savings have far-reaching implications on 'total cost'. Designers save with lower energy costs and smaller batteries, and there are no complex design requirements—resulting in fewer external components such as heat sinks and fans.

Security from Fraudulent Manufacturing

As counterfeit products flourish in the marketplace, companies not only suffer unrecoverable losses in revenues, their reputation and credibility can also be significantly tarnished. Using Device DNA, an electronic serial number that is factory-programmed into every Spartan-3A/3AN/3A DSP device, designers can implement a low cost and highly robust design-security solution.

The Device DNA security mechanism is similar to an ATM transaction (Figure 9). In an ATM transaction, the active value generated from the card number plus PIN number combination is compared to a number stored in a bank computer that authorizes or rejects the transaction. Similarly, the unique 57-bit Device DNA number is used with a customer-defined security algorithm to generate an active value. The active value is compared to a pre-stored check value to determine whether design functionality can proceed.

Device DNA security helps designers protect their business from common security threats such as reverse-engineering, cloning and overbuilding. It can be used for protecting both hardware and software IP and customers have complete flexibility in designing an authentication algorithm based on their unique application requirements.
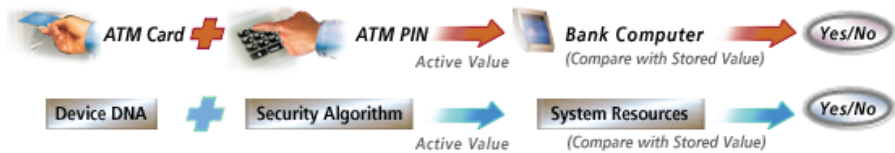
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Figure 9: **Easy as an ATM Transaction, Device DNA Offers Robust, Low-cost Security**

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Summary

In today's extremely competitive environment, high volume application designers must strive to cut costs at every stage of their business operation—component costs, engineering costs, assembly and manufacturing costs, costs to maintain high quality, system power consumption costs, and the cost to protect designs from fraudulent manufacturing—among others.

Spartan-3 generation FPGAs are designed from the ground-up to deliver the *lowest total cost* for high volume applications. The five domain-optimized platforms provide designers with the industry's largest selection of devices and packages, so designers can count on finding the most cost-optimal device for their unique application. The Spartan FPGA's on-chip features eliminate or reduce the number of external components, such as voltage regulators, buffers, drivers, and expensive filtering components required to create a solution using other FPGAs. Fewer components not only reduce BOM costs, they go a long way towards reducing the manufacturing costs and improving the quality of the products. The dual power management modes in Spartan FPGAs save considerable power in real-world applications and require fewer heat sinks and fans compared to competing solutions. Device DNA security is another key attribute that provides a flexible low-cost solution to protect customers from fraudulent manufacturing. In addition, the industry's most thriving ecosystem of IP, boards/kits, and software tools provides considerable support in helping designers get to market sooner. All these cost-saving factors translate to one key value for our customers—succeed in their business by saving up to 50% in total cost compared to competing solutions. The Spartan-3 generation FPGAs deliver the lowest total cost. *Period*.

For more information on Spartan-3 generation FPGAs, please visit:

www.xilinx.com/spartan/

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/08/08	1.0	Initial Xilinx release.

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