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Hot-Swapping Virtex-II, Virtex-II Pro, Virtex-4, and Virtex-5 Devices

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Summary

Hot-swapping or hot insertion describes a potentially dangerous method of inserting an un-powered board into a powered-on (hot) running system. There are several concerns: the insertion must not cause physical harm or permanent damage to the system or to the inserted board, and the insertion must not cause data corruption or any transient system upsets. This application note describes the physical aspects of hot-inserting a Virtex™-II, Virtex-II Pro, Virtex-4, or Virtex-5 based card into a system or system backplane, using sequenced connectors, where V_{CC} and GND mate well before any signal pins can mate. The dangers of using normal non-sequenced connectors are also described in **Hot Plug-In**. Not addressed in this application note are system issues, including detecting the presence or absence of a card, or how the card is accepted in the system.

Introduction

Plugging a board into a live ("hot") system can pose many problems, since the electrical connections might occur in an unpredictable sequence. By using specialized sequenced connectors, most problems are avoidable since the contact arrangement guarantees ground and V_{CC} mate before any signal pins mate. V_{CC} distribution on the plug-in board does, however, often include regulators with significant delay. This delay could exceed the insertion time, and thus defeat the purpose of the staggered connector pins.

The conventional CMOS output structure in the Virtex-II through Virtex-5 family architecture in Figure 1 incorporates two strong diodes on every pin, one to GND and one to V_{CC}. Conversely, the Virtex and Virtex-E families have an unconventional output structure with isolated p-channel pull-up transistors and a non-standard bipolar/SCR protection diode arrangement that discharges positive input spikes to ground, not to V_{CC}. Although the previous structure simplifies hot plug-in solutions, it also uses non-standard processing methods and is, therefore, not used in devices in the Virtex-II through Virtex-5 families. The I/O structures in these families support LVDS differential receivers and drivers, HSTL Class IV receivers and drivers, and the digitally controlled impedance (XCITE™) feature on all single-ended receivers and drivers.

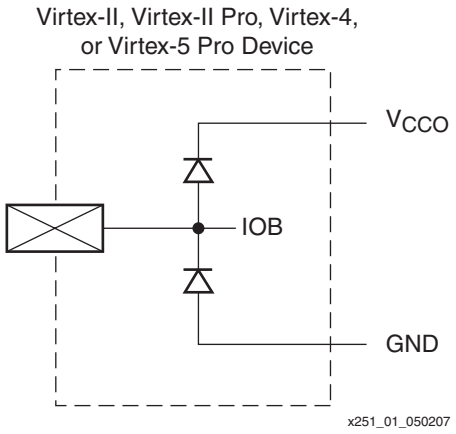

Figure 1: **A Cold Card Insertion**

In the best case, ground and V_{CC} pins mate first and the V_{CC} distribution on the board feeds all the positive supply pins before any signal pins mate.

When the onboard V_{CC} distribution is slow and signal pins mate before the supply voltage is completely powered, then any active High signal pin might drive current through the diode into the V_{CC} pin. This can cause signal loss on the driving side. One possible solution is to bypass the onboard V_{CC} distribution with a passive network, as shown in Figure 2. This guarantees power on the I/O of the FPGA before any signal pins can mate.

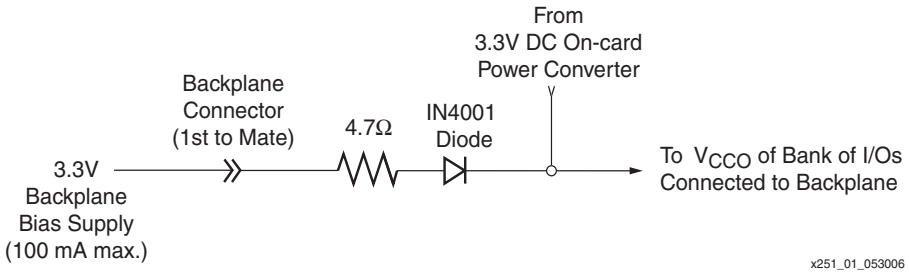

Figure 2: **Small Bias Supply Example**

When the signal pins mate with the backplane, the level of the signals shared between cards might be affected. The instantaneous charge transfer between the PCB trace capacitance, the package capacitance, and the device I/O capacitance must all be considered. If this total capacitance is, for example, 50 pF and the signal value is a "1", the insertion of a card can result in the signal glitching to the "0" state. A simulation should be performed to evaluate this effect. Protocol should be in place to prevent the propagation of errors due to glitches.

Damage to the backplane by sudden large currents can cause arcing or pitting in the contacts. To prevent large destructive currents, the onboard power converter must be soft started. This soft start requirement conflicts, however, with the need to be up and running before the signal pins mate.

Card Failure

There are many potential sources of card failure. Only the failure of the power supply is covered here.

When the onboard V_{CCO} power supply fails or is not present, the diodes in Virtex-II through Virtex-5 devices can become forward biased if the V_{CCO} of the I/O bank falls well below the voltages on the affected common signals. The currents involved are not large (50 mA worst case) unless the V_{CCO} is clamped solidly to ground (e.g., in the case of a short from a tantalum capacitor failure).

Providing enough time for the power supply to come up to voltage before the critical I/Os connect to the backplane appears impossible. A supply voltage must be present on the backplane for use by the critical I/O bank before the power supply can power up the card.

The solution to prevent the clamping action is to use some power supply redundancy or a small bias supply as shown in Figure 2. When combining the power source(s), simple diodes are the best choice. In Figure 2, the low current backplane bias quickly powers on the V_{CCO} of the card. This prevents the clamping of signals. The 1N4001 diode protects the bias supply from transients and isolates the local, on-card, 3.3V DC power supply. The 4.7Ω resistor limits the surge current to prevent arcing and pitting of contacts.

In Figure 3, a 3.3V DC source from the on-card supply could be passed through a low drop-out (LDO) regulator with the ability to supply 500 mA at 2.5V DC to a common backplane bus pin shared by all of the cards.

The reliability of an LDO is similar to a that of a diode, about five failures per billion hours (five FITs). Since the failure mode is surely an open, the reliability of the LDO is better than the typical 10 FITs of a backplane connector pin pair. For offset connector system details, refer to the backplane connector manufacturer.

If each card supplies 2.5V DC to this current-limited common rail, then the critical I/O bank on each card is powered from this pin through a 2.2Ω resistor to the bank-specific bypass capacitors. A card insertion does not affect the other cards using the common bus, and the inrush current is limited to avoid pin damage. The I_{CC} load on the banks powered this way needs to be small enough so that the 2.2Ω resistor does not drop more than 200 mV.

The critical I/O banks use the LVTTL 2.5V DC standard, rather than the 3.3V DC standard. The critical bank supply has more than enough capacity to provide power to any critical I/O bank card if the 3.3V DC converter fails. A “loss of on-card power supply detector” powered from the critical power pin must be used to force all I/Os into a 3-state condition. If a fault exists for the V_{CCINT}, V_{CCAUX}, or V_{CCO} on the card for other banks, then 3-stating the part will register a card alarm.

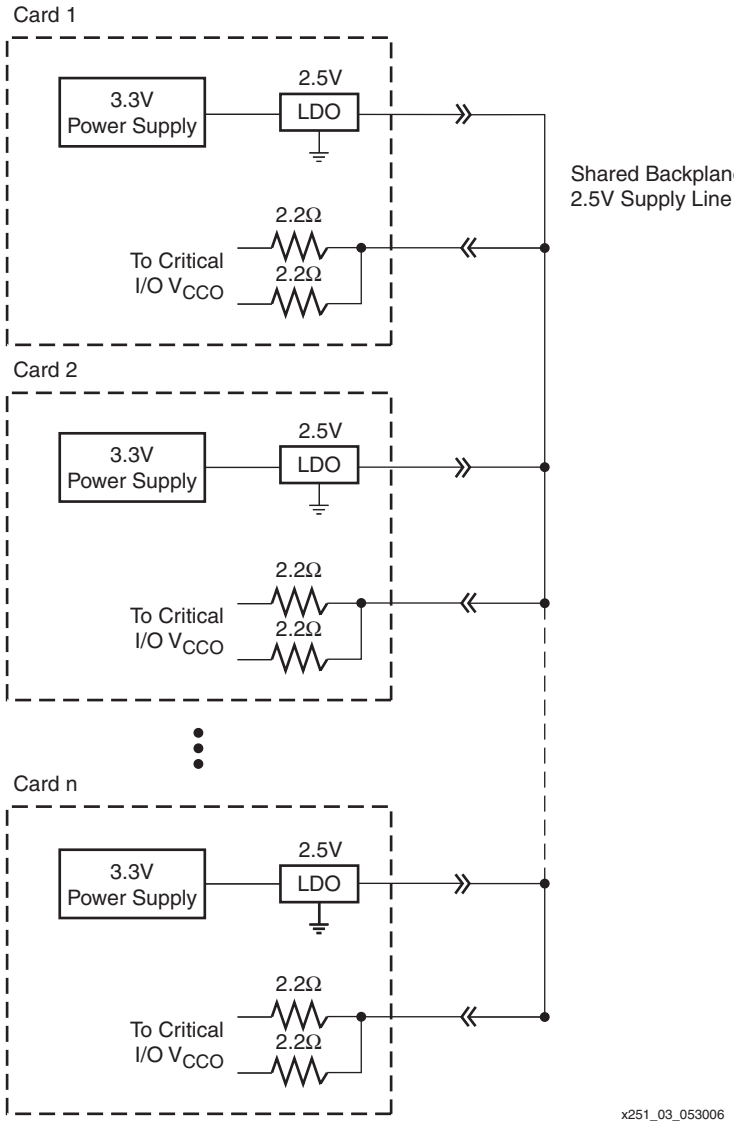

Figure 3: **Solution**

Hot Plug-In

Danger of Non-Sequenced Connectors

Plugging a board or device into a powered-up system is dangerous because the pins can make contact in an unpredictable sequence. There may be many milliseconds from making the first contact to the last one. What occurs in between is the problem.

In the best cases (as described on the previous pages), GND and V_{CC} mate first before any signal pins make contact. There are specialized connectors to enforce the correct mating sequence; GND and V_{CC} pins are longer, making them always mate first. These kinds of sockets are popular in telecom applications where hot plug-in is standard practice. With specialized connectors, there are no electrical hazards.

Without a sequenced connector, permanent electrical damage is possible. Consider the case where GND and a few signal pins make contact first, and one of these signals is driven High by a 3.3 V CMOS driver with a 20Ω output impedance. Until the V_{CC} pins make contact, this High signal will forward-bias the pin-to-V_{CC} diode and try to drive the not-yet-connected V_{CC} distribution network to a marginally High level.

The logic signal acts as a surrogate V_{CC} supply, but none of the signal traces and circuit elements are strong enough for this job. The current value depends on the number and the nature of the devices fed from the unpowered V_{CC} net. SRAM-based FPGAs can actually start the configuration process in master mode, still only powered by one or a few logic signals. As a result, the configuration will usually be aborted before it is finished. These uncontrolled activities and uncontrolled electrical overstresses are not desirable.

A similar problem occurs when V_{CC} and a few signals make contact before GND is connected. A Low signal output on the powered-up board acts as the surrogate GND for the plug-in device, with current coming in through the pin-to-GND diode from the unpowered device.

Virtex-II through Virtex-5 devices have two strong diodes on each input pin, one connected to GND, and one connected to the V_{CC}, to send excessive input charge into the supply rails. The XC4000XL, Virtex, Virtex-E, and Spartan™ devices do not have a diode to V_{CC}, but rather use a positive discharge structure to GND. This eliminates some of the hot-plug-in problems.

The normal ramping-up of V_{CC} in a digital system is complicated enough, with different devices coming “alive” at different voltage levels. A haphazard plug-in procedure is much worse. Hot plug-in should be avoided unless the equipment is specially designed.

Conclusion

With proper precautions and the correct connectors, systems can be designed that allow the hot-swapping of cards on a backplane.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/12/01	1.0	Initial Xilinx release.
08/15/01	1.1	Revised introduction.
05/30/06	1.2	Updated with Virtex-II Pro information.
05/02/07	1.3	Updated to add reference to Virtex-4 and Virtex-5 families.
05/14/07	1.3.1	Typographical error.