Understanding True CMOS Outputs

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Summary

This document provides a description of the CMOS output structures of the CoolRunner CPLDs and details some advantages of using true CMOS (rail-to-rail capable) output drivers.

Introduction

Today's integrated digital logic devices trace their roots back to RTL (Resistor-Transistor Logic) components which were pioneered in the 1960s. RTL eventually evolved into DTL (Diode-Transistor Logic) which in turn was followed by TTL. With TTL (Transistor-Transistor Logic) and then ECL (Emitter Coupled Logic), designers found components that were orders of magnitude better than the first RTL devices, providing acceptable noise immunity, the ability to fanout to more than one device, and usable (25 MHz) propagation speeds. At the time, this logic provided engineers with a technology that enabled them to increase the density of their systems by providing pre-packaged functions for "drop in" design use. However, these early devices consumed a significant amount of power (typically 30 to 40 mW *per gate* at 1 MHz) which catalyzed a demand for lower powered devices.

In response to the demand for lower power, RCA developed the first MOSFET based, mass production logic devices in the early 1970s. This family (remembered as the 4000 series family) provided devices that accommodated a large range of supply voltage and had zero quiescent (excluding leakage) currents. The outputs would swing from rail-to-rail and the inputs were high impedance, so input current was minimal. Drawbacks to this early CMOS offering included susceptibility to static induced latchup, poor output drive (as little as 1 mA even with the "buffered" version), and a high initial price tag which was typically $20 for a device with four gates.

Both bipolar and CMOS technologies have advanced significantly along their respective evolutionary paths, and have even merged in a family called BiCMOS which combines high input impedance, low quiescent power, and strong output drive characteristics. However, BiCMOS devices consume more power than pure CMOS ICs, and require approximately 30% more die space to implement the same function.

Manufacturers of semiconductors are continually seeking opportunities to decrease cost from their processes and products, which has resulted in widespread use of inexpensive plastic packages. These plastic packages have reduced thermal capabilities; the low power dissipation of the technology is one of the reasons why CMOS dominates (typically 90%) the VLSI market.

Programmable logic device manufacturers have benefitted from the CMOS technology, and are aggressively pursuing smaller pitch processes to gain advantages in speed, power, and cost. Various design techniques also exist to decrease die size, and thereby decreasing cost, at both the architecture and implementation level. One method of decreasing die size is to implement the output buffer in an NMOS fashion. While saving space, this method diverges from the complementary output structure resulting in a loss of some benefits. Since most programmable logic devices utilize a form of I/O structure where a pin may operate as an input or an output, the impact of modifying an "output" buffer also has "input" ramifications. A true CMOS (complementary) buffer provides desirable characteristics such as rail-to-rail output swings and overvoltage protected inputs. The benefits of true CMOS outputs will be discussed in this application note.

CMOS Outputs

CMOS is an acronym for **C**omplementary **M**etal **O**xide **S**emiconductor which indicates that the device has been constructed of both p-channel and n-channel transistors. The output buffers of a CMOS device may be CMOS type or NMOS type. If they are CMOS type, the driver structure is comprised of complementary elements; if they are NMOS type, the driver is typically created using two n-channel output drivers. A simplified example of CMOS and NMOS output structures is shown in Figure 1.

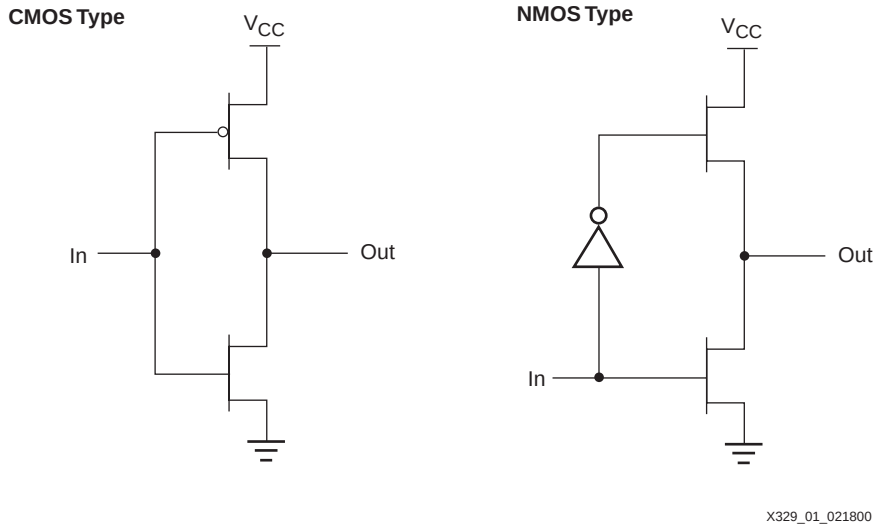

Figure 1: **CMOS vs. NMOS Output Buffers**

The benefit of using an n-channel pull-up transistor is that die space is conserved. A p-channel transistor must be approximately three times the size of an n-channel transistor in order to have similar output drive capabilities. Because of this, CMOS output buffers are twice the size of comparable NMOS buffers.

The advantage of using a CMOS buffer is that the output signal will transition from rail-to-rail (less the I*R drop of the transistor), where the NMOS output will transition from GND to one threshold below V_{CC} (approximately V_{CC} less 1V). See Figure 2 and Figure 3 for illustrations of typical CMOS and NMOS output curves.

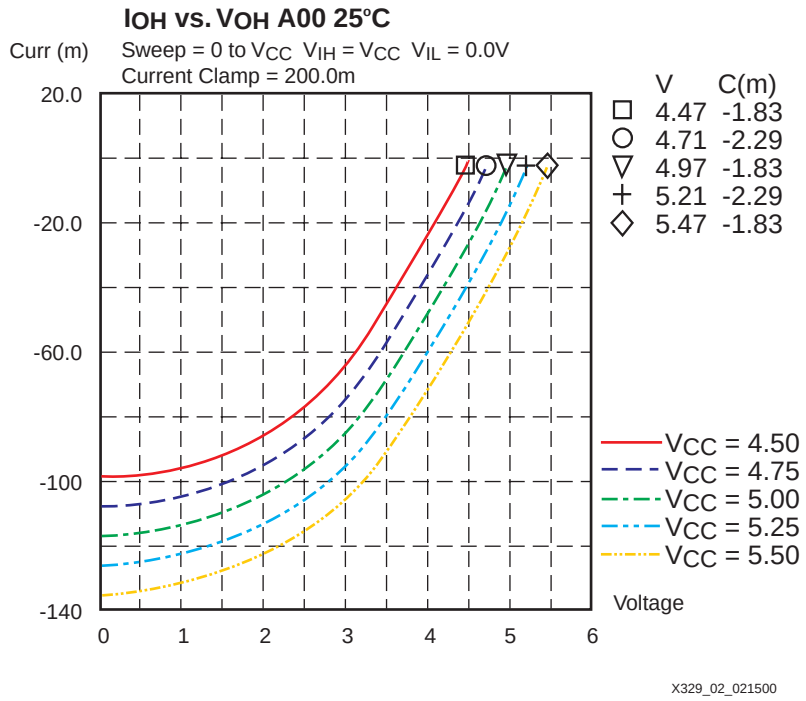

Figure 2: **CMOS Output Curves**

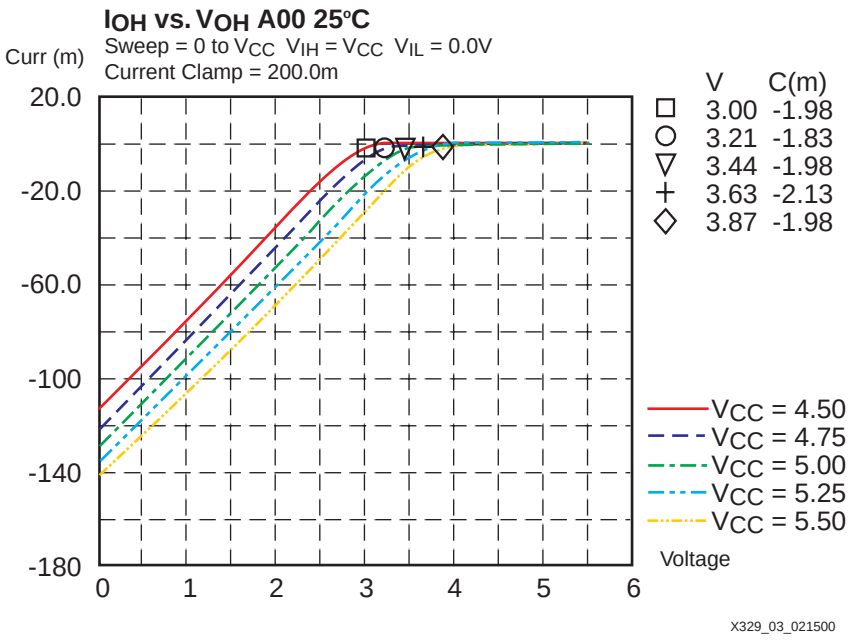

Figure 3: **NMOS Output Curves**

Note that these curves reflect V_{OH} data for 5V devices only. Because of the voltage threshold drop below V_{CC}, the option of using NMOS outputs exists only for 5V parts.

Benefits of CMOS Drive

The importance of using true CMOS outputs becomes readily apparent when system design is primarily comprised of CMOS devices driving other CMOS devices, and low power system operation is required. Examine the CMOS example in Figure 1. Input buffers are also constructed in this sort of fashion; the input signal to the buffer is applied to both transistor gates simultaneously. A review of the basics of FET theory reveals that these devices have a portion of their R_{DS} (Resistance, drain to source) vs. V_{GS} (voltage, gate to source) in a linear region, which means that for some portion of the V_{GS} range the device is not fully "on", nor fully "off". Note that this implies an input voltage region for the two transistors in which both are conducting to some degree. If this is the case, then current is flowing from V_{CC} to GND through this buffer structure, which indicates that the buffer is performing in the linear region and power is needlessly being consumed by this Class A current operation.

To avoid this Class A current mode, the board designer should ensure that signals driving CMOS inputs are as close to the voltage rails as possible, and that signal transitions (from logic low to logic high and vice-versa) are completed swiftly. **For designs that require absolute low power operation, it is imperative that CMOS inputs are driven by full CMOS (rail-to-rail) outputs**.

Additional benefits of CMOS outputs include an increased system noise immunity, and the ability to easily interface to other logic types. Using true CMOS output devices provides system designers with logic voltage levels as "far" as possibly apart ($V_{OH} – V_{OL}$ is maximized), which provides an additional margin of protection against signal noise causing false logic conditions. True CMOS outputs also interface (drive) easily to other logic families, since most V_{IH} and V_{IL} conditions are readily met.

Over Voltage Tolerance

A warning does exist for users of true CMOS outputs. Some devices that utilize true CMOS output structures do not allow for the external application of a pin potential on these pins that exceeds V_{CC} by more than approximately 0.5V. This is common in cases of programmable logic that have pins which may be configured as either inputs or outputs, and the outputs are fully PCI compliant. This issue stems from the 3.3V PCI requirement which insists upon some sort of protection diode terminating the input (anode of diode) to V_{CC} (cathode of diode). Devices that do not support this characteristic may be PCI compatible, but they are not PCI compliant. When this diode is in place and the external pin potential exceeds the V_{CC} voltage, the diode becomes forward biased and will conduct. The input impedance of the pin will be seen by the outside driving potential as being very low, and large input currents can result.

This input protection diode can also exist as a "parasitic" effect from true CMOS outputs. Examine Figure 4 and reflect on the characteristics of the p-channel pull up transistor when the drain voltage (output) exceeds the source voltage (V_{CC}).

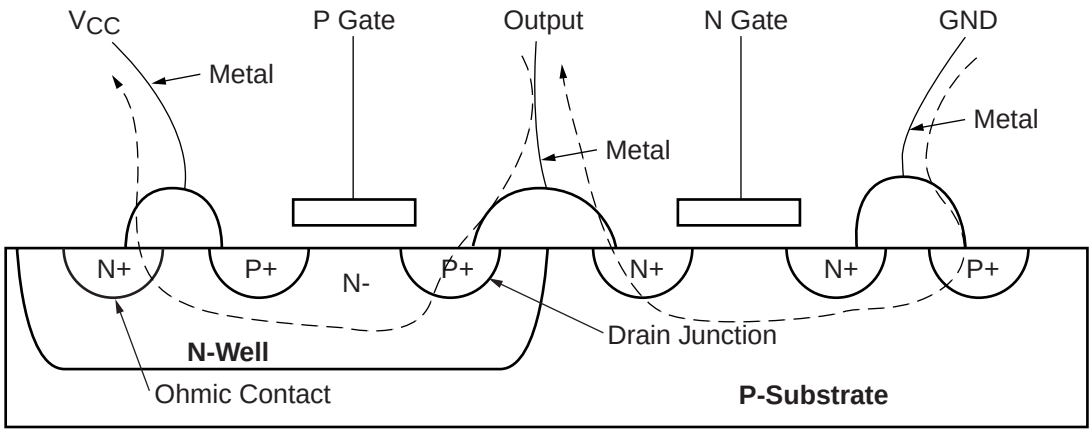

Figure 4: **CMOS Buffer Diagram**

The p-channel transistor has a PN junction (Drain Junction) that becomes forward biased when the output potential exceeds the V_{CC} potential. This causes current to flow from the output through the drain junction into the N well and then through the Ohmic contact made by the N+/N- junction and into V_{CC}. There exists another PN junction that creates a path from GND to the output; this second path becomes forward biased when the output potential falls below GND. Refer to Figure 5 for another example of this property.

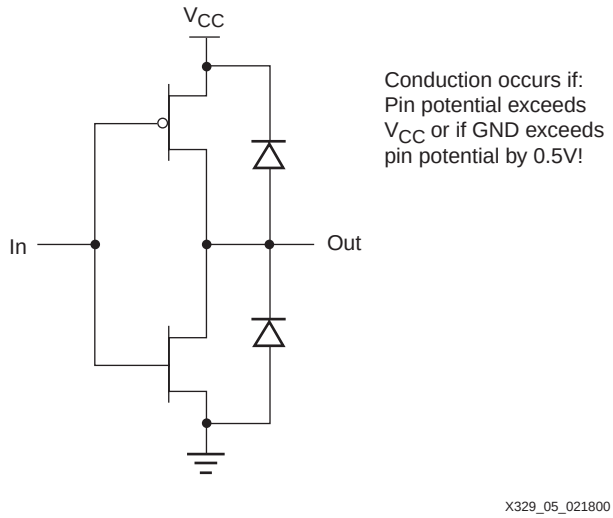

Figure 5: **"Parasitic" Diodes**

While these PN junctions provide a benefit to users who require PCI compatibility, and this mechanism also protects against static damage, it is these "parasitic" diodes that instigate latchup. This characteristic is also undesirable to those who require a tolerance of 5V on inputs of 3.3V devices. A solution does exist to allow for increasing input tolerance; the technique for implementing overvoltage (referenced to V_{CC}) tolerant inputs involves the addition of approximately five to ten transistors to switch N+ well to V_{CC} or the I/O pin. If an overvoltage condition exists on the pin, an internal circuit detects this condition and effectively detaches the N+ well from V_{CC} and allows for the N+ well to be powered directly from the I/O pin. This technique is used extensively for inputs on devices that are powered from 3.3V or less and who allow for over-voltage input. All reduced voltage (3.3V and below) powered devices must have full CMOS outputs because the output signal cannot afford the large threshold drop below V_{CC}.

Hot Plugging Issues

It is important for designers to understand the I/O operating characteristics of all devices in a system. The application of voltages to Input pins or I/O pins that exceed V_{CC} may cause not only damage, but also unexpected behavior in the device. In some instances these pins function as multi-purpose pins (while in manufacturing mode) and are used by manufacturers for functions such as programming or special test. Over-voltages applied to these pins may cause the device to enter into special operating modes which may cause erratic results. For this reason it is critical that absolute maximum ratings be observed and designs be implemented with caution regarding systems that may impose pin voltages prior to V_{CC} initialization.

Categorizing CoolRunner Outputs

CoolRunner CPLDs have true CMOS outputs with only a few exceptions. The data sheets that describe the characteristics of these devices do not reflect the actual output voltage/current curves; in many instances the data sheets are extremely conservative. An example of this can be found in the XCR5128-7 device. This device utilizes true CMOS outputs but is characterized by the data sheet as having a "worst case" V_{OH} of 2.4V at –12 mA. While this *worst case* specification is certainly accurate, this device *typically* has an output V_{OH} of greater than 4.5V

for that magnitude of output current. Table 1 illustrates the type of output structure used in each of the CoolRunner parts and indicates whether or not a 3V device has 5V tolerant inputs.

Table 1: **Chart of Device Output Types**

Device	5V Tolerant 3V Devices	CMOS or NMOS Output
XCRv032	N	CMOS
XCRv064	N	CMOS
XCRv128	N	CMOS
XCRv032C	N	CMOS
XCR5064C	N/A	NMOS
XCR5128C	N/A	NMOS
XCR3032A/D	Y	CMOS
XCR3064A/D	Y	CMOS
XCR3128A/D	Y	CMOS
XCR3320	Y	CMOS
XCR3960	N	CMOS
XCR22LV10	Y	CMOS

Notes:

For the devices above, a "v" in the part number indicates that this may be a 5 or 3 depending on whether the device is a 5V or 3V device. N/A indicates that the device does not exist in a 3V version.

Conclusion

Benefits of using true CMOS outputs include:

- Lower power operation when interfacing to other CMOS devices
- Increased system noise immunity
- Ability to easily interface to other logic families
- "Built-in" over and under voltage static protection
- "Built-in" termination for PCI compliance

Understanding the output structure of logic elements will facilitate the implementation of robust system design. Knowledge of the characteristics of output and input structures provides designers with key insight to avoid problems, but more importantly, recognizing critical device benefits (such as true CMOS outputs) can provide engineers with valuable knowledge when evaluating and selecting components for future designs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/18/00	1.0	Initial Xilinx release.
10/09/00	1.1	Added Application Note reference to header.