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In-System Programming of XPLA3 Devices

Summary

This document provides a brief description of how to perform ISP operations with XPLA3 CPLDs.

Introduction

With the possible exceptions of speed, deterministic timing, and low power, few things are as important to programmable logic designers as reconfigurability and available I/O. In-System Programming (ISP) has provided a flexible means of reconfigurability, but this feature mandates the availability of at least four pins to accommodate ISP and Boundary Scan operations. Some ISP devices provide dual configurations of the JTAG pins, where the ISP pins may be configured as general purpose I/O if not required for ISP or Boundary Scan. In most cases, however, the designation of JTAG pins as I/O precludes this device from future ISP operations unless the part is bulk erased using a VPP mode of erasure. Historically, the use of ISP techniques exacerbated the issue of insufficient device I/O, especially for smaller devices with low I/O counts.

Xilinx XPLA3 devices provide designers with a Port Enable pin, which both facilitates ISP and provides a maximum number of I/O pins for any given macrocell count XPLA3 CPLD. This pin serves as a control pin which may redirect JTAG pins that were previously configured as I/O. The use of this feature requires very little external circuitry to provide for the dual capability of JTAG pins as I/O.

XPLA3 ISP Pins

As in many other popular ISP devices, the XPLA3 family uses only four signal pins and a ground reference to implement ISP and Boundary Scan commands. The four required pins for XPLA3 JTAG operation are TDI, TMS, TCK, and TDO. These pins provide control of the standard 1149.1 TAP controller. The TRST signal is an optional signal and has been omitted from the ISP interface for XPLA3 devices. The IEEE 1149.1 specification requires either the TRST signal pin or internal device reset circuitry (as is the case with XPLA3 devices) to ensure that the JTAG controller powers up in a reset state. Additional information about JTAG pins and their functions can be obtained by referencing the IEEE 1149.1 specification. The Port Enable pin is an additional pin included with XPLA3 devices to allow for simple implementation of dual-purpose ISP pins.

Port Enable Pin

The Port Enable pin is a CMOS input with a very simple mode of operation. This pin should be held low during power up and during normal operation. If the device has been programmed such that the JTAG port pins are used as I/O, a High logic level signal placed on the Port Enable pin will revert those pins back to their normal JTAG function. The maximum time delay from Port Enable High to JTAG pins with ISP functionality is 10 µs; conversely, the maximum delay from Port Enable Low to JTAG pins functioning as programmed I/O is also 10 µs.

Implementation

If it is desired to use the JTAG pins in a dual-purpose mode, consideration should be given to the function of each of these I/O pins and the logic to which they will be interfacing. When possible, use the dual-purpose pins for control or status signals, as the external circuitry required to implement this function will add some delay to the signal path. Figure 1 shows an

example of how to safely interface I/O signals with the JTAG pins. TMS and TCK have been omitted for clarity; as input signals, these two may be handled similarly to the example of TDI.

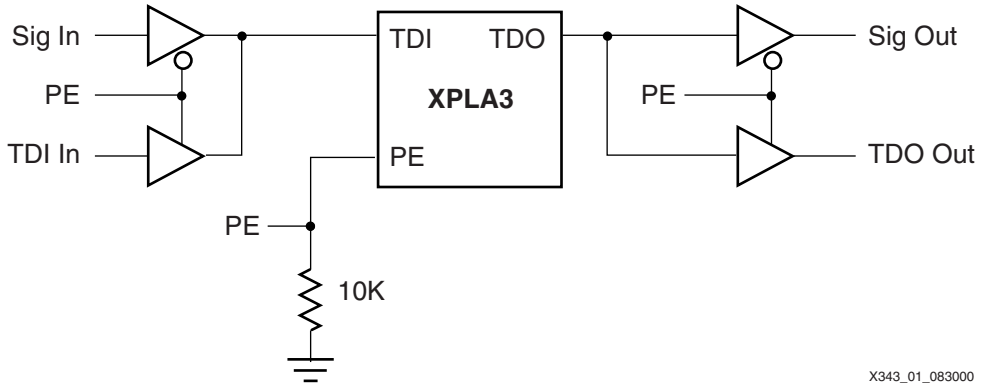

Figure 1: **Implementing I/O on JTAG Pins**

Conclusion

The addition of the Port Enable pin to the XPLA3 devices yields a unique flexibility that allows JTAG pins to serve as dual-purpose pins; this provides the maximum amount of I/O without sacrificing the benefits of In-System Programming.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/30/00	1.0	Initial Xilinx release.