



XAPP381 (v1.0) September 1, 2002

CoolRunner-II Demo Board

Summary

This document describes the demo board that uses the CoolRunner™-II 64-macrocell CPLD.

Introduction

The new CoolRunner-II CPLD family utilizes a true CMOS based architecture that provides ultra low power consumption combined with high speed operation. This new class of CPLDs provides an all-digital core, eliminating power-hungry sense amplifiers in the speed path.

Additional silicon features are provided by the CoolRunner-II CPLD family that promote integration, such as clock division and dual edge clocking, DataGATE, Schmitt trigger inputs, I/O banking and multiple I/O standards. All features are fully supported in the 128-macrocell and larger parts; for a complete overview of the CoolRunner-II CPLD family, refer to the [CoolRunner-II CPLD Family Datasheet](#).

This demo board illustrates the low power operation of the CPLD and showcases the use of the Schmitt trigger inputs. A simple R/C oscillator functions as an onboard clock, optimally requiring the use of a Schmitt trigger input. Additional demos of the board may include a visual demonstration of dual-edge clocking, low power measurements, and miscellaneous I/O operations.

Board Description

Board Overview

As shown below in [Figure 1](#), the CoolRunner-II demo board was designed to provide a compact operational demonstration of the newest member of the Xilinx CPLD family. As a reference, the board dimensions are approximately 2.0 inches by 2.5 inches. A minimal number of components comprise the demo board, whose main elements are a CoolRunner-II CPLD, a boost power regulator, display unit(s), a small amount of user I/O, and two clock sources. An additional PCB footprint is included for a 50 Ohm high speed clock interface. A single AAA battery is the primary source of board power, and is mounted on the reverse side.

Important Note: Reverse polarity protection is not provided for in this design. Use caution to maintain correct battery polarity when inserting a battery into the battery clips.

The reverse side of the board has mounting holes which will accommodate a standard, two-digit by seven-segment LCD display (such as the Varitronix VI-201 series). This allows the end user to place a second display on the board, facilitating additional experimentation. Note that both the core voltage and the I/O voltage are supplied by the 1.9V DC/DC converter. As such, the drive available for the second display is only 1.9V. If the secondary display requires a higher drive voltage, the contrast of the display may be somewhat diminished.

Power Jumpers JP1/JP2

Two small headers on the bottom right side of the demo board have been provided to control the power for the demo board. JP1 is the battery connection/shutoff jumper, and JP2 is the power selection jumper. Refer to [Table 1](#) for a description of jumper settings.

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Table 1: Power Jumper Settings

| Jumper : Pin Position | Function |
|-----------------------|--|
| JP1 : 1-2 | Battery connected to DC/DC converter |
| JP1 : 2-3 | Battery "floating", power off |
| JP2 : 1-2 | V _{CC} = DC/DC converter output |
| JP2 : 2-3 | V _{CC} = auxiliary power input |

Auxiliary Power

Two small pads are placed on the right side of the display for an auxiliary power and ground source. These pads may be used as a "Grapefruit Demo." Jumper JP2 allows the user to choose between power sources. When JP2 is in the 1-2 position, the board is powered from the onboard DC/DC converter. When in the 2-3 position, the board is powered from the auxiliary pads. JP1 functions as a battery disconnect. Bulk decoupling of the board is provided for both power sources. **Do not exceed 2.0VDC when using auxiliary power pads.**

For more information on powering the board using the "Grapefruit Demo" refer to the section titled **Demonstration 3 : Low Power Operation**, page 9 in this document.



Figure 1: CoolRunner-II Demo Board

CoolRunner-II CPLD

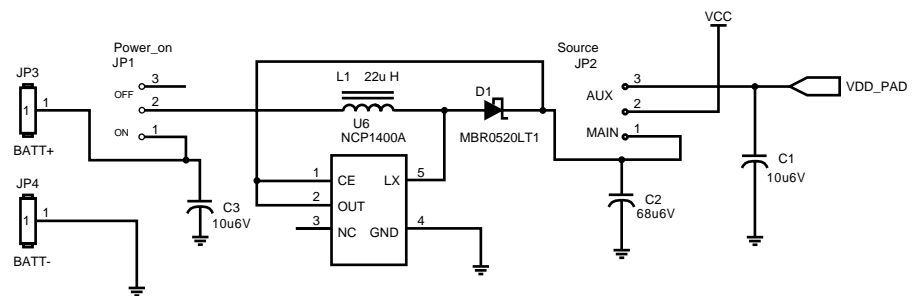
The CoolRunner-II demo board utilizes the 64-macrocell device as the LCD driver. Other interfaces to the CPLD include a standard JTAG header (JP5), two push button (momentary close) micro switches (SW1, SW2), eight general purpose I/O (JP6), an R/C clock, a precision 32.768 kHz clock, and a 50 Ohm high speed clock input (J1).

The primary firmware demonstration that is provided for the demo board utilizes both of the onboard clocks. In one mode, the design uses the Pletronics oscillator as the clock source. In the second mode, the R/C oscillator is employed to drive the display, and the Xilinx logo is scrolled at a slower rate. The user may toggle the mode of operation by pressing the SW2 button. The SW1 button may be used to reset the internal state machine at any time, which will also blank the display for the duration of the reset, and reassign the Pletronics oscillator as the clock source. The Pletronics oscillator provides an exceptional clock source for low power

electronics. This oscillator consumes approximately 5 μA , while providing 100 ns edges into a 15 pF load.

Boost Regulator

Figure 2 displays the schematic for the DC/DC converter. The controller for the boost regulator is the ON Semiconductor NCP1400A. This highly integrated controller provides switching control and regulation while requiring only a minimal number of external components. Other components comprising the high-efficiency converter include a low forward voltage Schottky diode (also from On Semiconductor), and a DO-1608C surface-mount inductor from Coilcraft. The Coilcraft inductor was chosen for its low physical volume characteristics. As the power required by the demo board is very low, saturation risk is minimal, and a higher value inductor was suggested by Coilcraft to improve efficiency. This particular regulator/inductor combination provides a high-efficiency, low-noise DC/DC solution. Start-up voltage in this application is typically 0.9VDC, and the converter will run down to 0.3V while providing a regulated 1.9V output.



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Figure 2: DC/DC Converter

LCD Displays

The primary display on the demo board is a custom display fabricated specifically for operation at 1.8V drive levels. Each operable visual item in the display is a separate LCD segment which is driven directly by the CPLD.

To properly drive an LCD such as this one, the CPLD provides a reference signal to the backplane of the display. This signal is approximately 100 Hz at a 50% duty cycle. To enable any segment on the display, the segment is driven by a 100 Hz, 50% duty cycle signal that is 180 degrees out of phase with the backplane. To disable or "turn off" any graphic on the display, that segment is driven at the same frequency, phase, and duty cycle as the backplane.

On the reverse (solder side) of the demo board, there are additional pads for interfacing to a standard seven-segment, two-digit display. Note that if a secondary 3.3V display is used, the contrast may not be as pronounced due to the 1.8V output drive configuration of the CoolRunner-II CPLD. Refer to **LCD Drive**, page 5 for additional details.

Board Function

The demo board's primary function is operating the custom LCD display. The Xilinx logo scrolls from left to right, with the CoolRunner-II logo, High Speed, Low Power, and lightning segments displaying in a sequential fashion.

The example code provided for use with the demo board also has a 1 Hz output signal which drives pin 1 of JP6, and two input and output pins on this same I/O header to display the CoolRunner-II Schmitt trigger function. Refer to the section titled **Demonstration 1: Schmitt Trigger** for more information.

Switch SW2 on the demo board toggles the system clock between the Pletronics oscillator and a simple R/C oscillator. When the R/C oscillator is chosen, an additional delay stage in the

source code slows the progression of the display, as well. The default clock source upon power-up is the Pletronics oscillator.

Switch SW1 on the demo board provides a reset for the CPLD. Pressing reset also returns the clock selection to the default power up condition which uses the Pletronics oscillator.

CPLD Pinout

This demo board positions the 64-macrocell CPLD in the center of the PCB. In addition to the pins used to drive the LCD display, other pins are used as inputs from the clock and as I/O connections to the test header JP6. Refer to the schematic or to [Table 2](#) for definitions of the various I/O assignments.

Table 2: CPLD Terminations

| Signal Name | Function | VQ100 Pin |
|-------------|-------------------|-----------|
| N-SEG | LCD2 Drive | 49 |
| M-SEG | LCD2 Drive | 50 |
| BP | LCD1/LCD2 Drive | 64 |
| LOGO | LCD1/LCD2 Drive | 61 |
| CR | LCD1/LCD2 Drive | 72 |
| HS | LCD1/LCD2 Drive | 67 |
| LIGHT | LCD1/LCD2 Drive | 70 |
| LOPO | LCD1/LCD2 Drive | 74 |
| TWO | LCD1/LCD2 Drive | 68 |
| X-2 | LCD1/LCD2 Drive | 60 |
| N | LCD1/LCD2 Drive | 58 |
| I-2 | LCD1/LCD2 Drive | 56 |
| L | LCD1/LCD2 Drive | 55 |
| I-1 | LCD1/LCD2 Drive | 53 |
| X-1 | LCD1/LCD2 Drive | 52 |
| SW1 | Push Button Input | 97 |
| SW2 | Push Button Input | 99 |
| TEST1 | JP6:8 User I/O | 10 |
| TEST2 | JP6:7 User I/O | 11 |
| TEST3 | JP6:6 User I/O | 12 |
| TEST4 | JP6:5 User I/O | 13 |
| TEST5 | JP6:4 User I/O | 14 |
| TEST6 | JP6:3 User I/O | 15 |
| TEST7 | JP6:2 User I/O | 16 |
| TEST8 | JP6:1 User I/O | 17 |
| 32k_OSC | GCLK1 | 23 |
| E/D | 32k_OSC Enable | 24 |
| RC_IN | GCLK0 | 22 |

Table 2: CPLD Terminations (Continued)

| Signal Name | Function | VQ100 Pin |
|-------------|---------------------|-----------|
| RC1 | R/C Clock Drive | 18 |
| RC2 | R/C Clock Equalizer | 19 |
| TDO | JTAG Out JP5:O | 83 |
| TCK | JTAG Clock JP5:C | 48 |
| TMS | JTAG Mode JP5:M | 47 |
| TDI | JTAG In JP5:I | 45 |

In addition to the terminations listed in Table 2, several of the remaining I/Os on the CPLD are tied together on the PCB. This provides a demonstration platform to highlight the features of DataGATE, available in 128-macrocell (and larger) CoolRunner-II CPLDs. Refer to the schematic of the demo board for a detailed view of which CPLD pins are connected together by the PCB.

JTAG Connections

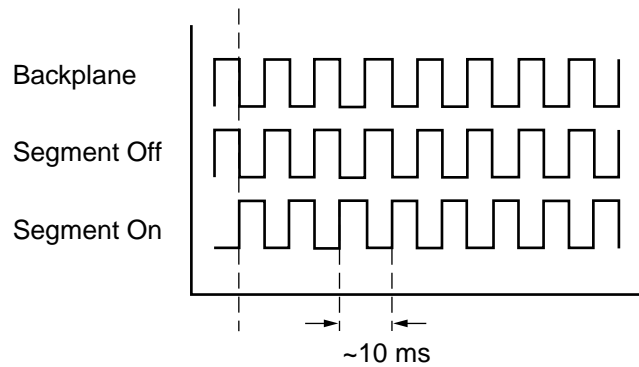
A Xilinx Parallel Cable IV JTAG cable is used to program the CoolRunner-II demo board. In many instances the Parallel Cable III (PCIII) will work correctly, but proper operation of the PCIII cable with lower voltage devices (less than 2.5V) is not guaranteed. Use version III of the cable only if a version IV cable is not available. The demo board includes a V_{REF} connection at the JP5 header to provide power/reference to external cables. Refer to Table 3 for JTAG connections to the demoboard.

Table 3: JP5 Terminations

| Pin Name | JP5 Pin Designator |
|----------|--------------------|
| VDD | V |
| TDO | O |
| TCK | C |
| TMS | M |
| TDI | I |
| GND | G |

LCD Drive

The drive requirements for the custom LCD on the CoolRunner-II Demo Board are typical of similar simple LCD devices. A back plane for the display is driven directly by the CPLD with a 50% duty cycle square wave, at roughly 100 Hz. Each segment of the display is bonded out to a pin on the LCD, which is then driven directly by a dedicated pin from the CPLD. In order to turn on a segment, the corresponding pin is driven at a similar frequency, duty cycle, and amplitude as the backplane, but the driving signal is 180 degrees out of phase with the backplane. In order to turn off a segment, the segment is driven in phase with the backplane, at the same duty cycle and amplitude. Refer to Figure 3 for a graphical representation of proper LCD drive.



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Figure 3: LCD Drive Characteristics

CoolRunner-II Demo Board Feature Examples

Preparation

In order to demonstrate some of the capabilities of the CoolRunner-II CPLD using the demo board, first process the source file demo_bd_cr2.vhd. This sample design, available from the [VHDL Code Download section, page 11](#), provides VHDL source, a constraint file, and a simulation file. This design should be processed with either WebPACK™ 4.2i or Foundation™ ISE 4.2i service pack 2 (or later) in order to generate the downloadable JEDEC file.

Demonstration 1: Schmitt Trigger

To display the capabilities of the Schmitt trigger inputs, a 1.5k Ohm resistor, a 100 μF capacitor, and an oscilloscope are required.

As mentioned above, the source code contains an internal divider that outputs a 1 Hz, 50% duty cycle signal to pin 1 of JP6. JP6 has an additional four pins that are used to demonstrate the Schmitt trigger capabilities. Refer to [Table 4](#) for a description of JP6 pin function.

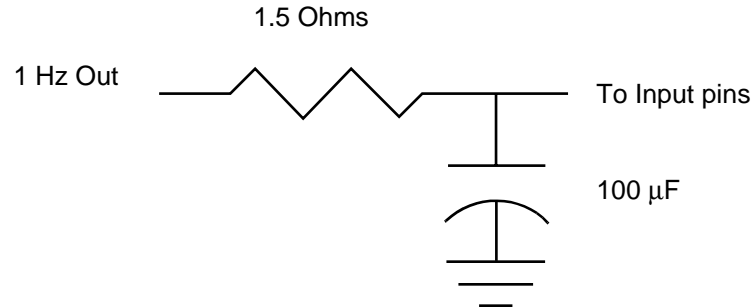
Table 4: JP6 Schmitt Trigger Demonstration Pinout

| JP6 Pin Number | Pin Function |
|----------------|-----------------------------|
| 1 | 1 Hz signal output |
| 2 | Non-Schmitt input |
| 3 | Buffered non-Schmitt output |
| 4 | Schmitt input |
| 5 | Buffered Schmitt output |

In [Table 4](#), the non-Schmitt input is a standard input pin that does not have the Schmitt trigger enabled. The buffered non-Schmitt output is an output that buffers this non-Schmitt input. In a similar fashion, the buffered Schmitt output pin directly outputs a signal that is input on a pin with the Schmitt trigger feature enabled.

In order to demonstrate the Schmitt trigger capability, a slow rising and falling edge signal must be provided to the inputs. This is done by taking the output from the 1 Hz pin of JP6 and

passing it through a low pass filter created using the 1.5k Ohm resistor and the 100 μ F capacitor. Refer to [Figure 4](#) for a description of the circuit.



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Figure 4: Low Pass Filter for Schmitt Trigger Demo

When attaching the output of the low-pass filter to the input pins, connect only one input pin to the filter at a time. Since the edges of the signal are extremely slow, this circuit may be constructed using jumper wires.

Once the filter is connected to the non-Schmitt input (JP6-2), use a scope to examine the signal output on the non-Schmitt output (JP6-3). It should resemble the traces below in [Figure 5](#). The top trace is the output of the low pass filter, viewed at the non-Schmitt input. The bottom trace is the output of the CPLD, as seen at pin 3 of JP6. Notice that because of the slow edge transitions, the input buffer starts to oscillate at the threshold and is unstable for a significant amount of time. Because of the high-driving impedance at the input pin (the 1.5k resistor), this noise can even be observed at the input pin. If a lower impedance-driving resistor was used, this noise on the input pin would be somewhat reduced, but still present.

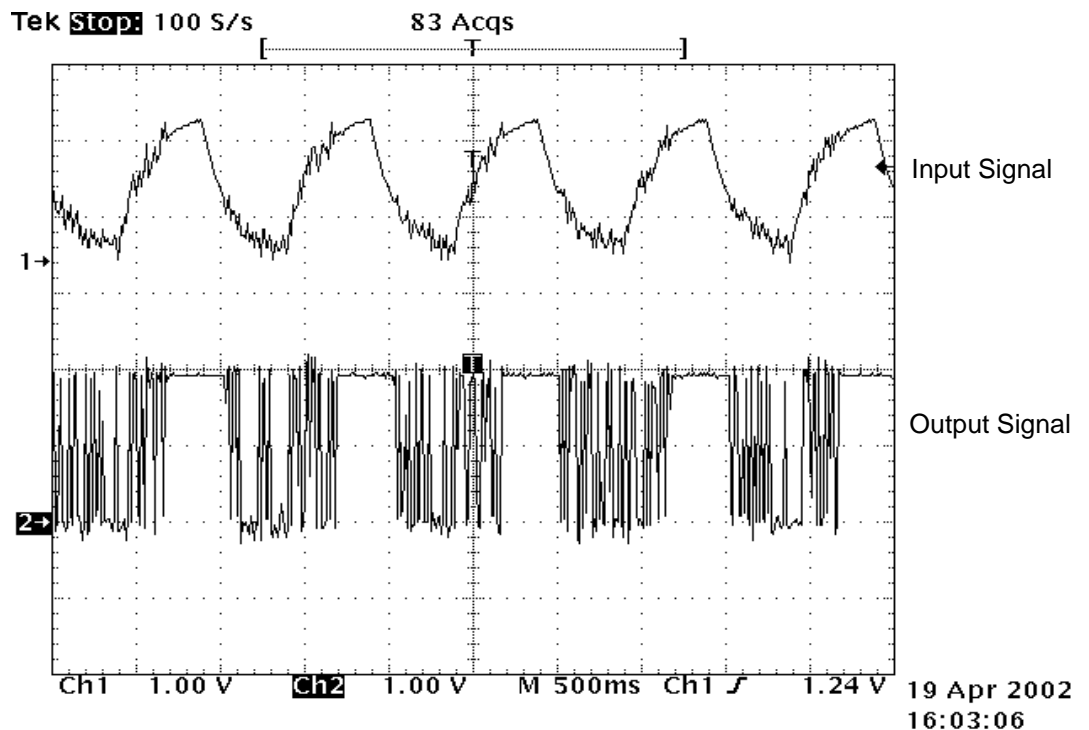


Figure 5: Non-Schmitt Waveforms

Now connect the output of the low pass filter to JP6-4 which is the Schmitt trigger input. View the output buffered signal corresponding to this input which is on JP6-5. The resulting display should be similar to **Figure 6**.

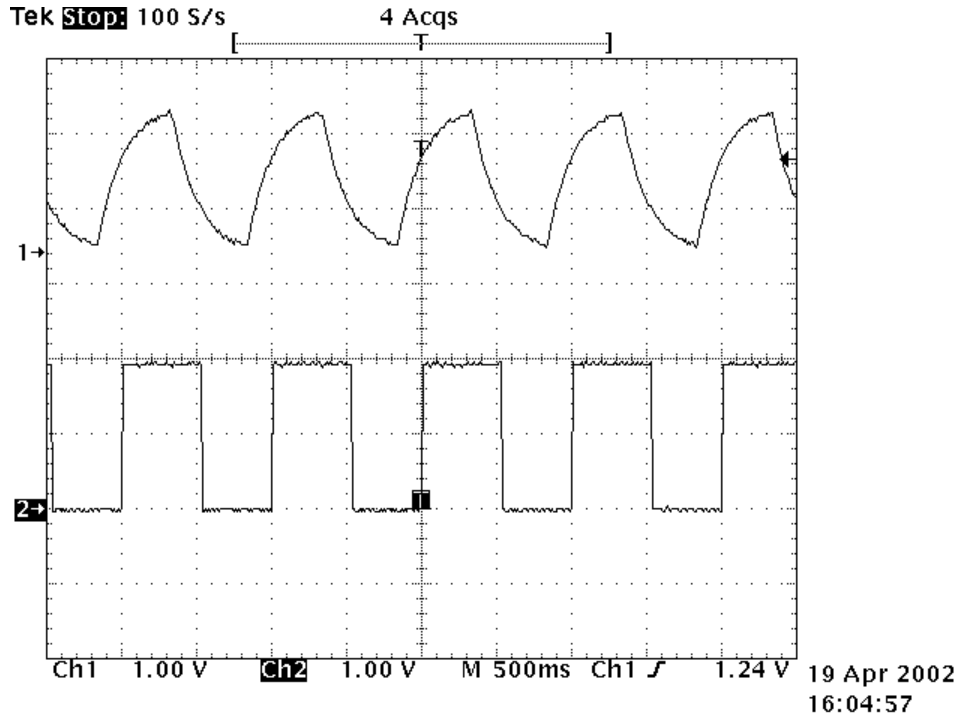


Figure 6: Schmitt Waveforms

Note that the output signal is significantly cleaner than when the non-Schmitt trigger input was used. There is no sign of buffer oscillation the output, and the buffer noise that was fed back to the input has disappeared. Also note the relative high-to-low and low-to-high transition points between the two traces: the Schmitt trigger buffer adds a small amount of hysteresis (approximately 500 mV) which shifts the transition points of the input buffer.

Schmitt trigger inputs should be used for slow-rising inputs, or when an output driver from a signal source is of a relatively high value (greater than 200 Ohms). In some instances, the decision to use Schmitt trigger inputs may be based upon purely empirical data. The CoolRunner-II devices allow the enabling of Schmitt trigger inputs on a pin-per-pin basis.

Demonstration 2: Dual Edge Flip Flops

Within the VHDL source code provided (demo_bd_cr2.vhd) there is a section of code starting on line 200 that is "commented out." Remove the "--" comment indicators from the start of the line, and place comment indicators preceding the text on line 206. When you are finished, your code should be similar to the code in **Figure 7**.

```

-----
--*****
-- UN-COMMENT the below line to infer the clock doubler for this shift register
--*****
    elsif (clk_scaler(10) 'event) then

--*****
-- COMMENT the below line when inferring the clock doubler for this shift register
--*****
        elsif (clk_scaler(10) 'event) and (clk_scaler(10) = '1') then
-----

```

Figure 7: Dual Edge Flip-Flop Source Modification

This modification will enable the DualEdge flip-flops for the section of code that is a shift register. The speed at which this shift register progresses controls the apparent rate of the LCD. Before processing and downloading the modified code, examine the previous rate at which the LCD display enables the individual segments. After downloading the modified file, the LCD display should scroll significantly faster. Note, however, that not all registers in the design are affected by the dual edge modification; therefore the display is scrolling faster but not twice as fast.

Demonstration 3 : Low Power Operation

The CoolRunner-II demo board may be used to demonstrate the low power consumption of the the CPLD. The most simple way to do this is to use a μA Ammeter to directly measure the power consumption of the CPLD/Clock/Display. There is no way to isolate the CPLD to measure just the power consumption of the CoolRunner-II device, but the power consumption of the oscillator and the LCD device are extremely low (on the order of $8\ \mu\text{A}$). A more involved but much more visual demonstration of the low power capabilities involves running the demo board using battery cells made from fruit. Both methods are described below.

Ammeter Measurement

To measure the power consumption of the CPLD, clock and LCD, use the original `demo_bd_cr2.vhd` source code and select the Pletronics oscillator as the clock source. The R/C clock uses significantly more power both because of the charging/discharging behavior of the capacitor in the R/C clock network and because slow rise and fall times force the input buffer to remain in the linear region longer.

If using the battery power supply and DC/DC converter as a power source, place jumper JP1 in the 1-2 position (which starts the DC/DC converter) and place the Ammeter in series with the V_{CC} current by replacing the shunt jumper on JP2 pins 1-2 with the Ammeter leads.

If using the Alternate Power pads, place jumper JP1 in the 2-3 position, remove the shunt jumper from JP2, and connect the Ammeter leads across JP2 : 2-3.

Current measurement of the entire board (including the DC/DC converter) can be made by placing JP2 shunt in the 1-2 position, removing JP1 shunt, and measuring total board power by putting the Ammeter leads across JP1 : 1-2.

Fruit Powered

The legacy of the CoolRunner devices includes operation from battery cells made from fruit. The original Fast Zero Power™ (FZP) devices were initially operated from grapefruit, subsequent technical experimentation has shown that other fruits and fluids such as fruit juices and vinegar will also provide adequate electrolyte for the cells.

Extensive testing using beer for an electrolyte also proved successful.

The CoolRunner-II Demo Board has been shown to operate from cells as small as those that are constructed from kumcuats. The alternate power pads are used as the power input for this demonstration.

In order to build up fruit cells for powering the demo board, three pieces each of copper and zinc are required for the electrodes. Solid 12-gauge (and larger) copper wire may be found at home improvement stores. Zinc electrodes may be made from galvanized nails, or by purchasing Zinc strips which are easily found at stained glass hobby shops. The larger the surface area of the electrodes, the better the cells will work.

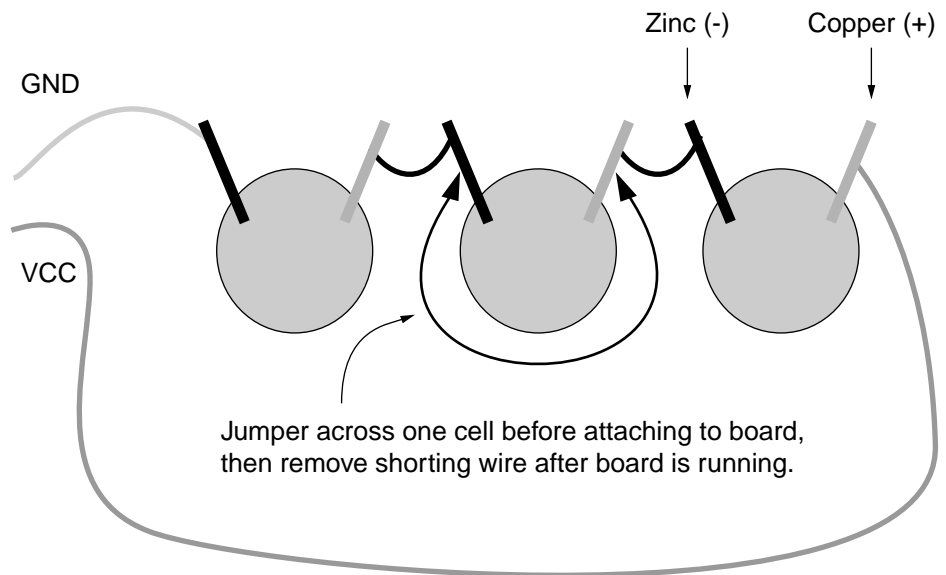
Important Note: Before making connections to cells, read the entire directions. CPLD damage may occur if the below steps are not followed correctly.

A cell is constructed by inserting one zinc and one copper electrode into each cell. Copper creates the positive electrode, and zinc becomes the negative electrode. Make sure that the electrodes are not contacting one another. Each cell has an output voltage potential of approximately 900 mV into a high-impedance load. Since a fruit cell has a relatively high series impedance, this available voltage drops as output current increases.

In order to provide enough potential to power the CPLD at a current consumption of 55 μ A, approximately three fruit cells in series are required to sum to an acceptable potential.

In order to get the demo board to start up, an inrush current is required to properly configure the CPLD. The demo board provides a 10 μ F capacitor (C1) which stores a charge across the Alternate Power pads. The fruit power array is attached to the Alternate Power pads while JP2 has the shunt jumper removed. Capacitor C1 is charged up with **two** fruit cells to a potential of approximately 1.8V, and then applied to the V_{CC} of the demo board by placing the shunt in the JP2 : 2-3 position. After the board is running, a third cell in series is applied to bring the operating voltage of the entire array up to approximately 1.8V under load. This will improve the contrast of the LCD on the demo board in operation.

It is important to not allow C1 to charge up using a three cell fruit battery, as the charge potential will exceed the safe operating range of the CoolRunner-II CPLD. A simple way to implement this demonstration is to build the three-cell battery before attaching it to the demo board, and use an alligator clip jumper to temporarily short out one cell. After the cell is shorted, attach the array to the power pads, allow C1 to charge, start the board, and then remove the shorting jumper from the shorted cell. Refer to **Figure 8** for a graphical representation of this technique.



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Figure 8: Fruit Cell Schematic

VHDL Code Download

VHDL source code and test benches are available for this design. THE DESIGN IS PROVIDED TO YOU "AS IS". XILINX MAKES AND YOU RECEIVE NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, AND XILINX SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR A PARTICULAR PURPOSE. This design has not been verified on hardware (as opposed to simulations), and it should be used only as an example design, not as a fully functional core. XILINX does not warrant the performance, functionality, or operation of this Design will meet your requirements, or that the operation of the Design will be uninterrupted or error free, or that defects in the Design will be corrected. Furthermore, XILINX does not warrant or make any representations regarding use or the results of the use of the Design in terms of correctness, accuracy, reliability or otherwise.

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Conclusion

The CoolRunner-II demo board was designed to promote the newest family of Xilinx CPLD product offerings. Equipped with a custom display, integrated DC/DC converter, two onboard clocks and push button inputs, and additional I/O interfacing, this board provides a small-form factor demonstration platform for a full-featured CPLD.

References

The components for this demo board were chosen specifically to suit the requirements of the project. Small size, low cost, ease of use, reliability, availability, and especially customer service/technical support were all factors in determining the optimal component solution for this low-power system. Additional information on the key components used may be found by contacting the below vendors. The contact list was created on May 13, 2002 and may change in time.

Table 5: Partner Vendors for CoolRunner-II Demo Board

| Ref. | Component | Manuf. | Contact |
|------|--|---------------------|---|
| L1 | DO1608C-333 DC/DC Inductor | Coilcraft | Info: http://www.coilcraft.com/do1608.cfm Spice Models: http://www.coilcraft.com/models Samples and 10k pricing available on web |
| D1 | MBR0520LT1 High Efficiency Schottky | ON Semiconductor | Home: http://www.onsemi.com Tech Support: http://www.onsemi.com/tech_support Tech Support Hotline: (800) 282-9855 |
| U6 | NCP1400ASN19T1 DC/DC Controller | ON Semiconductor | As Above |
| U5 | S3883-32.768K Micro Power Oscillator | Pletronics | Home: http://www.pletronics.com Info: http://www.pletronics.com/S3883.htm |

Revision History

The following table shows the revision history for this document..

| Date | Version | Revision |
|---------|---------|-------------------------|
| 09/1/02 | 1.0 | Initial Xilinx release. |