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PCB Pad Pattern Design and Surface-Mount Considerations for QFN Packages

Summary

Xilinx Quad Flat No-Lead (QFN) package is a robust and low profile leadframe-based plastic package that has several advantages over traditional leadframe packages.The exposed die attach paddle enables efficient thermal dissipation when directly soldered to the PCB. Additionally, this near chip scale package offers improved electrical performance, smaller package size, and an absence of external leads. Since the package has no external leads, coplanarity and bent leads are no longer a concern.

For QFN package to perform at the peak, special considerations are required to properly assemble the package and design the PCB. For optimal thermal, electrical, and board level performance, the exposed pad on the package should be soldered to the board using a corresponding thermal pad on the board. Also, for proper heat conduction through the board, the thermal pad region of the PCB should contain thermal vias.

The following factors have major effect on the quality and reliability of assembling QFN packages: PCB pad pattern design, amount of solder paste in thermal pad region, stencil design, type of solder paste, and reflow profile. This application note provides a good guideline on PCB pad pattern design and assembling of QFN packages for optimal reliability and quality. This is only a guideline and users are encouraged to perform actual studies to optimize the process.

PCB Pad Patterns

Figure 1 below shows the PCB pad pattern dimensions to be determined. The dimension X and Y indicate the width and length of the pad. CLL and CPL define the clearances needed to avoid solder bridging. CLL defines the minimum distance between land to land for the corner joints on adjacent sides and CPL defines the minimum distance between the inner tip of the peripheral lands and the outer edge of the thermal pad. CLL should be 0.1 mm and CPL should be 0.15mm.

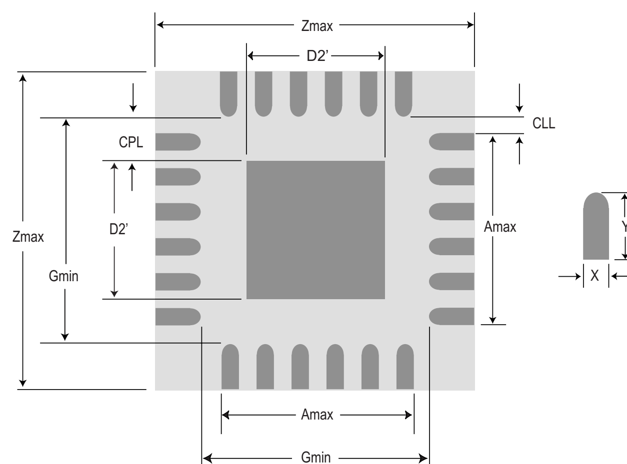

Figure 1: **PCB Land Pattern Dimensions**

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Tolerance analysis should be performed on the package and the PCB dimensions in order to design a proper pad pattern. The recommended PCB land pattern dimensions are shown in Table 1.

Table 1: **Recommended PCB Land Pattern Dimensions (all dimensions in mm)**

Package			PCB Land Pattern Dimensions					
Package	**Body Size**	**Lead Pitch**	**Xmax**	**Yref**	**Amax**	**Gmin**	**Zmax**	**D2max**
QFG32	5 x 5	0.50	0.28	0.69	3.78	3.93	5.31	3.63
QFG48	7 x 7	0.50	0.28	0.69	5.78	5.93	7.31	5.63

Thermal Pad and Via Design

Typical deployment of a QFN package has a thermal resistance (theta-JA) of 35 - 45º C/Watt (depending on package size). When needed, the base performance can be improved and a lower overall theta-JA is achieved by taking advantage of the exposed thermal pad feature. To take advantage of the exposed thermal pad under the package, the PCB should incorporate thermal pad and thermal vias. The thermal pad on the PCB acts as a solderable surface and the thermal vias provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat. The number of thermal vias will depend on the following: application, power dissipation and electrical requirements. The thermal performance gets better as more thermal vias are added. However, there is a point of diminishing returns as shown in Figure 2 where the effect of number of vias on theta-JA is plotted for a 7mm, 48 lead package. A via diameter of 0.3 mm was used for this simulation.

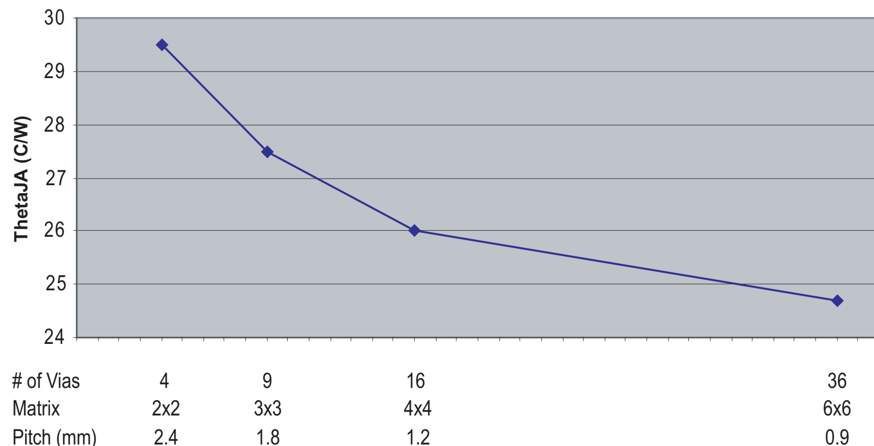

Figure 2: **Theta-JA vs. Number of Vias Graph**

Based on the above and similar thermal simulations, it is recommended to incorporate an array of thermal vias that have pitch of 1.0 to 1.2 mm with via diameter of 0.3 to 0.33 mm.

Solder Masking Considerations

The PCB have pads that are either solder mask defined (SMD) or non solder mask defined (NSMD). NSMD pads are preferred over SMD pads since the copper etching process has tighter control than the solder masking process. Furthermore, NSMD pads with solder mask opening larger than the metal pad size improves the reliability of the solder joints as solder is allowed to wrap around the sides of metal pads.

The solder mask opening should be larger than the pad size by 120 to 150 microns. This results in a clearance of 60 – 75 microns between the copper pad and the solder mask.

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The thermal pad area may be solder mask defined in order to avoid any solder bridging between the thermal pad and the perimeter pads. The mask opening should be 100 microns smaller than the thermal land size on all four sides.

Stencil Design for Perimeter Pads

To achieve reliable solder joints, the solder joints on the perimeter pads should have about 50 to 75 microns standoff height and good side fillet on the outside. Good stand off can be achieved by having a stencil aperture opening that allows for maximum paste release. This is accomplished by having an area ratio that is greater than 0.66 and an aspect ratio that is greater than 1.5. Area Ratio and Aspect Ratio is defined below:

Area Ratio = LW/2T(L+W)

Aspect Ratio = W/T

Where L and W are the aperture length and width, and T is the stencil thickness. The stencil aperture should have a 1:1 ratio with the PCB pad sizes as both area and aspect ratio targets can easily be achieved by this aperture. Also, the stencil should be laser cut and electro-polished.

Stencil Design for Thermal Pad

To enhance thermal and electrical performance, the die paddle should be soldered to the PCB thermal pad. Since outgassing occurs during reflow process and may cause defects such as splatter and solder balling, care must be taken to avoid large solder paste coverage. Thus, it is recommended to use smaller multiple openings in the stencil instead of one big opening for printing solder paste on the thermal pad area. By doing this, 50 to 80% solder paste coverage can be achieved. Figure 3 below shows one way to achieve these levels of solder paste coverage.

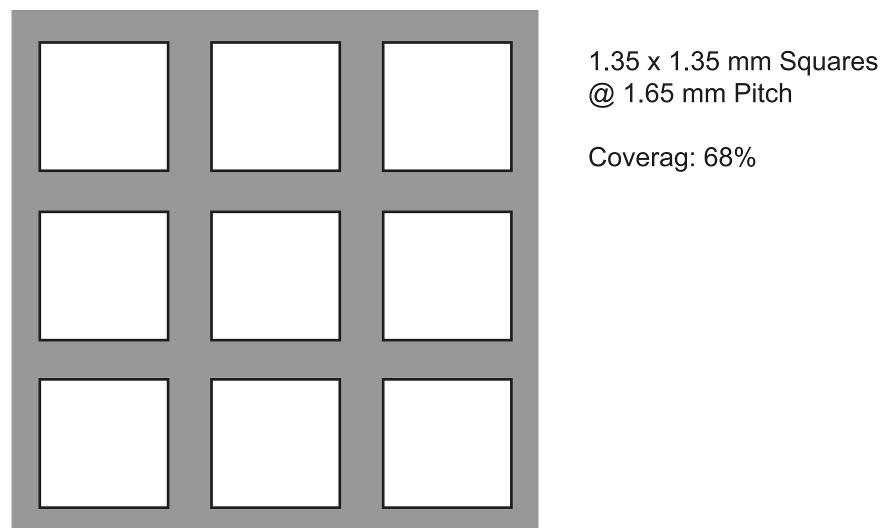

Figure 3: **Thermal Pad Stencil Design**

Via Types and Solder Voiding

Voids in the thermal pad region are not expected to degrade thermal and electrical performance. However, large voids in the thermal pad area should be avoided. To control these voids, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow. Methods commonly used in the industry to control the voids include “via tenting” (top or bottom side) using dry film solder mask, “via plugging” with liquid photo-imageible (LPI) solder mask from the bottom side, or “via encroaching”. Figure 4 shows these options. For via tenting, the solder mask diameter should be 100 microns larger than the diameter of the via.

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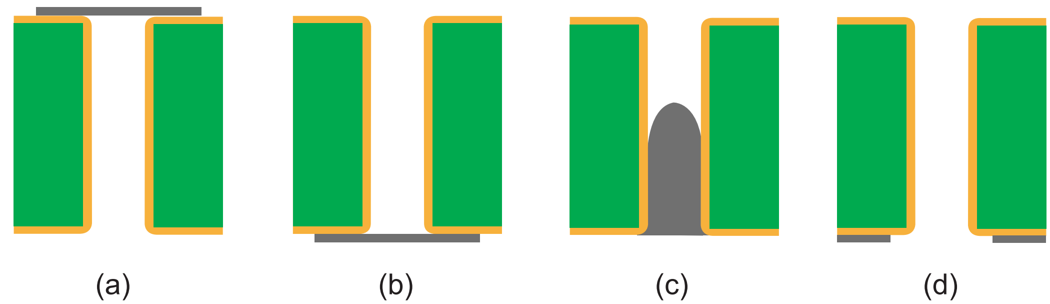

Figure 4: **Solder mask options for thermal vias: (a) via tenting from top, (b) via tenting from bottom, (c) via plugging from bottom, and (d) via encroached from bottom.**

There are advantages/disadvantages to each of these options. Via tenting from top side may result in smaller voids, but the presence of solder mask on the top side of the board may hinder proper paste printing. Via tenting from the bottom and via plugging from the bottom may result in larger voids because of outgassing. Finally, encroached vias allow the solder to wick inside the vias and reduce the size of the voids. This option, however, result in lower standoff of the package.

Stencil Thickness and Solder Paste

For 0.5 mm pitch parts, a stencil thickness of 0.125 mm is recommended. Also, to improve the paste release, a stainless steel stencil with electro-polished trapezoidal walls is recommended.

For the paste, it is recommended to use “No Clean”, Type 3 paste. Since the pads on the package are plated with 100% matte Sn, the package can be soldered using either Pb-free or SnPb solder paste.

Reflow Profile

Reflow profile for QFN packages is similar to reflow profile of other SMT packages. It is recommended to follow the paste manufacturer’s specification on peak reflow temperature, soak times, time above liquidus, and ramp rates. Typical profile for Sn/Pb solder paste has peak temperature between 220 – 235º C with time above liquidus between 60 – 90 seconds. For Pb-free solder paste, the typical profile has peak temperature between 245 – 260º C and time above liquidus in the 60 – 90 seconds range.

References

Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages, Dec. 2003.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/11/05	1.0	Initial release.

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