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Spread-Spectrum Clocking Reception for Displays

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Summary

Consumer Display applications like flat-panel displays and video players commonly use high-speed Low Voltage Differential Signaling (LVDS) interfaces to transfer video data. To address Electromagnetic Compatibility (EMC) issues, spread-spectrum clocking can be used to reduce th impact of radiated energy produced by these signals. When a spread-spectrum clock is used as the source from which these signals are derived, the radiated energy is spread across a range of frequencies, effectively reducing the peak energy at any one frequency.

This application note shows that a spread-spectrum clock will drive the LVDS interfaces of Spartan®-3E and Extended Spartan-3A family devices with no adverse effects on a system's performance. It describes how to estimate the maximum spread-spectrum clock modulation frequency for the Digital Clock Manager (DCM) and describes a simple test setup to evaluate the effects of the spread-spectrum clock on a typical LVDS communications path.

Note: This application note applies to Spartan-3E and Extended Spartan-3A family devices ONLY.

Reducing EMI with a Spread-Spectrum Clock

Manufacturers of electronic devices must ensure their products do not emit levels of electromagnetic energy that interfere with the operation of other nearby electronic devices. For example, the clarity of a phone call should not worsen when the phone is next to a video display. In the same way, the display should not be affected when the phone is being used.

EMC regulates the noise or Electromagnetic Interference (EMI) that causes these disturbances. Typical solutions for meeting EMC requirements involve adding expensive shielding, ferrite beads, or chokes. These solutions can adversely impact the cost of the final product by complicating PCB routing and forcing longer product development cycles.

To confirm EMC regulations are met, the field strength of the electromagnetic energy radiating from a working product is measured. An antenna measures the field strength across a range of frequencies at various distances from the product being tested. If the field strength at any frequency violates the specified field strength levels (Table 1), the product could potentially interfere with other products.

Table 1: **Maximum Acceptable EMC Levels**

Frequency (MHz)	FCC[1] Field Strength (dBμV/m) @ 10 meters	CISPR[2] Field Strength (dBμV/m) @ 10 meters
88	29.5	30
216	33	30
230	35.6	30
960	35.6	37

Notes:

1. FCC: Federal Communications Commission.
2. CISPR: International Special Committee on Radio Interference.

A spread-spectrum clock reduces the peak electromagnetic energy at any one frequency by modulating its output. This resulting variation in output frequency spreads the energy across a

range of frequencies, reducing the peak EMI at any one frequency. Figure 1 shows the frequency output of a spread-spectrum clock.

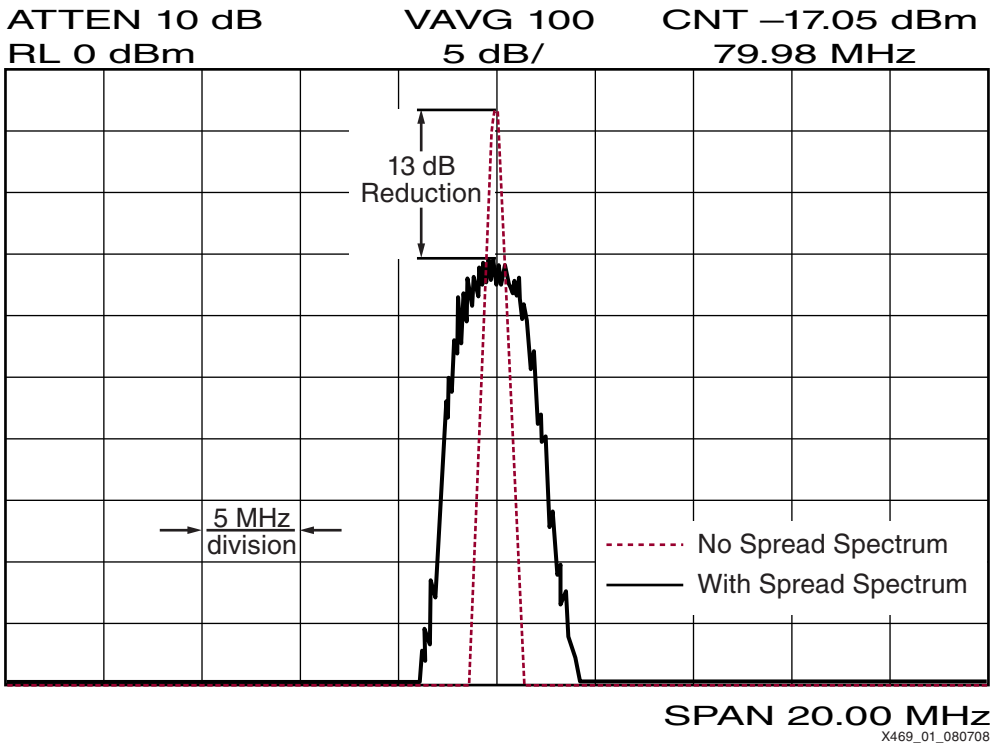

Figure 1: **Spread-Spectrum Energy Distribution**

A triangular modulation waveform is shown in Figure 2. The modulation frequency, the deviation, and the shape of the modulation waveform are factors in reducing EMI levels. The modulation frequency determines the rate at which the clock sweeps through the range of frequencies. Deviation defines the range of swept frequencies. The shape of the modulation waveform changes the shape of the output spectrum.

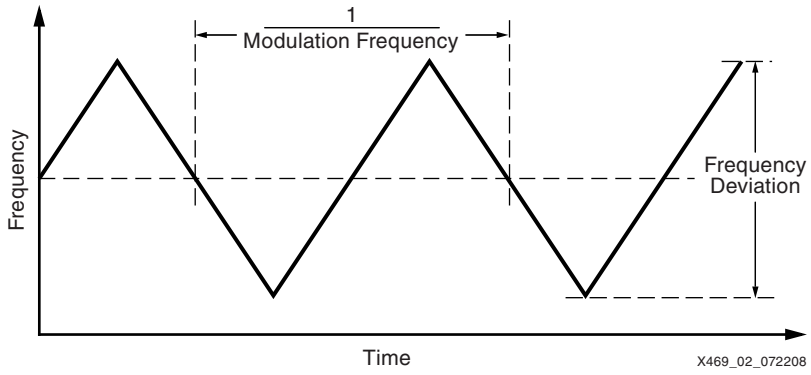

Figure 2: **Spread-Spectrum Triangular Modulation Profile**

Common modulation waveform shapes include sinusoids, triangles, and the *Lexmark* or *Hershey's Kiss* profile (Figure 3) originally developed by Lexmark International. The Hershey's Kiss waveform flattens the top of the spectral energy profile over the deviation range to further reduce EMI levels. Because DCM performance depends on the rate (slope) of the frequency change, a modulation waveform having a constant slope yields a simpler analysis and still provides good performance. For this reason, a triangular profile is used in the rest of this discussion.

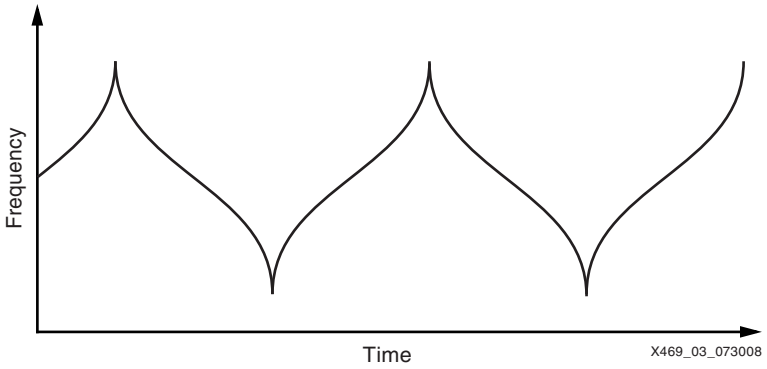

Figure 3: **Hershey's Kiss Modulation Profile**

Spread-spectrum clocks are available that define the frequency changes relative to the oscillator source frequency in one of three ways. Center-spread variation distributes the frequency changes above and below the source frequency. Down-spread variation distributes the frequency changes below the source frequency. Up-spread variation distributes the entire frequency change above the input frequency. Regardless of the spreading style, the designer must consider operation at the highest frequency output by the spread-spectrum clock to guarantee proper DCM performance.

When selecting a spread-spectrum clock for use with the DCM, consider the effects of both frequency variation and modulation frequency. A wide frequency deviation reduces EMI by distributing energy over a broader spectrum, reducing the maximum energy at any given frequency. However, if the modulation frequency rate of change is too fast, cycle-to-cycle jitter can exceed acceptable levels.

DCM Settings for Use with a Spread-Spectrum Clock

To create the high-speed clocks used by the receiver's deserializer, the DCM multiplies the frequency of the incoming spread-spectrum clock. To maintain phase and frequency alignment, the DCM must follow the spread-spectrum clock source (Figure 4) and update the deskewing and phase shifting without distorting the source.

Figure 4: **Tracking DCM Frequency Over Time**

To determine the acceptable range of operation for the DCM, a calculation can be made to estimate the acceptable limits of the modulation frequency for a given frequency deviation.

Beyond these limits, the DCM phase and frequency alignment deteriorates, reducing the receiver's skew margin.

Maximum Modulation Frequency, DLL

Video display receiver designs use both the Delay-Locked Loop (DLL) and Digital Frequency Synthesizer (DFS), with the DLL providing the digital deskew circuit. Equation 1 estimates the maximum modulation frequency (F_{mDLL}) for a spread-spectrum clock for a given input frequency. The dashed line shown in Figure 5 shows the resulting curve for a range of input frequencies.

$$F_{mDLL} < \frac{\text{DCM\_DELAY\_STEP}}{(24 \times S \times T_{in}^{2})} \qquad \textit{Equation 1}$$

F_{mDLL} = Maximum modulation frequency (Hz) that the DLL can follow

DCM_DELAY_STEP = Finest delay resolution (seconds) for the DCM from the FPGA data sheet (see the table called Switching Characteristics for the DLL)

S = Maximum spread or frequency deviation (%)

T_{in} = Shortest effective input clock period (seconds)

24 = Factory-based constant related to the update rate of DLL frequency and phase adjustments

Maximum Modulation Frequency, DFS

The DFS provides a range of output frequencies based on the ratio of two user defined integers, a multiplier (CLKFX_MULTIPLY), and a divisor (CLKFX_DIVIDE). Equation 2 estimates the maximum modulation frequency (F_{mDFS}) for a spread-spectrum clock for a given input frequency. The solid line shown in Figure 5 shows the resulting curve for a range of input frequencies.

$$F_{mDFS} < \frac{\text{DCM\_DELAY\_STEP}}{(2 \times M \times D \times S \times T_{in}^{2})} \qquad \textit{Equation 2}$$

F_{mDFS} = Maximum modulation frequency (Hz) that the DFS can follow

DCM_DELAY_STEP = Finest delay resolution (seconds) for the DCM from the FPGA data sheet (see the table called Switching Characteristics for the DLL)

M = CLKFX_MULTIPLY

D = CLKFX_DIVIDE

S = Maximum spread or frequency deviation (%)

T_{in} = Shortest effective input clock period (seconds)

2 = Factory-based constant related to the update rate of DFS frequency and phase adjustments

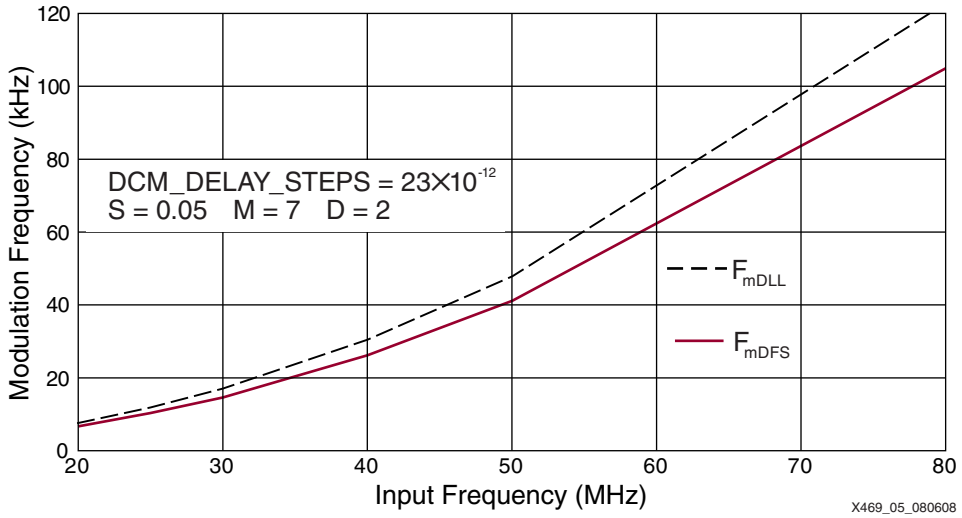

Figure 5: **Maximum DCM Modulation Frequency**

Example

For applications using both the DFS and DLL, the maximum modulation frequency is determined by the lower of the two curves shown in Figure 5. The DCM settings in Figure 6 are used for the tests summarized in the Characterization Methodology section. These parameters represent the 7:1 LVDS designs commonly found in displays. Setting **CLKFX_MULTIPLY** = 7 and **CLKFX_DIVIDE** = 2, the DCM multiplies the clock to 3.5 times the original frequency. Using a double data rate (DDR) register as described in *1:7 Deserialization in Spartan-3E/3A FPGAs at Speeds Up to 666 Mbps* [Ref 1] and *7:1 Serialization in Spartan-3E FPGAs at Speeds Up to 666 Mbps* [Ref 2] provides the full 7X data rate multiplication.

```
dcm_rxclka : dcm_sp
     generic map (
          DESKEW_ADJUST => "0", --banks 0/2
          --DESKEW_ADJUST => "3", --banks 2/3
          CLKFX_MULTIPLY => 7,
CLKFX_DIVIDE => 2,
          PHASE_SHIFT => 55,
          CLKOUT_PHASE_SHIFT => "FIXED");
```

Figure 6: **Typical DCM Settings For Display Applications (VHDL Example)**

Note: When using a spread-spectrum clock, fixed phase shifting should be used (`CLKOUT_PHASE_SHIFT => "FIXED"`). Setting `CLKOUT_PHASE_SHIFT => "VARIABLE"` disables the internal phase shift controls that update phase shift with changing frequency. Because of this, variable phase shifting should not be used with spread-spectrum clock inputs.

Applying the DCM settings from Figure 6 and using Equation 1 and Equation 2, and using the typical DCM_DELAY_STEP value of 23 ps from the *Spartan-3A FPGA Family: Data Sheet* [Ref 3], the limits for a 75 MHz spread-spectrum clock having a 5% frequency deviation can be estimated as indicated in Equation 3 and Equation 4.

$$F_{mDLL} < \frac{23 \times 10^{-12}}{(24 \times 0.05 \times (13.3x10^{-9})^{2})} = 108 \text{ kHz} \qquad \textit{Equation 3}$$

$$F_{mDFS} < \frac{23 \times 10^{-12}}{(2 \times 7 \times 2 \times 0.05 \times (13.3x10^{-9})^2)} = 92.9 \text{ kHz} \qquad \textit{Equation 4}$$

Designs for display functions using PPDS or MINI_LVDS might need other serialization ratios such as 10:1 or 8:1. The ability of the DCM to track the spread-spectrum clock when multiplying is a function of the multiply and divide values used in Equation 2. Therefore, for other display functions such as PPDS (M = 5, D = 1) or MINI_LVDS (M = 4, D = 1), the modulation frequency threshold is actually higher than the 7X analysis presented here.

Characterization Methodology

To evaluate the potential impact of a spread-spectrum clock on a system, a typical display environment was modeled using a 75 MHz pixel clock with a 525 Mb/s data rate (Figure 7). To test the receiver's ability to correctly follow spread-spectrum signals, a spread-spectrum source was created for the transmitter circuit. Clock and data derived from this source were transmitted on a loop to the receiver inputs. In the receiver, the spread-spectrum clock signal drives the DCM, which in turn drives the serializer circuitry. The serialized data was then compared to the transmitted data to confirm that the receiver circuitry follows the spread-spectrum source correctly.

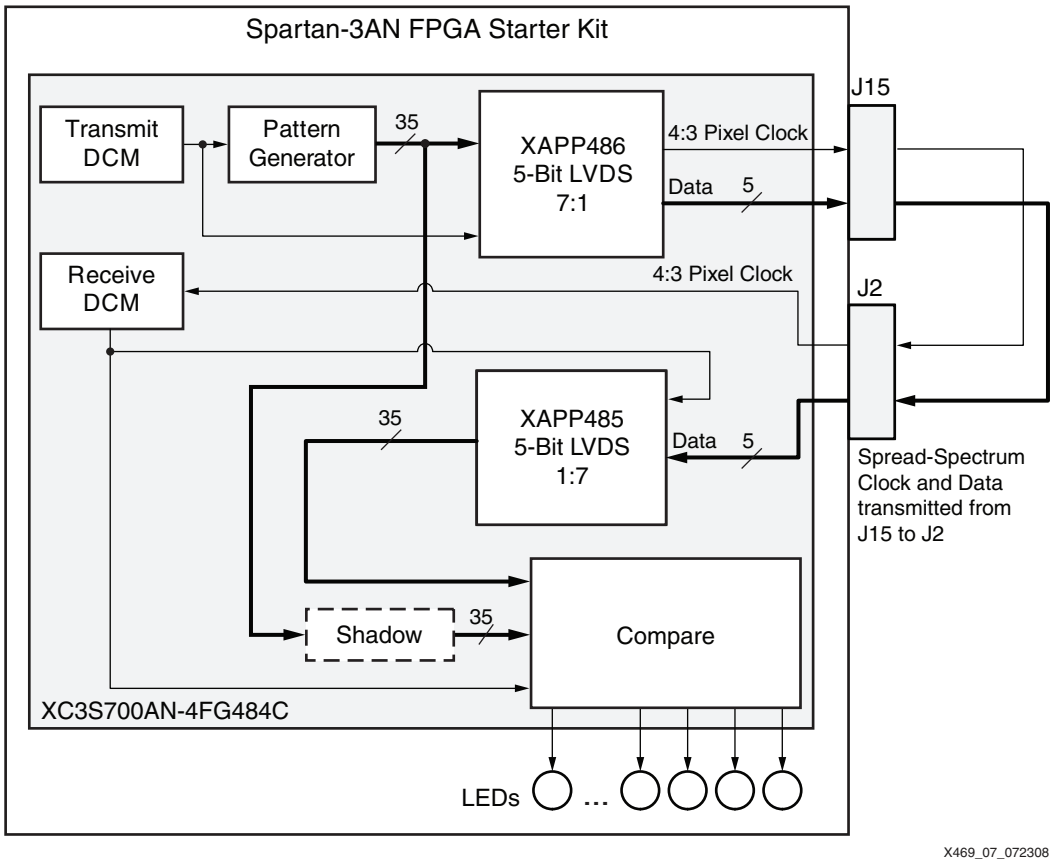

Figure 7: **Spread-Spectrum Loopback Test**

To evaluate the quality of reception, the eye width was measured by testing the phase shift values that were correctly receiving the loopback test data. The number of phase shift values that correctly received the transmitted data indicated the receiver's skew margin. The skew margin with the spread-spectrum clock was then compared to a system run without a spread-spectrum clock (Figure 8).

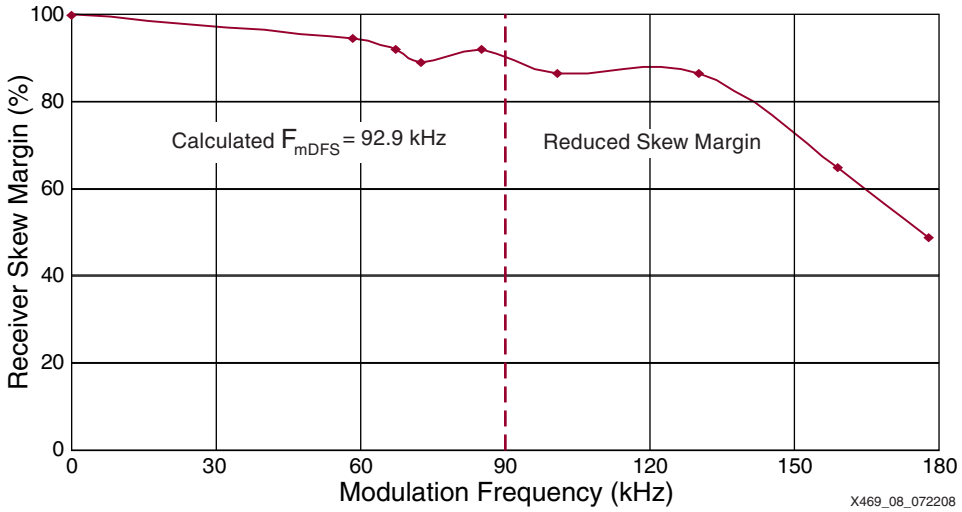

Figure 8: **Testing of 75 MHz Frequency Modulation**

Testing was performed at pixel clock frequencies of 20, 50, and 75 MHz. Modulation frequencies were selected to identify the limit of the DCM's ability to follow the spread-spectrum clock as indicated by a decrease in skew margin exceeding 5%. From Equation 2, the DFS should be able to follow a 5% frequency deviation up to 90 kHz. Test results confirmed little change in the receiver's skew margin as the modulation frequency was increased to 130 kHz.

Based on these results, Xilinx recommends using the lowest possible frequency deviation and modulation frequency to meet EMC requirements.

Other Methods for Reducing EMI

In addition to being compatible with spread-spectrum clocks, the Extended Spartan-3A family can further reduce EMI by controlling the I/O type selected in the SelectIO™ interfaces.

Another potential source of EMI is the ringing created by the fast switching of traditional LVCMOS and LVTTL outputs. The Extended Spartan-3A family provides LVCMOS and LVTTL I/Os with separate SLEW rate and DRIVE strength attributes. Setting the SLEW rate to SLOW or QUIETIO in the Extended Spartan-3A family reduces ringing. When setting the slew attribute to **FAST**, reducing the drive strength can reduce ringing.

Noisy LVTTL interfaces used by LCD modules are being replaced with more EMC compliant differential interfaces like reduced swing differential signaling (RSDS), MINI_LVDS, and even point-to-point differential signaling (PPDS). The Extended Spartan-3A family can directly drive these differential interfaces, further reducing EMI.

For more information on SelectIO interface standards, see *Spartan-3 Generation FPGA User Guide* [Ref 4].

Conclusion

This document shows how to use a spread-spectrum clock with Spartan-3E and Extended Spartan-3A family FPGAs for video applications. The DCM functions normally, but the phase shift must be set to **FIXED**. To estimate the limit of the spread-spectrum clock modulation frequencies that the DCM can follow, this application note provides mathematical models and then validates them in hardware. While the focus is specifically on LVDS display applications, applications with similar DCM usage can also use a spread-spectrum clock.

References

This document uses the following references:

1. XAPP485, *1:7 Deserialization in Spartan-3E/3A FPGAs at Speeds Up to 666 Mbps*.
2. XAPP486, *7:1 Serialization in Spartan-3E FPGAs at Speeds Up to 666 Mbps*.

3. DS529, *Spartan-3A FPGA Family: Data Sheet*.
4. UG331, *Spartan-3 Generation FPGA User Guide*.

Additional Resources

The following resources provide additional information useful for the subject covered in this application note:

1. Federal Communications Commission, http://www.fcc.gov.
2. American National Standards Institute, http://www.ansi.org.
3. International Special Committee on Radio Interference, National Telecommunications and Information Administration, http://www.ntia.doc.gov/osmhome/international/cispr.html.
4. Flat Panel Displays, National Semiconductor, http://www.national.com/appinfo/fpd/.
5. Engineering Note 290: *Comparison of FCC Limits with CISPR Limits*, Communication Certification Laboratory, http://www.cclab.com/engnotes/eng290.htm.
6. UG334, *Spartan-3A/3AN Starter Kit Board User Guide*.
7. DS312, *Spartan-3E FPGA Family: Data Sheet*.
8. DS557, *Spartan-3AN FPGA Family Data Sheet*.
9. DS610, *Spartan-3A DSP FPGA Family: Data Sheet*.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
08/22/08	1.0	Initial Xilinx release.

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