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3.3V PCI Design Guidelines

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Summary

This application note describes the 3.3V PCI™ solution for the Virtex®-5, Virtex-4, and Virtex-II Pro families. For 3.3V I/O design guidelines for the Spartan®-3 Generation families, refer to [XAPP457](#).

The 3.3V regulator reference design described in this application note is verified to work with the Virtex family I/O pins, operating in the 3.3V PCI I/O standard.

PCI Compliance

The PCI Compliance Specification requires the clamp diodes to withstand -3.5V and 7.1V pin voltages for 11 ns in undershoot and overshoot tests, respectively. The only exception is the PCI clock pin.

Figure 1 shows the compliance test setup and requirements. This figure is extracted from the PCI Compliance Specification.

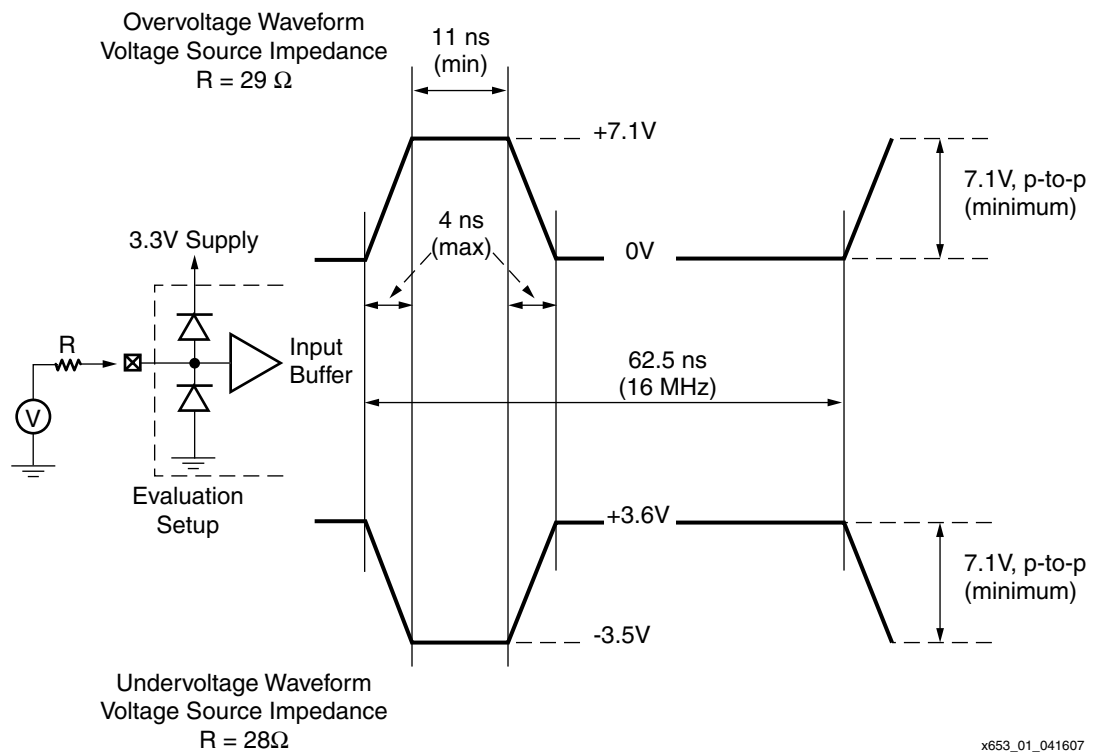


Figure 1: PCI Overshoot/Undershoot Compliance Test Requirements

Virtex-5 and Virtex-II Pro Devices

To meet the PCI compliance requirement, Xilinx recommends regulating the Virtex-5 and Virtex-II Pro FPGA V_{CCO} at 3.0V (the minimum PCI V_{CCO} compliance requirement) to extend the lower absolute maximum limit. The lower absolute maximum limit is derived from this equation:

$$\text{Undershoot}_{MAX} = V_{CCO} - GOS_{MAX} \quad \text{Equation 1}$$

where GOS_{MAX} (maximum gate oxide stress) is a constant 4.05V.

The upper absolute maximum limit is derived from [Equation 2](#).

$$\text{Overshoot}_{MAX} = \text{Ground} + GOS_{MAX} \quad \text{Equation 2}$$

Hence, maximum overshoot is 4.05V, regardless of V_{CCO} level.

When V_{CCO} is 3.75V (the absolute maximum supply voltage for Xilinx® FPGAs), Undershoot_{MAX} becomes -0.3V. When V_{CCO} is lowered to 3.0V, Undershoot_{MAX} is extended to -1.05V, based on [Equation 1](#).

In this case, the ground clamp diode turns on at approximately -0.6V, clamping the pin voltage before it reaches the absolute maximum limit. However, the voltage across the diode increases as more current passes through it. To determine the exact voltage across the ground clamp diode, use [Equation 3](#).

$$I_D = (V_S - V_D - GND) / R \quad \text{Equation 3}$$

where:

- I_D is the diode current
- V_S is the source voltage
- V_D is the diode voltage drop
- GND is ground
- R is the source voltage impedance

Because I_D and V_D are unknown, V_D value is assumed. The corresponding I_D is compared against the IBIS models to validate the assumption.

Based on the PCI undershoot test conditions, V_S is 3.5V and R is 28Ω. The assumption is that V_D is 0.9V, and it is applied in [Equation 3](#) as follows:

$$I_D = 3.5 (0.9) / 28 = 93 \text{ mA}$$

The result implies the diode current I_D is 93 mA when V_D is 0.9V. Since it closely corresponds to the ground clamp diode I-V characteristics found in published IBIS models ([Table 1, page 4](#)), the assumption is valid. In other words, when a 3.5V source voltage is applied to the Virtex-5 or Virtex-II Pro FPGA I/O through a 28Ω resistor, the ground diode clamps at 0.9V.

Similar to [Equation 3](#), current going through the power clamp diode during the PCI overshoot test is calculated as follows:

$$I_D = (V_S - V_D - V_{CCO}) / R$$

Based on the PCI overshoot test conditions, V_S is 7.1V and R is 28Ω.

The assumption is that V_D is 1.0V, and it is applied in [Equation 3](#):

$$I_D = 7.1 - 1.0 - 3.0 / 29 = 106 \text{ mA}$$

The result implies the diode current I_D is 106 mA when V_D is 1.0V. Since it corresponds to the power clamp diode I-V characteristics found in published IBIS models (refer to [Table 2, page 5](#)),

the assumption is valid. In other words, when a 7.1V source voltage is applied to the Virtex-5 or Virtex-II Pro FPGA I/O through a 28 Ω resistor, the power diode clamps at 4.0V.

In summary, the ground and power clamp diodes can meet the PCI undershoot and overshoot compliance requirements (assuming $V_{CCO} = 3.0V$) because of the following:

- The ground clamp diode limits the pin voltage to $-0.9V$ before reaching the lower absolute maximum limit of $-1.05V$.
- The power clamp diode limits the pin voltage to 4.0V before reaching the upper absolute maximum limit of 4.05V.

Virtex-4 Devices

As stated in the data sheet for the Virtex-4 family, when more than 100 I/Os are used, the Virtex-4 device absolute maximum V_{IN} limit is 4.05V, and the absolute minimum V_{IN} limit is $-0.95V$. In this case, as described in the previous section, regulating V_{CCO} at 3.0V applies.

However, these limits are relaxed when 100 or fewer I/Os are used. In such cases, the maximum V_{CCO} can be set to 3.35V for commercial grade or 3.25V for industrial grade devices.

Additional Information

For additional I/O information, see [UG072](#), *Virtex-4 PCB Designer's Guide*, [UG203](#), *Virtex-5 PCB Designer's Guide*, and [XAPP659](#), *Virtex-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines*.

Voltage Regulation

Regulator Reference Design

The reference design schematic shown in [Figure 2](#) provides a solution for regulating V_{CCO} at 3.0V. It offers electrical compliance to the PCI standard for Virtex-5, Virtex-4, and Virtex-II Pro FPGA designs. This low-cost solution uses minimal PC board space and has been verified.

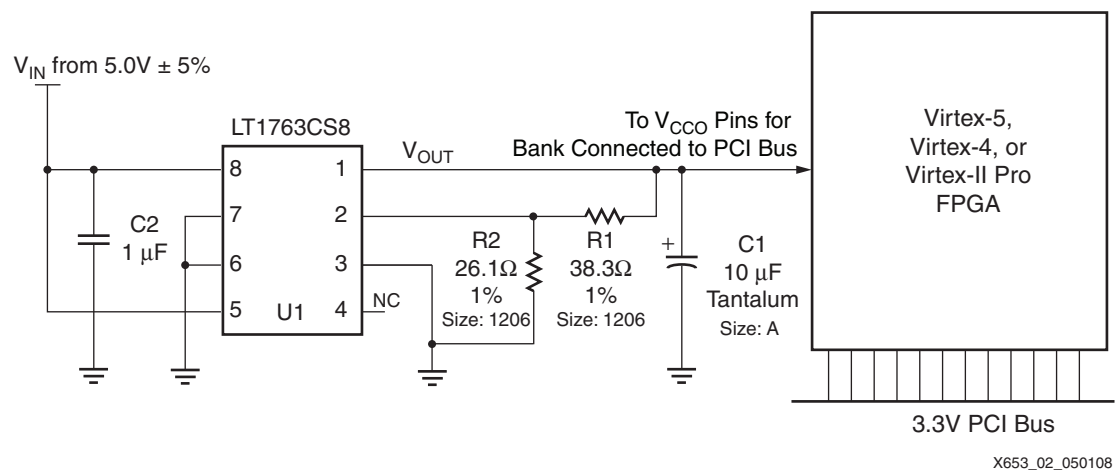


Figure 2: Reference Design Schematic

Regulator Implementation

The highlighted elements in [Figure 3](#) (U1, R1, R2, C1, and C2) comprise the regulator implementation on a typical FPGA PCB layout. This configuration supplies a V_{OUT} tightly regulated at 3.0V for the 3.3V PCI V_{CCO} banks. The LT1763CS8 regulator covers an industrial operating temperature range since the regulator has a junction temperature range of $-40^{\circ}C$ to $+125^{\circ}C$. The reference design provides a fully compliant PCI electrical interface for Virtex-5, Virtex-4, and Virtex-II Pro devices. Depending on PCI performance requirements, the PCI33 or PCI66 I/O standard for the I/Os connecting to the PCI bus should be used.

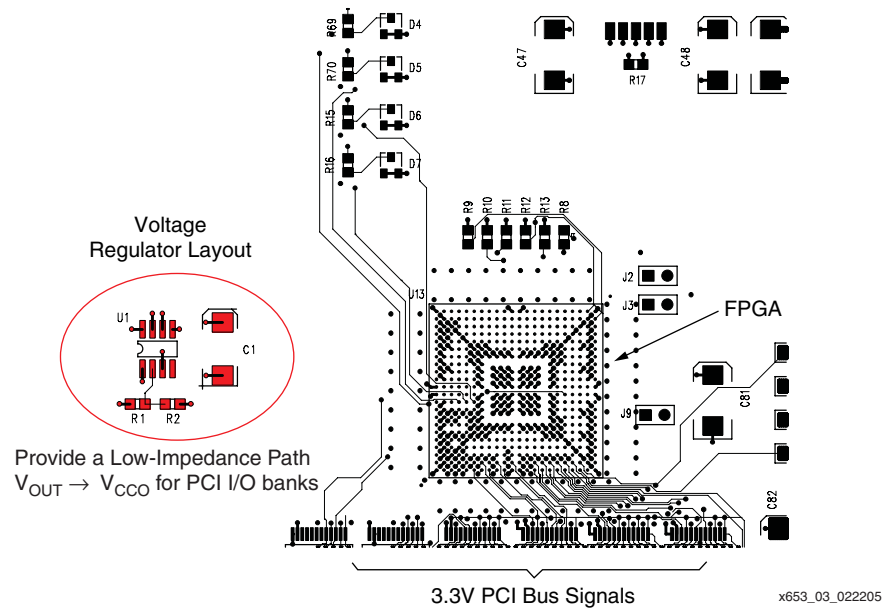


Figure 3: Layout Area Example

Linear Technology - LT1763CS8 Devices

Linear Technology manufactures the low noise, low dropout, micropower LT1763 series of regulators. These devices are capable of supplying 500 mA of output current with a dropout voltage of 300 mV. Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting, and reverse current protection. The LT1763CS8 regulator used in this application is an adjustable device with a 1.22V reference voltage. For regulator details from Linear Technology, see the data sheet at the Linear Technology website at the following URL: <http://www.linear.com>.

Solution Cost

The total cost of the solution shown in Figure 2 is estimated to be less than \$2.00 in 1000-piece quantities. This estimate includes the LT1763CS8 regulator, resistors, and 3.3 μF capacitor.

Appendix

Table 1 and Table 2 show the voltage-current characteristics of Virtex-II Pro FPGA I/O protection diodes under different temperature and voltage conditions. This data, along with additional information about the I/O drive capability, is located in the IBIS models.

Table 1: Virtex-II Pro FPGA Ground Clamp Diode I-V Characteristics

External Pin Voltage	I (typ) ⁽¹⁾	I (min) ⁽²⁾	I (max) ⁽³⁾	Unit of Measure
-3.3000	-4.9900	-4.5330	-4.9880	A
-3.2000	-4.7610	-4.3320	-4.7580	A
-3.1000	-4.5320	-4.1310	-4.5280	A
-3.0000	-4.3030	-3.9300	-4.2980	A
-2.9000	-4.0740	-3.7280	-4.0680	A
-2.8000	-3.8450	-3.5270	-3.8380	A
-2.7000	-3.6160	-3.3260	-3.6080	A
-2.6000	-3.3870	-3.1260	-3.3780	A
-2.5000	-3.1580	-2.9250	-3.1480	A

Table 1: Virtex-II Pro FPGA Ground Clamp Diode I-V Characteristics (Continued)

External Pin Voltage	I (typ) ⁽¹⁾	I (min) ⁽²⁾	I (max) ⁽³⁾	Unit of Measure
-2.4000	-2.9290	-2.7260	-2.9180	A
-2.3000	-2.7010	-2.5260	-2.6890	A
-2.2000	-2.4720	-2.3280	-2.4590	A
-2.1000	-2.2450	-2.1300	-2.2310	A
-2.0000	-2.0190	-1.9330	-2.0040	A
-1.9000	-1.7940	-1.7380	-1.7790	A
-1.8000	-1.5720	-1.5440	-1.5550	A
-1.7000	-1.3530	-1.3520	-1.3350	A
-1.6000	-1.1380	-1.1620	-1.1190	A
-1.5000	-0.9302	-0.9775	-0.9107	A
-1.4000	-0.7315	-0.7977	-0.7115	A
-1.3000	-0.5469	-0.6261	-0.5270	A
-1.2000	-0.3813	-0.4659	-0.3625	A
-1.1000	-0.2385	-0.3210	-0.2240	A
-1.0000	-0.1281	-0.1957	-0.1294	A
-0.9000	-70.5400	-99.1700	-89.4300	mA
-0.8000	-47.3200	-46.2500	-65.7900	mA
-0.7000	-30.4600	-25.8900	-44.8300	mA
-0.6000	-16.4200	-14.3600	-26.3200	mA
-0.5000	-6.2200	-6.2200	-11.6000	mA
-0.4000	-1.2320	-1.6750	-2.8860	mA
-0.3000	-0.1076	-0.2328	-0.3018	mA
-0.2000	-4.5180	-18.5600	-13.8700	μA
-0.1000	-0.1127	-1.0300	-0.3010	μA
0.0000	-6.6770	-66.9100	-13.2700	nA

Notes:

1. Typical conditions are 25°C, 3.3V.
2. Minimum conditions are 100°C, 3.0V.
3. Maximum conditions are 0°C, 3.45V.

Table 2: Virtex-II Pro FPGA Power Clamp Diode I-V Characteristics

External Pin Voltage	I (typ) ⁽¹⁾	I (min) ⁽²⁾	I (max) ⁽³⁾	Unit of Measure
3.3000	4.2620	3.4560	4.4610	A
3.2000	4.0700	3.3060	4.2590	A
3.1000	3.8770	3.1560	4.0570	A
3.0000	3.6850	3.0050	3.8550	A
2.9000	3.4930	2.8560	3.6530	A
2.8000	3.3010	2.7060	3.4510	A
2.7000	3.1090	2.5560	3.2490	A
2.6000	2.9170	2.4070	3.0470	A

Table 2: Virtex-II Pro FPGA Power Clamp Diode I-V Characteristics (Continued)

External Pin Voltage	I (typ) ⁽¹⁾	I (min) ⁽²⁾	I (max) ⁽³⁾	Unit of Measure
2.5000	2.7260	2.2580	2.8460	A
2.4000	2.5340	2.1090	2.6450	A
2.3000	2.3430	1.9600	2.4440	A
2.2000	2.1520	1.8120	2.2430	A
2.1000	1.9610	1.6650	2.0420	A
2.0000	1.7700	1.5170	1.8420	A
1.9000	1.5800	1.3710	1.6420	A
1.8000	1.3890	1.2250	1.4430	A
1.7000	1.2010	1.0800	1.2470	A
1.6000	1.0150	0.9373	1.0530	A
1.5000	0.8339	0.7954	0.8634	A
1.4000	0.6584	0.6558	0.6793	A
1.3000	0.4927	0.5195	0.5034	A
1.2000	0.3397	0.3884	0.3393	A
1.1000	0.2032	0.2656	0.1932	A
1.0000	94.8800	156.7000	87.4000	mA
0.9000	39.6900	73.0000	46.4600	mA
0.8000	23.3600	29.6200	31.4500	mA
0.7000	14.3400	15.0000	20.0800	mA
0.6000	7.3070	7.8690	10.7500	mA
0.5000	2.4360	3.1010	3.9780	mA
0.4000	0.3499	0.6618	0.6555	mA
0.3000	21.9300	70.4200	39.3900	μA
0.2000	0.8963	5.2470	1.7000	μA
0.1000	0.0760	0.5476	0.4264	μA
0.0000	0.0429	0.2878	0.3536	μA

Notes:

1. Typical conditions are 25°C, 3.3V.
2. Minimum conditions are 100°C, 3.0V.
3. Maximum conditions are 0°C, 3.45V.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/17/02	1.0	Initial Xilinx release.
02/06/03	1.1	Added “ PCI Compliance ” section. Added I/O standard suggestions for connecting to PCI bus.
04/14/03	1.2	Added references to Spartan-3 FPGA family.
01/09/04	1.3	Replaced “ PCI Compliance ” section with more detailed information. Added “ Appendix ”.
05/19/04	1.3.1	Removed statement about alternate solutions from “ Regulator Implementation ” section.
03/07/05	2.0	Updated application note to include Virtex-4 devices.
03/09/05	2.0.1	Corrected author’s name.
05/03/07	2.1	<ul style="list-style-type: none"> Expanded to include Virtex-4, Virtex-5, Spartan-3, and Spartan-3E devices. Modified information on PCI Compliance Specification requirement in “PCI Compliance” section. Restructured document headings, resized figures, and reformatted tables in Appendix.
07/09/07	3.0	<ul style="list-style-type: none"> Throughout: Removed all references to Spartan-3 Generation devices. Refer to XAPP457 for Spartan-3 Generation 3.3V information. Figure 2: Changed regulator output capacitor from 3.3 μF to 10 μF.
05/05/08	3.1	Figure 2, page 3 : Added a 1 μ F capacitor to pin 8 of the regulator.
05/12/08	3.1.1	Repagination.

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