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Interfacing QDR II SRAM Devices with Virtex-6 FPGAs

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Summary

With an increasing need for lower latency and higher operating frequencies, memory interface IP is becoming more complex and needs to be tailored based on a number of factors such as latency, burst length, interface width, and operating frequency. The Xilinx® Memory Interface Generator (MIG) tool enables the creation of a large variety of memory interfaces for devices such as the Virtex®-6 FPGA. However, in the Virtex-6 FPGA, QDR II SRAM is not one of the options available by default. Instead, the focus has been on the QDR II+ technology using four-word burst access mode.

This application note presents a Verilog reference design that has been simulated, synthesized, and verified on hardware using Virtex-6 FPGAs and QDR II SRAM two-word burst devices.

Design Characteristics

Table 1 shows the salient features of the reference design.

Table 1: **Reference Design Characteristics**

Parameter	Description
RTL language	Verilog
QDR SRAM part reference number	Cypress Semiconductor CY7C1412BV18, Samsung Electronics K7R321882C
Reference design LUT utilization for 18-bit read/write	1,247
Slice register utilization for 18-bit read/write	1,866
Synthesis	XST 12.2
Simulation	ISim 12.2
Implementation tools	ISE® Design Suite 12.2
MIG software version	MIG 3.4
Total number of I/O blocks (IOBs) for complete reference design	72 (data, address, control, clock, and test signals)
XPower Analyzer power estimation	1.04W dynamic power

Design Description

The reference design is based on a MIG 3.4 QDR II+ four-word burst design. The essential differences between QDR II SRAM devices and QDR II+ SRAM devices are:

- Address bus: The QDR II SRAM two-word burst design uses double the clock rate for the address bus.
- QVLD signal: The QDR II SRAM specification does not call for a data valid signal.

The code base was designed to be adaptable. Many parameters can be passed from the top-level RTL module to the levels lower down in the hierarchy. The control layers of the design

operate mostly at half the rate of the memory interface, and the ISERDES and OSERDES are used to interface to the external memory components.

Adaptation of the Design

Preparing the design involves these general tasks:

- Generate the most appropriate combination of QDR II+ interfaces using the MIG tool.
- Modify the parameter values to adapt to the specifications of the QDR standard.
- Set up the simulation environment using the Cypress and Samsung memory models.
- Modify the state machine to operate properly for two-word burst.
- Modify the testbench to verify correct operation for two-word burst.
- Implement two modules to connect the testbench to the user interface at the external memory clock frequency.
- Place and route the design and close timing.
- Create a user interface front end running at the full interface frequency for legacy. purposes, or for designs that need to feed one read and one write command per cycle.
- Debug and verify proper functionality through functional simulation.

The result of this process is presented in the QDR II SRAM Virtex-6 FPGA reference design provided with this application note. Most of the description of the physical and control layers is based on the *Memory Interface Solutions User Guide* [Ref 1].

Design Architecture

The QDR reference design includes a user interface by which simultaneous read and write commands can be fed in at the interface rate. Because the MIG testbench test fixture has been kept in the reference design, a module that speeds up twice the signals at half the rate has also been included. Figure 1 shows the overall data and address flow across the design, along with data width and clock rates.

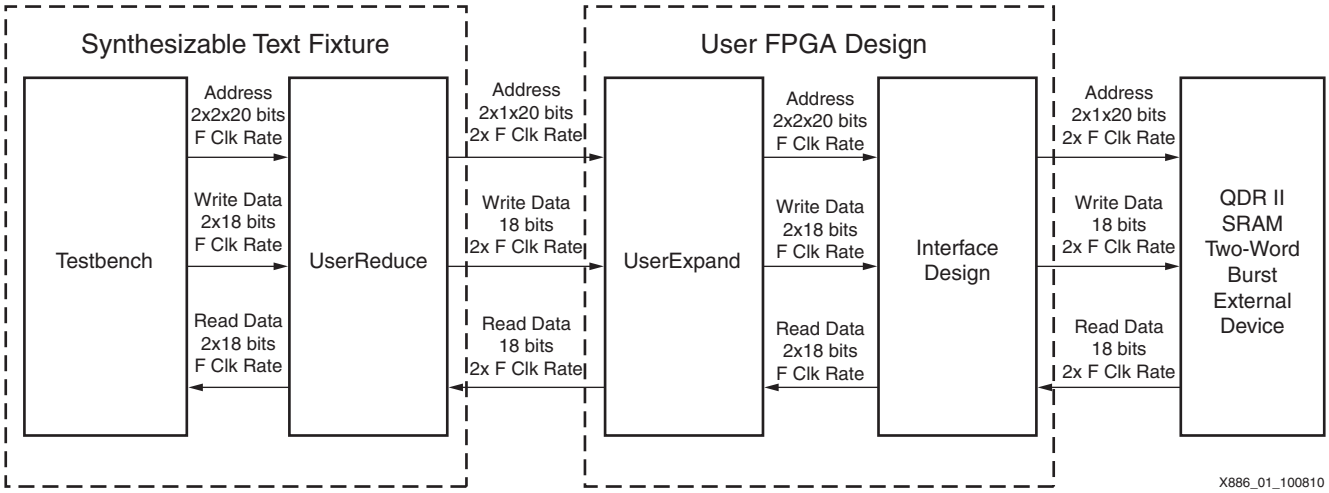

Figure 1: **Data and Address Flow across the Design**

Two new modules have been added from the MIG 3.4 reference design:

- `UserExpand.v`: This module takes in write data, and address and command signals at the external interface rate and expand the inputs to twice the size at half the external memory interface frequency to be processed in the physical layer of the interface. The `UserExpand.v` module provides valid data strobe and read data at the external memory interface frequency. It is meant to be used at the user interface to connect to the user design. This module is not necessary when the signals provided at the user interface are half the external memory interface frequency.

- `UserReduce.v`: This module takes in a double set of read and write address and data signals at half the external memory interface frequency. The `UserReduce.v` module converts them to one set of signals at the external memory interface frequency, and expands the valid data and read data. This module is meant to be used when using the reference design testbench as provided.

Figure 2 presents the block diagram of the modified reference design. The main difference from the original reference design is the addition of a module connecting to the user interface such that command and data signals are provided at the external memory rate. Another module has been added to adapt the MIG synthesizable testbench running at half the frequency of the memory interface to the new full rate interface. These two models can by bypassed if the interface is used at half the external memory frequency.

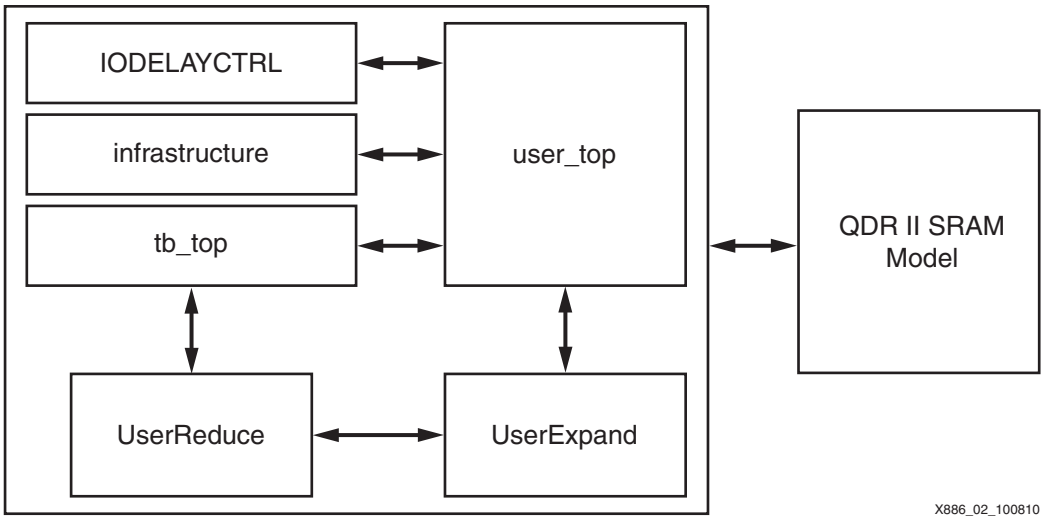

Figure 2: **Reference Design Block Diagram**

The entire source code for the design is available and should be referred to for details on all input and output signals for the modules. Figure 3 shows the file structure of the reference design.

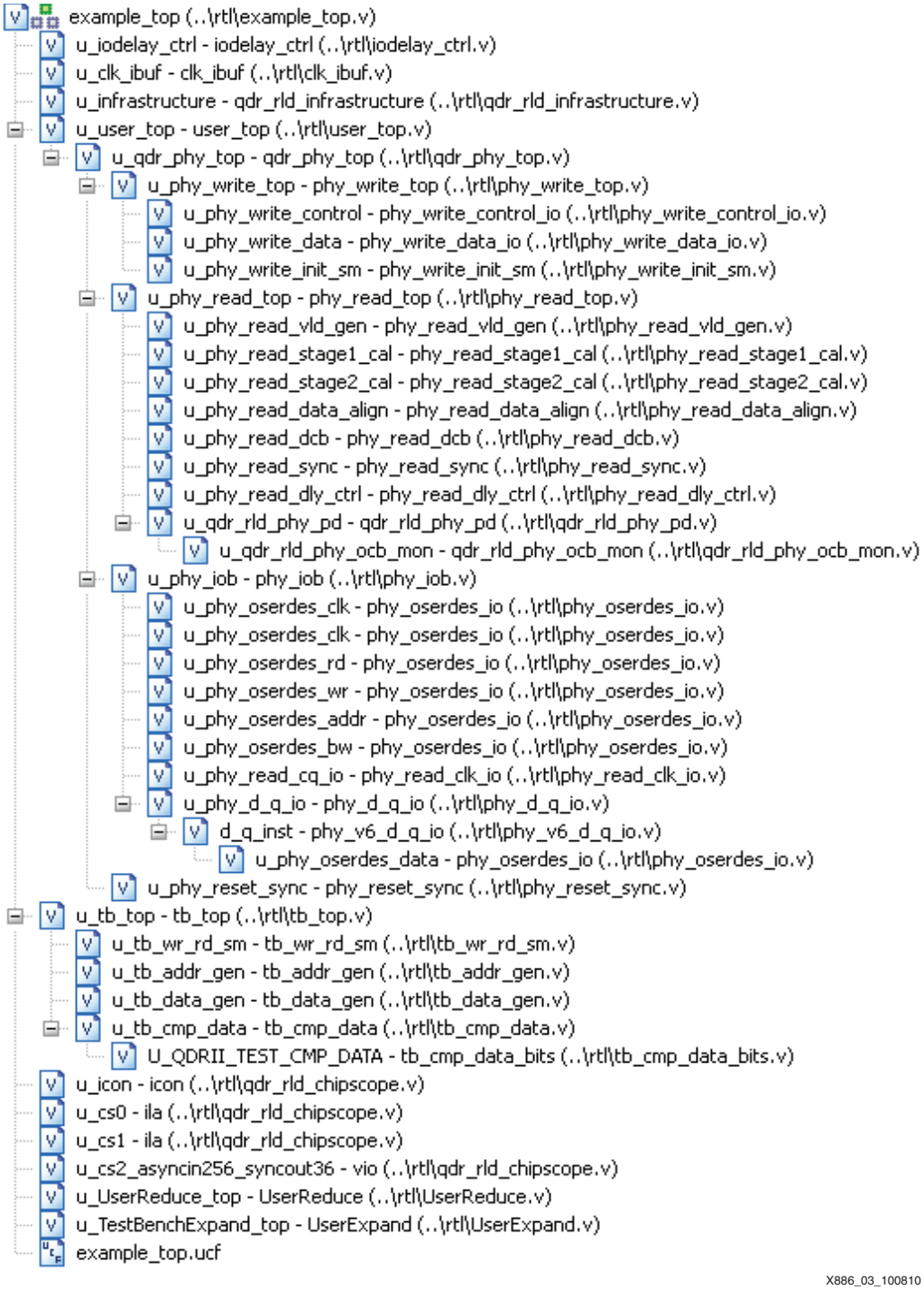

Figure 3: **Hierarchical List of Modules in Reference Design**

The following code lists the parameters used to implement the QDR II SRAM two-word burst design.

```
REFCLK_FREQ          = 200,      // Iodelay Clock Frequency
IODELAY_GRP          = "IODELAY_MIG",
                                 // It is associated to a set of IODELAYs with
                                 // an IDELAYCTRL that have same IODELAY CONTROLLER
                                 // clock frequency.
CLKFBOUT_MULT_F      = 8,            // write PLL VCO multiplier
CLKOUT_DIVIDE        = 4,            // VCO output divisor for fast (memory) clocks
DIVCLK_DIVIDE        = 2,                    // write PLL VCO divisor
CLK_PERIOD           = 8000,                 // Double the Memory Clk Period (in ps)
DEBUG_PORT           = "OFF",                // Enable debug port
CLK_STABLE           = 2048,                 // Cycles till CQ/CQ# is stable
ADDR_WIDTH           = 20,                   // Address Width
DATA_WIDTH           = 18,                   // Data Width
BW_WIDTH             = DATA_WIDTH/9,         // Byte Write Width
BURST_LEN            = 2,                    // Burst Length
NUM_DEVICES          = 1,                    // No. of Connected Memories
FIXED_LATENCY_MODE = 0,                      // Enable Fixed Latency
PHY_LATENCY          = 0,                    // Expected Latency
SIM_CAL_OPTION       = "NONE",               // Skip various calibration steps
MMCM_ADV_PS_WA       = "ON",                 // MMCM_ADV Phase Shift Work Around
                                             // Turn ON for hardware
SIM_INIT_OPTION      = "NONE",               // Simulation only. "NONE", "SIM_MODE"
PHASE_DETECT         = "OFF",                // Enable Phase detector
IBUF_LPWR_MODE       = "OFF",                // Input buffer low power mode
IODELAY_HP_MODE      = "ON",                 // IODELAY High Performance Mode
TCQ                  = 100,                  // Simulation Register Delay

INPUT_CLK_TYPE       = "DIFFERENTIAL",       // # of clock type
RST_ACT_LOW          = 1                     // Active Low Reset
```

Figure 4 shows the functional simulation waveforms with the code and modified synthesizable testbench. The figure shows the latency between a write and a read performed at different locations.

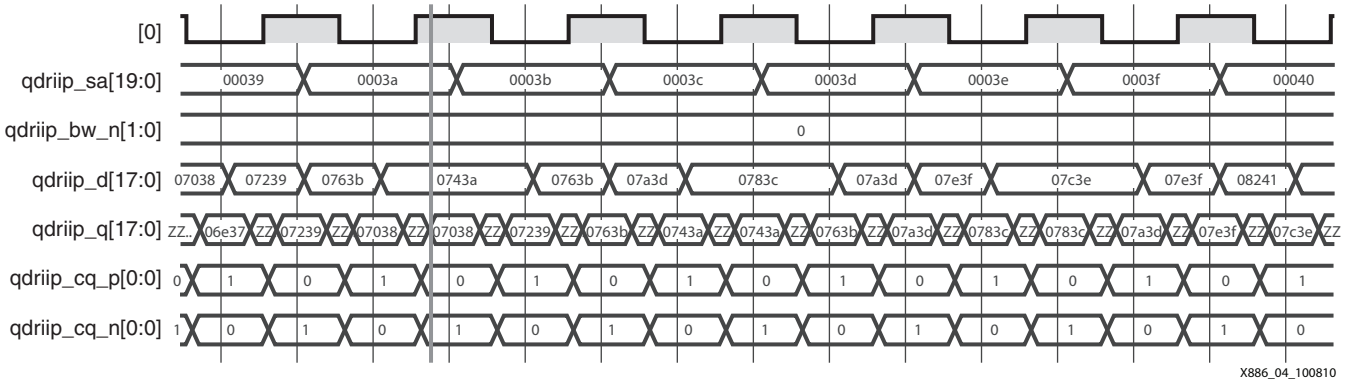

Figure 4: **Sample Waveforms of Continuous Read and Write Operations**

Reference Design

The reference design files for this application note can be downloaded at:

https://secure.xilinx.com/webreg/clickthrough.do?cid=154544

Note: Xilinx cannot include the memory models of memory vendors with the reference design because users must accept the memory vendors' license agreements. Functional HDL memory device models for Samsung and Cypress parts can be obtained through the memory vendors' respective websites. The memory model should be added to the project and compiled to be able to run the functional simulation. Refer to the `readme.txt` file in the reference design ZIP file for examples.

The reference design checklist is shown in Table 2.

Table 2: **Reference Design Checklist**

Parameter	Description
General	
Developer Name	Olivier Despaux
Target Device	Virtex-6 FPGA
Source Code Provided?	Yes
Source Code Format	Verilog
Design Uses Code or IP from Existing Reference Design, Application Note, 3rd party, or CORE Generator™ Software?	Yes
Simulation	
Functional Simulation Performed?	Yes
Timing Simulation Performed?	No
Testbench Provided for Functional and Timing Simulations?	Yes
Testbench Format	Verilog
Simulator Software and Version	ModelSim SE 6.6b and ISim 12.2
Spice/IBIS simulations	No
Implementation	
Synthesis Simulator Software and Version	XST 12.2
Implementation Software Tools and Version	ISE 12.2
Static Timing Analysis Performed?	Yes, same as MIG 3.4
Hardware Verification	
Hardware Verified?	Yes
Hardware Platform Used for Verification	ML662 memory interface development board

References

1. UG086, *Memory Interface Solutions User Guide*.
2. UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide*
3. DS186, *Virtex-6 FPGA Memory Interface Solutions Data Sheet*.
4. 36-Mbit QDR II SRAM 2-Word Burst Architecture, Cypress Semiconductor http://www.cypress.com/?docID=18650.
5. 36Mb QDRII SRAM Specification, Samsung Electronics http://www.samsung.com/global/system/business/semiconductor/product/2007/6/11/HighSpeedSRAM/QDRI_II/36Mbit/K7R321882C/ds_k7r32xx82c_rev11.pdf.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
12/02/10	1.0	Initial Xilinx release.

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