

Introduction

Thank you for participating in the Virtex®-7 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades	Temperature
Virtex-7	XC7VX485T CES9937	0	All	-1, -2	0 to 85°C

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

External Memory Interfaces

Dual Rank for DDR3 and DDR2

Dual rank topologies are not supported for DDR3 and DDR2 SDRAM interfaces. This applies to dual rank DIMM modules and dual rank component topologies, including those implemented using twin or dual die configurations in a single package.

Phaser Block Divide by Two Mode for DDR3 and DDR2

The Phaser block "divide by two" mode used to implement DDR3 and DDR2 external memory interfaces at frequencies from 303–399 MHz is not operational. The Phaser block must be used in 1:1 mode, which restricts the minimum supported DDR3 and DDR2 memory clock frequency to 400 MHz (800 Mb/s DDR).

Work-around

Select a Memory Clock frequency of 400 MHz (DDR3 or DDR2) or higher (DDR3 only) in the Memory Interface Generator (MIG) tool to ensure that the Phaser block is set to 1:1 mode.

XADC

Integral Nonlinearity

The XADC has a four LSB (~1 mV) integral nonlinearity (INL) error versus the data sheet specifications ([DS183](#), *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics*, v1.3) of two LSBs.

XADC On-chip Reference Variation

The XADC on-chip reference source can exceed the [DS183](#), *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* data sheet specification of $1.25V \pm 1\%$ by an additional 0.5%. See [Answer Record 44971](#) for more information on the impact to XADC measurements when the on-chip reference source is used.

GTX Transceivers

Out-of-Band Signaling

The GTX transceiver circuitry for out-of-band (OOB) signaling is always enabled.

GTX Line Rate

The GTX transceiver operation is limited to a maximum of 6.6 Gb/s.

QPLL Frequency Range

The supported QPLL frequency range is 5.93–6.6 GHz.

TXOUTCLK and RXOUTCLK Ports

The GTX transceiver TXOUTCLK and RXOUTCLK ports can exhibit loss of edges or excessive jitter when used simultaneously within a GTX channel and with other channels in a transceiver Quad.

The following rules must be followed for proper operation of TXOUTCLK and RXOUTCLK:

- Use either TXOUTCLK or RXOUTCLK within any GTX channel, not both.
- Use either TXOUTCLK of GTX0 or RXOUTCLK of GTX1, not both.
- Use the reference clock directly from IBUFDS_GTXE2 to drive the fabric logic and GTX user clocks when necessary ([TX/RX]USRCLK, [TX/RX]USRCLK2).

Set RXOUTCLKSEL = 3'b000 when RXOUTCLK is not used. Set TXOUTCLKSEL = 3'b000 when TXOUTCLK is not used.

See [Answer Record 43244](#) for more information.

QPLL Use Mode

The QPLL can lose lock if reset at one temperature extreme and operated at the other.

Work-around

See [Answer Record 43244](#) for the user design work-around.

Receiver Link Margin

The receiver can have a reduction in jitter tolerance when used in full-rate mode (RXOUT_DIV == 1).

Work-around

See [Answer Record 43244](#) for attribute updates and equalization selection.

CPLL Jitter

The GTX CPLL when operated at 3.1 GHz, or above, can exhibit higher jitter when MGTAVTT is higher than nominal.

Transmit Electrical Idle

The transmitter common mode voltage is higher than expected when TX electrical idle is enabled. The electrical idle detection in the receiver is not impacted when links are AC coupled.

Receiver Detection for PCIe

The Receiver Detection feature used for PCIe® applications is not supported.

Work-around

Set the following attributes to force the transmitter to always detect a receiver:

- TX_RXDETECT_REF = 3'b000
- RX_CM_SEL = 2'b11
- (PMA_RSV2[4], RX_CM_TRIM[2:0]) = 4'b1010

PCIe ASPM Support

ASPM L0s is not supported for Gen 2 (5 Gb/s) line rate.

Work-around

Set the following attributes on the Integrated Block for PCI Express to disable ASPM L0s:

- LINK_CAP_ASPM_OPTIONALITY = TRUE
- LINK_CAP_ASPM_SUPPORT = 0

See [Answer Record 43243](#) for additional details.

IEEE Std 1149.6 for GTX Transceivers

In the devices listed in [Table 1](#), IEEE Std 1149.6 (ACJTAG) boundary-scan test commands EXTEST_PULSE and EXTEST_TRAIN are not supported.

SelectIO Resources

Internal Weak Pull-Ups/Pull-Downs for High-Range I/O Bank0

The internal weak pull-ups/pull-downs for the high-range (HR) I/O configuration bank 0 will not achieve valid logic-1 and logic-0 states for 1.8V and lower V_{CCO_0} . External resistors should be used for V_{CCO_0} of 1.8V and lower.

Power

Static Current

The devices listed in [Table 1](#) can exhibit up to 50% higher static current on all supplies compared to the static current reported in XPE 13.3. Also, up to an additional 95 mA is consumed by the MGTAVCC for each powered and uninstantiated transceiver Quad.

Power-On/Off Requirement

For V_{CCO_0} voltages of 3.3V in the high-range (HR) I/O configuration bank 0, the following requirements must be followed:

- When V_{CCINT} is less than 0.7V, V_{CCO_0} must not exceed 2.625V for longer than 800 ms with $T_j = 85^\circ\text{C}$ for each power-on/off cycle to maintain device reliability levels.
 - This time can be allocated in any percentage between the power-on and power-off ramps.
 - This time is based on 240,000 power cycles with nominal V_{CCO_0} of 3.3V or 36,500 power cycles with a worst case V_{CCO_0} of 3.465V.

Design Software Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.02 (or later) of Xilinx® ISE Design Suite 13.3 available at <http://www.xilinx.com/support/download/>.
- See Virtex-7 FPGA [Answer Record 43423](#) for known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Designs targeting DDR3 data rates above 800 Mb/s must include an external V_{REF} . For further details, refer to [Answer Record 42036](#).

Traceability

The XC7VX485T devices listed in [Table 1](#) are marked as shown in [Figure 1](#).

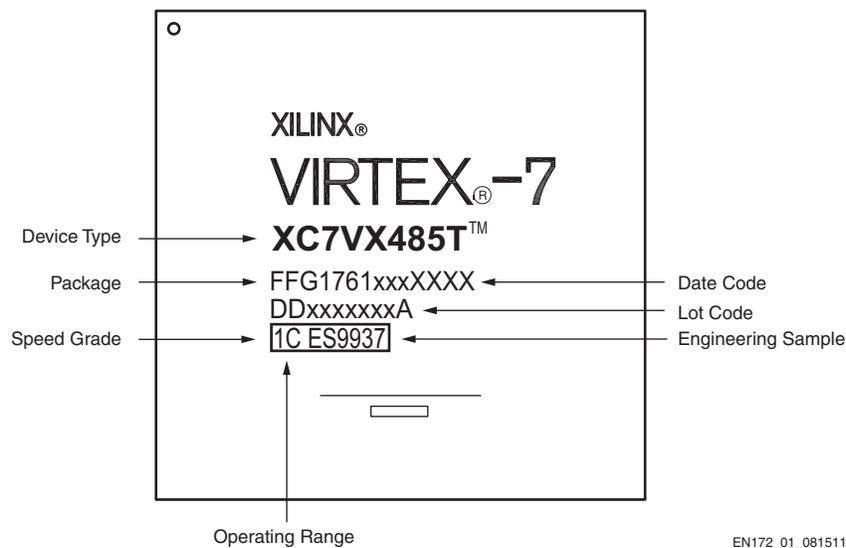


Figure 1: Example Device Top Mark

EN172_01_081511

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
08/25/11	1.0	Initial Xilinx release.
10/18/11	1.1	Removed DDR3 Operating Conditions; fixed in the Virtex-7 FPGA DDR3 memory interface IP generated by MIG in ISE 13.2 software. Updated Static Current . Updated Power-On/Off Sequence; new title is Power-On/Off Requirement and contains updated text.
11/08/11	1.2	Removed <i>XADC Auxiliary Analog Input Channels</i> errata; fixed pinout in UG475, 7 Series FPGAs Packaging and Pinout User Guide (v1.3) , and ISE Design Suite 13.3. Updated Design Software Requirements section.
12/01/11	1.3	Added XADC On-chip Reference Variation and updated Power-On/Off Requirement .
01/24/12	1.4	Added Dual Rank for DDR3 and DDR2 . Updated Phaser Block Divide by Two Mode for DDR3 and DDR2 , and XADC On-chip Reference Variation . Added Out-of-Band Signaling .

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

Engineering Sample Disclaimer

ENGINEERING SAMPLE (ES) DEVICES ARE MADE AVAILABLE SOLELY FOR PURPOSES OF RESEARCH, DEVELOPMENT AND PROTOTYPING. ALL ES DEVICES ARE SOLD "AS-IS" WITH NO WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED. XILINX DOES NOT WARRANT THAT ES DEVICES ARE FULLY VERIFIED, TESTED, OR WILL OPERATE IN ACCORDANCE WITH DATA SHEET SPECIFICATIONS. XILINX DISCLAIMS ANY OBLIGATIONS FOR TECHNICAL SUPPORT AND BUG FIXES. XILINX SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION DIRECT, INDIRECT, INCIDENTAL, SPECIAL, RELIANCE, OR CONSEQUENTIAL DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF ES DEVICES IN ANY MANNER WHATSOEVER, EVEN IF XILINX HAS BEEN ADVISED OF THE POSSIBILITY THEREOF. XILINX MAKES NO REPRESENTATION THAT ES DEVICES PROVIDE ANY PARTICULAR FUNCTIONALITY, OR THAT ES DEVICES WILL MEET THE REQUIREMENTS OF A PARTICULAR USER APPLICATION. XILINX DOES NOT WARRANT THAT ES DEVICES ARE ERROR-FREE, NOR DOES XILINX MAKE ANY OTHER REPRESENTATIONS OR WARRANTIES, WHETHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, INCLUDING, WITHOUT LIMITATION, IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. THE FOREGOING STATES THE ENTIRE LIABILITY OF XILINX WITH RESPECT TO ES DEVICES.