

Introduction

Thank you for participating in the Virtex®-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades	Temperature
Virtex-7	XC7VX485T CES9900	2	All	-2	0°C to 100°C

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

XADC

For improved linearity, a new BitGen option (XADCEnhancedLinearity = ON/OFF) must be set to ON (see [Answer Record 45781](#) for more information). The specifications enhanced by this BitGen option are INL, THD, and SNR (see [Table 2](#)). By default this BitGen option is set to OFF. Existing XADC designs operate with the OFF setting.

[Table 2](#) also lists errata for XADC DC accuracy specifications of Offset Error, Gain Error, Channel Matching, and On-Chip Reference Variation.

Table 2: XADC Errata

Parameter	XADC Errata		DS183 (v1.2), Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics Specifications
	XADCEnhancedLinearity = ON	XADCEnhancedLinearity = OFF	
Integral Nonlinearity (INL)	±3 LSBs Max	±5 LSBs Max	±2 LSBs Max
Total Harmonic Distortion (THD)	70 dB Typ	65 dB Typ	75 dB Min
Signal to Noise Ratio (SNR)	60 dB Min	60 dB Typ	60 dB Min
Channel Matching	11 LSBs Max	11 LSBs Max	10 LSBs Max
Offset Error	±6 LSBs Max	±6 LSBs Max	±4 LSBs Max
Gain Error	±0.5% Max	±0.5% Max	±0.4% Max
On-Chip Reference Variation ⁽¹⁾	1.25V ±1.5% Max	1.25V ±1.5% Max	1.25V ±1.0% Max

Notes:

- See [Answer Record 44971](#) for more information on the impact to XADC measurements when the on-chip reference source is used.

[DS183](#), *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* specifications will be updated to reflect the final device characterization.

GTX Transceivers

Line Rate Support

The GTX transceiver is limited to -1 speed grade specifications in the DS183, *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics Specifications*.

Out-of-Band Signaling

The GTX transceiver circuitry for out-of-band (OOB) signaling is always enabled.

CPLL Power Down

The GTX transceiver CPLL can become inoperative if conditions (1) and (2) persist for more than 8,000 hours:

1. Power has been applied to MGTAVCC and MGTAVTT.
2. The device is in one of the following states:
 - a. The FPGA is not configured.
 - b. The FPGA is configured, but the transceiver is uninstantiated.
 - c. The transceiver is instantiated, but the CPLL is held in power-down state.

When the QPLL is being used, enabling each CPLL will consume up to 30 mA on the MGTAVTT supply and 20 mA on MGTAVCC. See [Answer Record 45360](#) for more details.

GTX Transceiver Power-Up/Power-Down

The GTX transceiver can become inoperative if MGTAVTT is within its recommended operating range and MGTAVCC is at a voltage less than 0.4V for more than 10,000 cumulative hours. An additional 100 mA per transceiver is drawn when MGTAVTT is within its recommended operating range and MGTAVCC is at a voltage less than 0.4V.

IEEE Std 1149.6 for GTX Transceivers

In the devices listed in [Table 1](#), IEEE Std 1149.6 (ACJTAG) boundary-scan test commands EXTEST_PULSE and EXTEST_TRAIN are not supported.

Power

Static Power

All power supplies can exhibit up to 25% higher static current compared to the static current reported in XPE.

Also, up to an additional 30 mA per used transceiver, and up to an additional 50 mA per powered transceiver quad can be consumed by the MGTAVCC supply. And, up to an additional 50 mA per powered transceiver quad can be consumed by the MGTAVTT supply.

Design Software Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.03 (or later) of Xilinx® ISE® Design Suite 13.4 (or later) available at <http://www.xilinx.com/support/download/>.
- For GTX transceiver attribute updates, refer to [Answer Record 45360](#).
- See Virtex-7 FPGA [Answer Record 46345](#) for known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Physical Interface Rate for Memory Interfaces

Designs targeting DDR3 data rates above 800 Mb/s should include an external V_{REF} . For further details, refer to [Answer Record 42036](#).

Hardware Validation for Memory Interfaces

The memory interfaces listed in [Table 3](#) have been validated in hardware across the operating conditions for these devices at the time of publication. See [Answer Record 46521](#) for the latest hardware validation information.

Table 3: Hardware Validated Memory Interfaces

Type	Condition	Bank
DDR3	DIMM Single Rank	HP
	Component Single Rank	HP
	DIMM Single Rank	HR
QDRII+	Component Single Rank	HP

Traceability

Figure 1 shows an example device top mark for the devices listed in [Table 1](#).

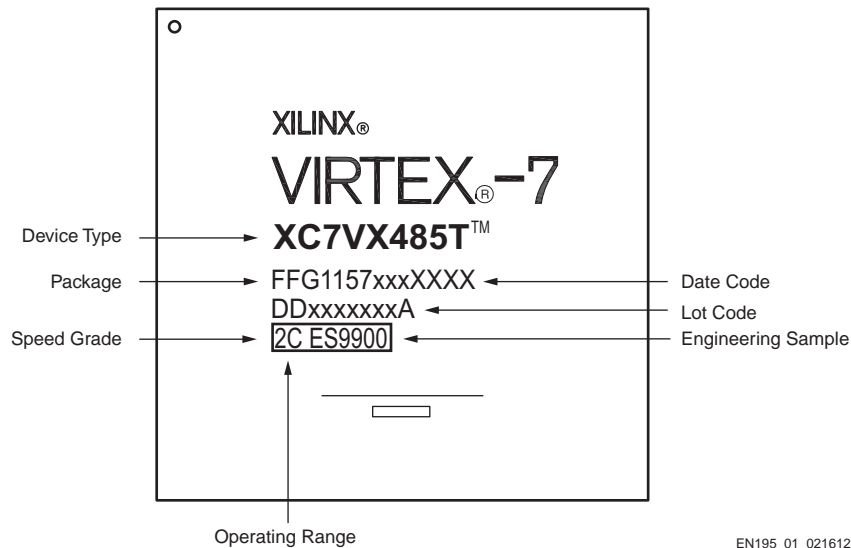


Figure 1: Example Device Top Mark

EN195_01_021612

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/28/12	1.0	Initial Xilinx release.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

Engineering Sample Disclaimer

ENGINEERING SAMPLE (ES) DEVICES ARE MADE AVAILABLE SOLELY FOR PURPOSES OF RESEARCH, DEVELOPMENT AND PROTOTYPING. ALL ES DEVICES ARE SOLD "AS-IS" WITH NO WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED. XILINX DOES NOT WARRANT THAT ES DEVICES ARE FULLY VERIFIED, TESTED, OR WILL OPERATE IN ACCORDANCE WITH DATA SHEET SPECIFICATIONS. XILINX DISCLAIMS ANY OBLIGATIONS FOR TECHNICAL SUPPORT AND BUG FIXES. XILINX SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION DIRECT, INDIRECT, INCIDENTAL, SPECIAL, RELIANCE, OR CONSEQUENTIAL DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF ES DEVICES IN ANY MANNER WHATSOEVER, EVEN IF XILINX HAS BEEN ADVISED OF THE POSSIBILITY THEREOF. XILINX MAKES NO REPRESENTATION THAT ES DEVICES PROVIDE ANY PARTICULAR FUNCTIONALITY, OR THAT ES DEVICES WILL MEET THE REQUIREMENTS OF A PARTICULAR USER APPLICATION. XILINX DOES NOT WARRANT THAT ES DEVICES ARE ERROR-FREE, NOR DOES XILINX MAKE ANY OTHER REPRESENTATIONS OR WARRANTIES, WHETHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, INCLUDING, WITHOUT LIMITATION, IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. THE FOREGOING STATES THE ENTIRE LIABILITY OF XILINX WITH RESPECT TO ES DEVICES.