Virtex-7 FPGA XC7VX1140T CES9937 Errata

EN211 (v1.0) July 20, 2012 **Errata Notification**

Introduction

Thank you for participating in the Virtex®-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades
Virtex-7	XC7VX1140T CES9937	0	All	-1, -2

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

GTH Transceivers

GTH Transceiver Power-On/Power-Off

The recommended power-on sequence is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ or $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$ to achieve minimum current draw. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If the recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down:

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 400 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3* $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3* T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

If the recommended sequence is followed, while $V_{MGTAVCC}$ is powered within its recommended operating range and $V_{MGTAVTT}$ is below 0.7V, an additional 70 mA per transceiver is drawn from $V_{MGTAVCC}$.

Depending on the number of transceivers used, this extra current can be greater than the consumption reported in XPE.

Refer to Answer Record 47443 for more information.

GTH Transceiver Eye Scan

To use the GTH receiver eye scan, RX_DATA_WIDTH must be set to 16, 32, or 64. Refer to Answer Record 47128 for more information.

GTH Transceiver Link Margin Reduction

For GTH transceiver line rates up to 8.5 Gb/s, there can be up to a 5% increase in transmitter output jitter and up to a 5% decrease in receiver input jitter tolerance when multiple channels are used.

For GTH transceiver line rates higher than 8.5 Gb/s, there can be up to a 10% increase in transmitter output jitter and up to a 10% decrease in receiver input jitter tolerance when multiple channels are used.

See Answer Record 47128 for additional information.

RXOUTCLK Port

For GTH transceiver line rates higher than 8.5 Gb/s, the GTH transceiver RXOUTCLK port, when configured to use the RXOUTCLKPCS or RXOUTCLKPMA path, can exhibit a phase jump of up to 2 UI of the line rate. In buffer bypass mode, the RXOUTCLK port cannot be used. For buffer use mode, see Answer Record 47128 for additional information.

$V_{MGTAVCC}$ Voltage Requirement

For GTH transceiver line rates higher than 10.3 Gb/s, $V_{MGTAVCC}$ must be 1.05V ± 30 mV.

PCIe

Virtual Channel Capability

The Virtual Channel Capability is always enabled in Configuration Space when the Secondary PCI Express® Capability is enabled.

Virtual Channel TC/VC Map

The Virtual Channel Resource Control register TC/VC Map is incorrectly reset to `8'h01` instead of the PCIe Base Specification 3.0 value of `8'hFF`.

Loopback Exit

Reset of the LTSSM state machine is required to exit Loopback.Active state in loopback slave mode at Gen3 link speed.

Power Budgeting Capability

The Power Budgeting Capability is not supported.

Resizable BAR

The optional PCIe Resizable BAR (RBAR) capability is not supported through configuration. The RBAR feature can be initiated after the FPGA has been configured.

End-to-End CRC

When End-to-End CRC (ECRC) is used with multiple functions (PF0 and PF1 enabled), then ECRC must be enabled for either both functions or neither. It cannot be enabled independently on a per function basis. If only PF0 is used, then ECRC can be enabled or disabled as required.

TLP Processing Hints

The TLP Processing Hints (TPH) Completer is not supported.

D1 Power State

The D1 lower power device state is not supported.

Root Port

Root Port mode is pending validation.

AER Header Log Overflow

For the Virtual Function Configuration Space, the optional AER Correctable Error Status register Header Log Overflow Status bit is not supported.

Function Level Reset

Function Level Reset (FLR) of SR-IOV Physical Functions is not supported. The ARI Capable Hierarchy bit in the Physical Function SR-IOV Control register is reset by a Function Level Reset of the Physical Function.

Configuration

Configuration Fallback

The fallback feature is not supported with the 32-bit addressing option during master SPI mode configuration.

This issue will not be fixed in silicon.

Power

Static Power

All power supplies can exhibit up to 50% higher static current compared to the static current reported in the Xilinx Power Estimator (XPE) 14.1. Also, up to an additional 50 mA per powered transceiver Quad can be consumed by the $V_{MGTAVCC}$ supply.

Packaging

Package Coplanarity

The package coplanarity (mechanical drawing symbol aaa) tolerance can be up to 0.30 mm (12 mils). Follow the guidelines in XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages* to ensure an optimal solder reflow profile.

Package Assembly

Bake units for 4 hours at 125°C before assembly. Within 30 minutes of taking the units from the bake oven, assemble them on the final system board. Failure to follow this baking procedure can result in device damage during assembly.

Design Tool Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.04 (or later) of Xilinx® Vivado™ Design Suite 2012.1 Device Pack (or later) available at http://www.xilinx.com/support/download/.
- For GTH transceiver attribute updates, refer to Answer Record 47128.
- See Virtex-7 FPGA Answer Record 47476 for the most current known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Hardware Validation for Memory Interfaces

The memory interfaces listed in Table 2 have been validated in hardware across the operating conditions for these devices at the time of publication. See Answer Record 46521 for the latest hardware validation information.

Table 2: **Hardware Validated Memory Interfaces**

Type	Condition	Bank
DDR3	DIMM and Component Single Rank	HP
QDRII+	Component Single Rank	HP
RLDRAMII	Component Single Rank	HP
DDR2	DIMM and Component Single Rank	HP

Traceability

Figure 1 shows an example device top mark for the devices listed in Table 1.

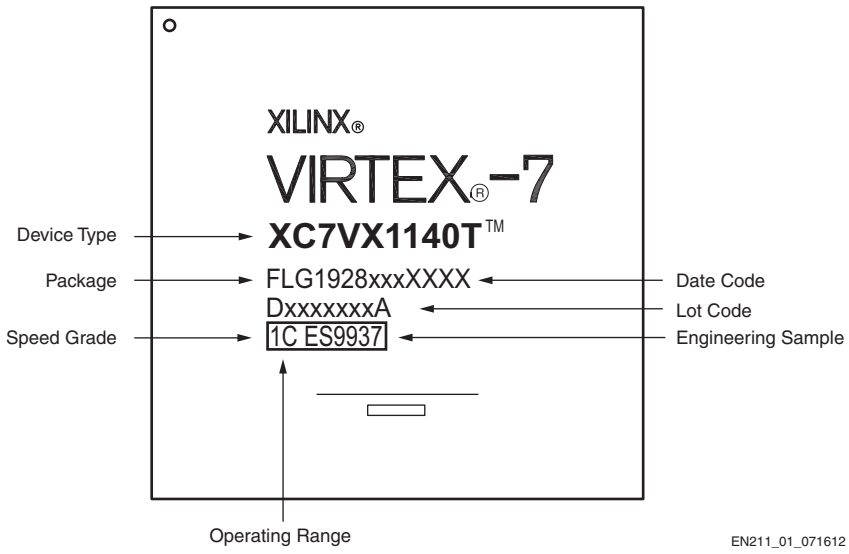

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact/index.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/20/12	1.0	Initial Xilinx release.

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