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SPI-4.2
Dynamic Phase Alignment

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This document explains the operation of the SPI-4.2 Dynamic Phase Alignment (DPA) Sink Core for Virtex®-4, Virtex-5, Virtex-6, and 7 series FPGAs and provides guidelines on how to use the SPI-4.2 DPA solution.

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DPA Operation Overview

The SPI-4.2 receiver interface consists of 18 DDR source-synchronous LVDS pairs: 16 data bits (RDat), 1 control bit (RCtl), and 1 clock (RDClk). Dynamic Phase Alignment logic is used to correctly capture source-synchronous data by shifting data relative to the clock to choose the optimal sampling point in the middle of the data eye and removing bit-to-bit skew on the data bus.

The SPI-4.2 Dynamic Phase Alignment core uses Advanced SelectIO™ technology built into every I/O of Virtex-4, Virtex-5, Virtex-6, and 7 series FPGAs. The ISERDES, available as part of the Advanced SelectIO technology, contains the IDELAY, SERDES, and BITSLIP sub-modules. The IDELAY sub-module has a 64-tap (Virtex-4 and Virtex-5 FPGAs) or 32-tap (Virtex-6 and 7 series FPGAs) delay line with a counter-controlled tap multiplexer. All the delay lines in a clock region are continuously calibrated by a servo system (IDELAYCTRL), using a 200 MHz user-provided reference clock. This reduces the effects of process, voltage, and temperature variations. The DPA logic uses the ISERDES and its sub-modules to deserialize, delay, and shift the data to align with the clock centered in the data eye.

The SPI-4.2 DPA logic supports different DPA features. The following features can be configured using CORE Generator™ software.

DPA Parameters

Master-Slave IDELAY Offset: This parameter determines the offset between the delay tap setting for the Master and Slave IDELAY. The default value is 2.

Alignment Test Interval: This parameter determines the number of samples taken per IDELAY tap value. The default value is 128.

DPA Clock Adjustment

Enable DPA Clock Adjustment: Enabling this option causes the DPA logic to adjust the clock delay to reduce the effects of IDELAY tap pattern jitter on system timing. This function is implemented by inserting an IDELAY on the RDClk signal. In Virtex-6 and 7 series FPGA designs, this feature is only available when RDClk clock distribution is regional.

Auto-Retry

Enable Auto-Retry: Enabling this option causes the automatic re-initiation of the DPA process (when it fails) until alignment is achieved.

Continuous Alignment

Enable Continuous Alignment: Enabling this option causes the DPA to continuously monitor alignment during operation, adapting the data sample point to system timing changes.

Generate Continuous Alignment Halt Pin: This option enables the dedicated input pin to be used to halt the continuous alignment process during operation.
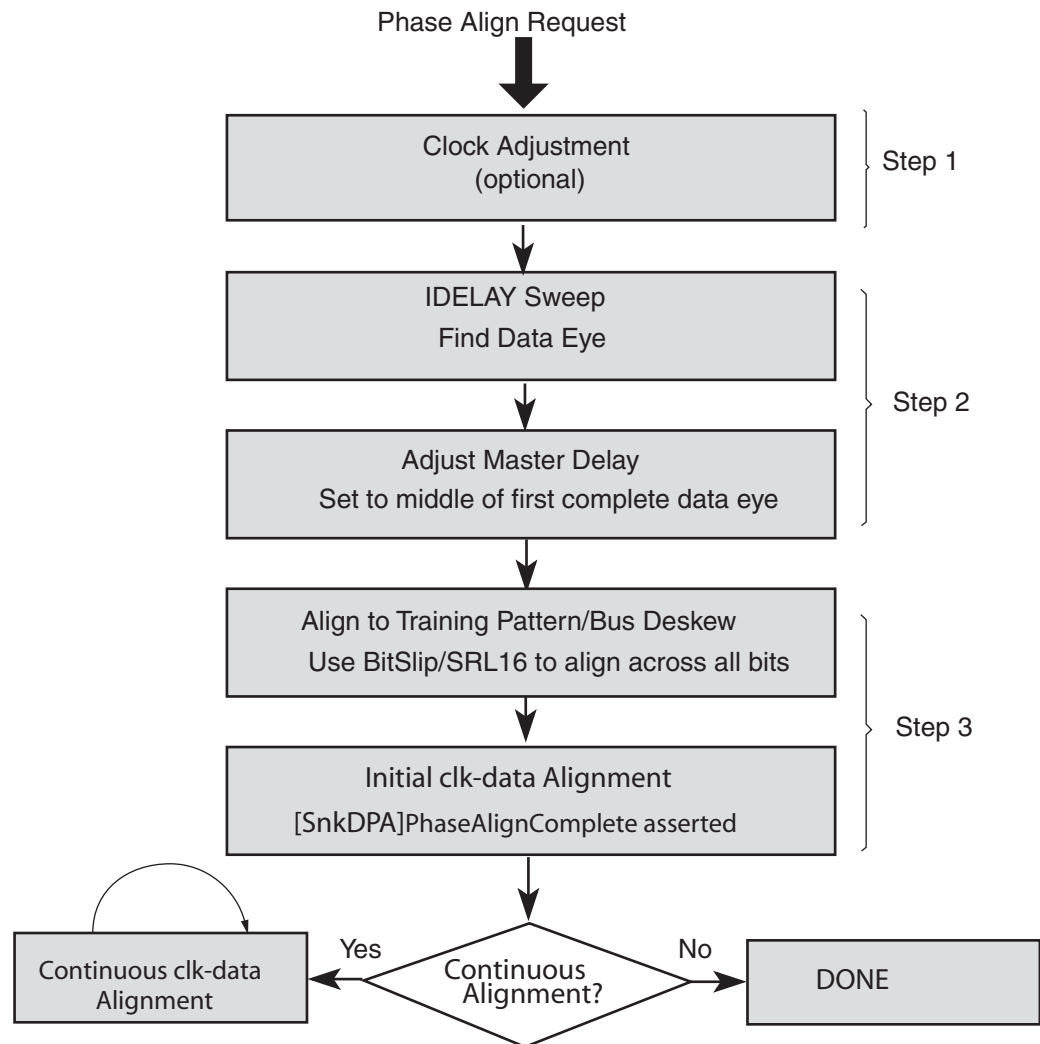
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Diagnostic Settings

Enable DPA Status Monitoring: This option enables the user to monitor the DPA logic using the `SnkBusErrStat` bus.

Report IDELAY on SPI-4.2 Bus Index: When enabled, the `SnkBusErrStat` reports the IDELAY setting during the initial alignment for the specified SPI-4.2 bus index. The valid index is 0 to 16, where 16 is the control bit.

Generate Advance DPA Diagnostic Ports: When enabled, this option allows the user to use advance DPA diagnostic ports to measure and capture the valid data window for each bit of the SPI-4.2 bus during operation.

Figure 1 is a high-level flow chart of the DPA operation.

Phase Align Request

Clock Adjustment
(optional)

Step 1

IDELAY Sweep
Find Data Eye

Adjust Master Delay
Set to middle of first complete data eye

Step 2

Align to Training Pattern/Bus Deskew
Use BitSlip/SRL16 to align across all bits

Initial clk-data Alignment
[SnkDPA]PhaseAlignComplete asserted

Step 3

Continuous clk-data
Alignment

Yes

Continuous
Alignment?

No

DONE

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Figure 1: **High-Level DPA Operation**

A high-to-low transition of the `[SnkDPA]PhaseAlignRequest` [1] signal places the DPA logic in a state waiting for a ready signal (internal to the core) from the IDELAYCTRLs, indicating that the IDELAY modules in the region are calibrated. When the ready signal from IDELAYCTRL is asserted, the DPA logic initiates the alignment process. Alignment operations are performed independently and simultaneously on every bit of the bus.

The alignment process involves four basic steps:

1. DPA clock adjustment (optional):

    Selection of this feature causes the DPA logic to perform a clock alignment phase prior to the initial bit alignment. This feature should only be selected if the traces for the data and control bits of the SPI-4.2 bus are approximately matched.

2. Initial bit alignment:

    The DPA logic performs bit alignment by shifting data relative to the clock to detect the optimal sampling point. Each bit of the SPI-4.2 bus is aligned to the clock independent of any other bit of the bus.

3. Word alignment:

    After bit alignment is completed for each bit, the DPA logic performs word alignment on the data bits to the SPI-4.2 training pattern to remove skew across data bits. The DPA logic indicates that it has achieved both bit and word alignment by asserting `[SnkDPA]PhaseAlignComplete`. If continuous alignment is not enabled, no further alignment is performed, even when additional training patterns are received.

4. Continuous alignment (optional):

    If the continuous alignment option is chosen, the continuous alignment process starts after `[SnkDPA]PhaseAlignComplete` is asserted. The DPA logic performs a constant non-disruptive monitoring of the ingress data samples and adjusts the data sampling point after the initial alignment is completed (`[SnkDPA]PhaseAlignComplete` is asserted). This process occurs continuously and independently on each bit of the bus and does not depend on the presence of SPI-4.2 training patterns. Any data pattern with transitions will exercise the monitoring feature.

Initial Bit Alignment

The initial bit alignment process uses offset sampling to detect data transitions and to determine the optimal data sampling point. Because the DPA logic detects the transition point of the data and uses this information to determine the optimal sampling point of the data eye, a valid SPI-4.2 training pattern must be sent when `[SnkDPA]PhaseAlignRequest` is asserted. The SPI-4.2 training pattern is a 20-bit training pattern with 10 zeros and 10 ones and is sent continuously by the transmitter in training mode. On the high-to-low transition of `[SnkDPA]PhaseAlignRequest`, the DPA logic also waits for the ready (internal to the core) from the IDELAYCTRLs before initiating the alignment process.

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1. `PhaseAlignRequest` is the signal name in SPI-4.2 v10.x and earlier. `SnkDPAPhaseAlignRequest` is the signal name in SPI-4.2 v11.x and later.

The DPA logic uses two ISERDES modules for each data bit. Figure 2 shows the basic DPA logic. The Master-Slave IDELAY offset parameter determines the difference in tap delay (each tap delay = 78 ps) between the two IDELAYs. During the alignment process, the DPA logic tests each of the possible IDELAY tap settings. Sweeping all the potential sample points allows the DPA logic to determine where the data eye or data transitions are located.
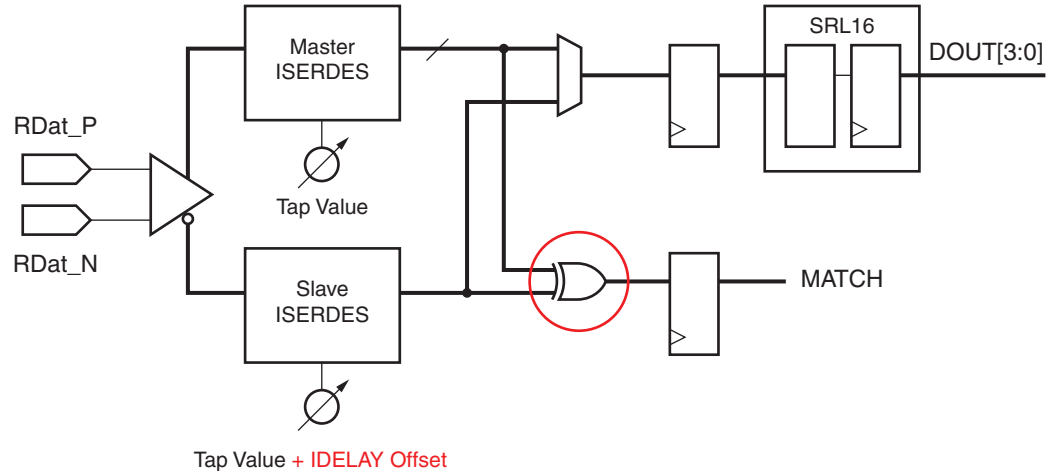
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Figure 2: **Basic DPA Logic**

As the logic traverses the IDELAY taps, the offset delay between two IDELAYs remains constant. The logic compares the sample values from the two ISERDES to determine if the sample point is in the valid data window. When both sample points are in the valid data window, the sample values match. When the sample points are near the data transition region, the sample values begin to mismatch, provided there are transitions in the data. The DPA logic accumulates all samples during a test (Alignment Test Interval) and only reports a match if all the samples matched. The match and mismatch information for each of the IDELAY tap settings is stored in memory and is then used to determine the optimal sampling point of the data eye. Figure 3 shows a sampling result captured at 400 MHz DDR (800 Mb/s).

Master Offset

Data Ch/Tap	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
0	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N
1	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M
2	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N
3	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M
4	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N
5	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N
6	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N
7	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N
8	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M
9	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N
10	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M
11	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N
12	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M
13	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N
14	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N
15	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M
16	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M

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Figure 3: **IDELAY Tap Sweep**

In Figure 3, the match and mismatch information is recorded for each sampling point (tap value) of the 17 data bits, where index 16 is the control bit. The "N" is a mismatch and "M" is a match. Based on the match and mismatch information, the optimal sampling point (green box) chosen is in the middle of the match region (data eye). The DPA logic always chooses the final optimal sampling point in the first complete data eye. As illustrated, each bit can have different data transition regions. The DPA logic aligns the optimal sampling point for each bit independently. Once all the bits are aligned to the optimal sampling point, the DPA logic initiates the word alignment process.

Word Alignment

The word alignment process removes the skew between all bits in the SPI-4.2 bus. The DPA logic aligns the 17 data bits of the SPI-4.2 interface (RDat[15:0] and RCtl) using the SPI-4.2 training pattern. Utilizing the Bitslip sub-module in the ISERDES and SRL16s, the DPA logic matches the output of the ISERDES to the training pattern and aligns all the data bits to remove bit-to-bit skew.

The assertion of [SnkDPA]PhaseAlignComplete indicates the initial alignment and word alignment have completed successfully. The alignment time between the high-to-low transition of the [SnkDPA]PhaseAlignRequest and the assertion of [SnkDPA]PhaseAlignComplete is only dependent on the RDClk frequency and the chosen alignment test interval. The approximate alignment time is:

Time ~= RDClk period * 128 * (Alignment Test Interval + 7)

Continuous Alignment

When the continuous alignment option is enabled, the continuous alignment process starts after [SnkDPA]PhaseAlignComplete is asserted. After the initial clock-data alignment, the sampling point of each data bit is aligned to the middle of the data valid window. However, in some systems, the valid data window can shift due to operating conditions (such as voltage or temperature) or other variations. The continuous alignment addresses this by performing a constant non-disruptive monitoring of the ingress data samples during normal operation and adjusting the sampling point as necessary to provide maximum margin. However, this is not typical because most SPI-4.2 transmitters (sources) have a fixed data/clock phase relationship by design.

Utilizing two ISERDES for each bit, with the Master IDELAY at the center of the data eye, the DPA logic takes Alignment Test Interval samples of the output data of the Slave IDELAY at the offset equal to Master IDELAY + 2, and then takes Alignment Test Interval samples of the output data of the Slave IDELAY at the offset equal to Master IDELAY - 2. The results of the two tests are then compared with the Master IDELAY. If the match test at one side matches and the other side does not, the valid data window has shifted or collapsed. In response to this, the Master IDELAY tap value is shifted away from the mismatched side by adjusting the tap value by ±IDELAY tap. This process is repeated continuously during the operation.

The adjustment of the Master IDELAY tap is done by first aligning the Slave IDELAY tap to the same value as the Master IDELAY tap and swapping the data output to the Slave IDELAY tap. The Master IDELAY tap is then adjusted and the output is swapped

again. This process eliminates any glitches that can occur while adjusting the tap value.

The continuous DPA monitors, and if necessary, adjusts all the bits in parallel. The adjustment opportunity (for any, or all bits) occurs periodically at a rate of:

DPA update rate ~= UI * (Alignment Test Interval * 8 + 136)

DPA Clock Adjustment (Optional)

The DPA Clock Adjustment feature should only be used if the traces for the data and control bits of the SPI-4.2 bus are closely matched. As shown in Figure 4, the DPA Clock Adjustment option inserts an IDELAY on the RDClk signal and adjusts the tap value on this IDELAY to alter the sampling point of the entire RDat/RCtl bus. This allows the core to move the sampling point of the first complete data eye to the lowest possible tap values (as described in the Initial Bit Alignment section). This effectively lowers the final IDELAY tap settings selected for the data and control bits, thus minimizing the effect of the IDELAY tap pattern jitter on system timing. The DPA Clock Adjustment logic can choose to either adjust the IDELAY on RDClk tap value downwards, or perform no adjustment at all, depending on the initial data test. Consequently, the initial clock delay should be in the middle of the IDELAY range (default is 32 for Virtex-4 and Virtex-5 FPGAs, and 16 for Virtex-6 and 7 series FPGAs) or at least at the number of IDELAY taps that correspond to 1 UI. In Virtex-6 and 7 series FPGA designs, this feature is only available when RDClk clock distribution is regional. See Figure 4.
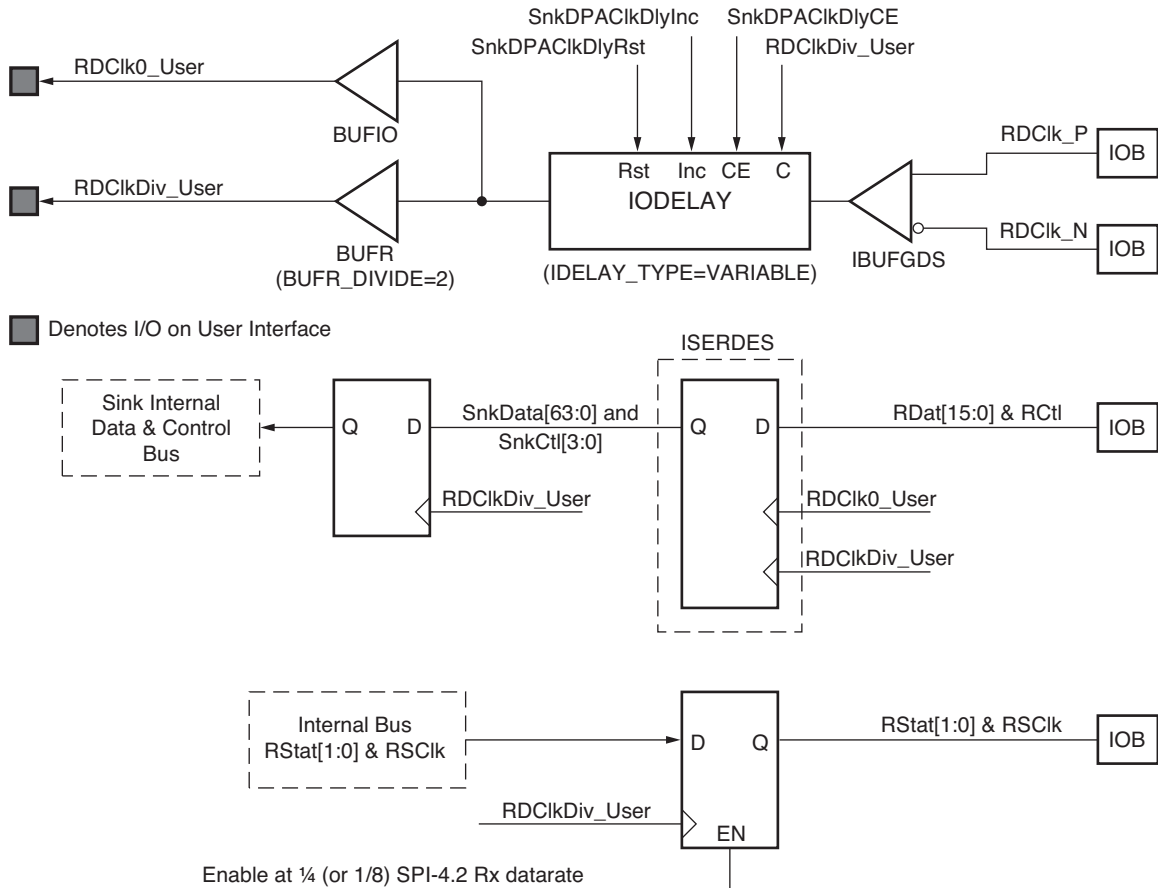
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Figure 4: **IDELAY Inserted on RDClk for DPA Clock Adjustment**

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For example, in a Virtex-6 FPGA system with an 800 Mb/s data rate, 1 UI is equivalent to 1250 ps. Each IDELAY tap offers a delay value of 78 ps, meaning 1 UI corresponds to about 16 taps at this data rate. Additionally, each tap delay can add up to ±5 ps pattern-dependent jitter.[1] As described in the Initial Bit Alignment section, the DPA logic compares the output of the Master IDELAY and ISERDES with that of the Slave IDELAY and ISERDES for each bit. Figure 5 and Figure 6 represent these comparisons using "N" as a mismatch and "M" as a match. The Dynamic Phase Alignment logic sweeps all the IDELAY tap values and then selects the final, optimal sampling point within the first complete data eye found.

The worst-case scenario IDELAY Tap Sweep example is shown in Figure 5, where the initial clock alignment (determined by board layout, with RDat/RCtl Master IDELAY tap values set to 0) falls at the very beginning of an "M" match window across all data/control bits. In this scenario, the DPA logic sweeps upwards through the data and control IDELAY tap values and finds the first complete data eye between tap values 14 and 25 for Bit 0. In this case, the DPA logic selects IDELAY tap 20 as the final sampling point for Bit 0. This selection represents a 20 tap delay difference (about 1.25 UI) between the clock sampling point and the data valid window selected. This is not necessarily an issue, but a larger final tap delay value on the data bit can contribute up to 5 ps of additional jitter per tap.

Data Ch \ Tap		Master Offset																															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M
1	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
2	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M
3	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M
4	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
5	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M
6	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M
7	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M
8	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N
9	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N
10	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N
11	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M
12	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
13	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	M
14	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M
15	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N
16	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N

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Figure 5: **Virtex-6 FPGA IDELAY Tap Sweep without DPA Clock Adjustment**

Using the same scenario, if DPA Clock Adjustment is used to change the initial clock alignment, the DPA Clock Adjustment logic decrements the tap value of the IDELAY on RDClk. This has the effect of shifting the match windows for the data/control bits to the "right," as shown in Figure 6. During the DPA Clock Adjustment phase, the tap values on each Master and Slave IDELAY on the RDat and RCtl bits do not change from their initial value (Master = 0, and Slave = Master-Slave IDELAY Offset); only the IDELAY tap value on RDClk is changed. The DPA Clock Adjustment logic continues decrementing the IDELAY on RDClk until it sees a transition from "match" across all data/control bits to "no match" across all data/control bits. This is considered the ideal starting point for per-bit DPA alignment because the first complete data eye is shifted

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1. $T_{IDELAYPAT\_JIT}$ value in DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*.

to lower IDELAY tap values. Note that because the DPA Clock Adjustment logic must see a transition to "no match" across all data/control bits, use of the Clock Adjustment option requires that the RDat and RCtl board traces are closely matched (the DPA process fails if it does not find this "no match" condition across the entire data and control bus). With this new initial clock alignment, the DPA logic sweeps upwards through the data and control IDELAY tap values and finds the first complete data eye between tap values 1 and 12 for Bit 0. The DPA logic then selects IDELAY tap 7 as the final sampling point for Bit 0. This is 13 tap delays fewer than in the previous example without DPA Clock Adjustment, for a potential jitter reduction of up to 65 ps.

Master Offset

Data Ch \ Tap	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
1	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M
2	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
3	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N
4	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N
5	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
6	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N
7	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N
8	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N
9	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N
10	N	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M
11	N	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N
12	N	N	N	M	M	M	M	M	M	M	M	M	M	M	N	N	N	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

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Figure 6: **Virtex-6 FPGA IDELAY Tap Sweep with DPA Clock Adjustment**

DPA Clock Adjustment must not be used unless there is a specific issue with data transfer. This type of issue typically manifests when the DPA completes successfully, but is followed by sporadic, though immediate, DIP4 errors during operation of the core. In these cases, the potential jitter reduction possible with the DPA Clock Adjustment feature can be useful. To evaluate the potential benefits of the DPA Clock Adjustment option in their system, users must find the actual final tap values for each implementation (with and without the Clock Adjust feature). These final tap values can be found using the DPA Diagnostics feature of the core. Based on the findings of final tap values, users can decide whether the potential jitter reduction improves their timing margin enough to reduce the number of DIP4 errors occurring.

Hardware Verification

The SPI-4.2 Dynamic Alignment Core with the default DPA parameters has been tested in hardware using the Virtex-4 FPGA ML450 Development board and the Virtex-5 FPGA ML 550 Development board, which contain XC4VLX25-FF668 and XC5VLX50T-FF1136 FPGAs respectively. The design works for data rates up to 1 Gb/s. The SPI-4.2 Dynamic Alignment core has also been tested in hardware using the Virtex-6 FPGA ML623 Development board, which contains the XC6VLX240T-FF1156-1 FPGA, up to data rates of 1.1 Gb/s. The default DPA parameters used in this design are:

Master-Slave IDELAY Offset = 2

Alignment Test Interval = 128

DPA Parameter Guidelines

The operational parameters of the DPA algorithm can be adjusted through the CORE Generator software GUI:

- Alignment Test Interval
- Master-Slave IDELAY Offset

For hardware operation, the Alignment Test Interval should be set to 128, and the Master-Slave IDELAY Offset should be set to 2 (default value) for all operating frequencies.

As previously discussed, the Alignment Test Interval determines the number of samples taken at each sample point. A large number provides more precision in detecting the transition locations of the data at the expense of longer alignment time. In general, the default value of 128 should be used. However, if the users want to simulate the core with a shorter alignment time, they can generate a simulation model with a value less than 128.

The Master-Slave IDELAY Offset determines the offset between delay tap setting for Master and Slave IDELAY and is related to the expected data eye (in IDELAY taps). The Master-Slave IDELAY Offset should be left at the default setting of 2 because larger values can cause DPA failures at high SPI-4.2 clock rates or in a noisy system.

DPA Diagnostics

If alignment issues occur during hardware operation (DIP4 Errors or Sink is out of frame), the DPA diagnostic ports can be used for debugging purposes.

If the DPA Status Monitoring option is enabled, the DPA diagnostic data is provided for the chosen SPI-4.2 bus index between the high-to-low transition of `[SnkDPA]PhaseAlignRequest` and the assertion of `[SnkDPA]PhaseAlignComplete`. The DPA diagnostic data provides the ability to monitor the data eye and the final sampling point of the initial alignment process for the chosen SPI-4.2 bus index.

The DPA logic has the following diagnostic ports: SnkBusErrStat[7:0], SnkDPARamAddr[5:0], SnkDPARamData[16:0], and SnkDPARamValid. These ports present the user with the data collected by the DPA logic while finding the valid data window for the data and control bits of SPI-4.2 bus during the initial alignment process. After the PhaseAlignRequest is pulsed, the DPA logic traverses the IDELAY tap to determine if the sampling for an IDELAY tap is within a valid window. The sampling information for each bit is captured and presented on the SnkDPARamAddr and SnkDPARamData bus when SnkDPAValid is asserted.

The `SnkBusErrStat[7:0]` bus is clocked by RDClkDiv_GP clock (output of the Sink core) during the initial alignment process. The bus reverts back to its normal function after `[SnkDPA]PhaseAlignComplete` is asserted and is clocked by SnkFFClk thereafter. The `SnkBusErrStat` bus can be connected to the ChipScope™ tool or similar logic probes to diagnose alignment failures.

The DPA diagnostics data on SnkBusErrStat[7:0] can be broken into four phases:

- DELAY tap sweep.
- Adjust tap value to middle of data eye.
- Confirm that all channels have aligned to the middle of data eye.
- Report final tap value and assert `[SnkDPA]PhaseAlignComplete`.

Figure 7 shows the first phase of the diagnostic process. In this phase, the DPA logic sweeps through the IDELAY tap to find the data eye. The SnkBusErrStat[5:0] shows the shadow counter of the IDELAY tap value that increments from 0 to 63. SnkBusErrStat[7] is asserted when the sampling point is in the valid data window. SnkBusErrStat[6] is ignored. In the example shown in Figure 7, the first complete valid data window is between IDELAY tap value (SnkBusErrStat[5:0]) 14 and 24 (in hexadecimal). The SnkBusErrStat[7] should change state as the DPA logic sweeps through the IDELAY tap.

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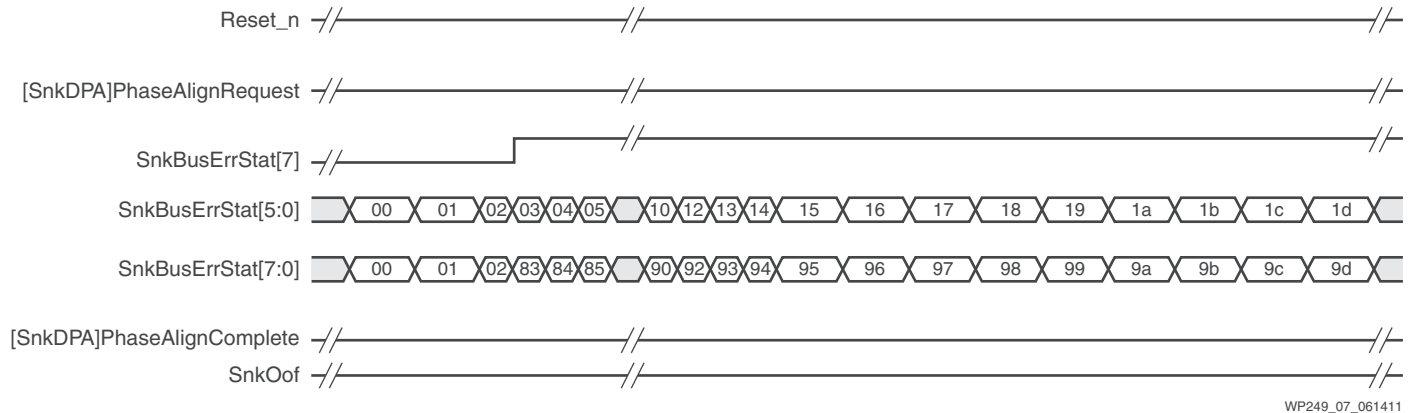
Figure 7: **DPA Diagnostics Phase 1**

If this signal does not change when SnkBusErrStat[5:0] increments from 0 to 63, it is an indication that something is wrong. Because the first phase occurs after the high-to-low transition of the [SnkDPA]PhaseAlignRequest and the assertion of ready signal (internal signal of the core) of the IDELAYCTRLs, the issue could be due to a number of things:

- [SnkDPA]PhaseAlignRequest was not pulsed correctly in the startup sequence as described in the Initializing the SPI-4.2 Core section in UG153, *LogiCORE IP SPI-4.2 v10.5 User Guide* and UG784, *LogiCORE IP SPI-4.2 v11.2 User Guide*.

- A 200 MHz clock was not connected to the SnkIdelayRefClk.

- The IDELAYCTRLs were not placed in the same clock regions as the SPI-4.2 Input pins (RDat[15:0] and RCtl).

- The SPI-4.2 data bit that the DPA logic is monitoring might be stuck at 0 or 1, or the training pattern is not being sent on this data bit.

Figure 8 shows the second phase of the diagnostic process. In this phase, the DPA logic adjusts the sampling point to the middle of the first complete data eye. The SnkBusErrStat[5:0] increments from 0 to the center tap value. The final tap (center tap) value shown in Figure 8 is 1D.
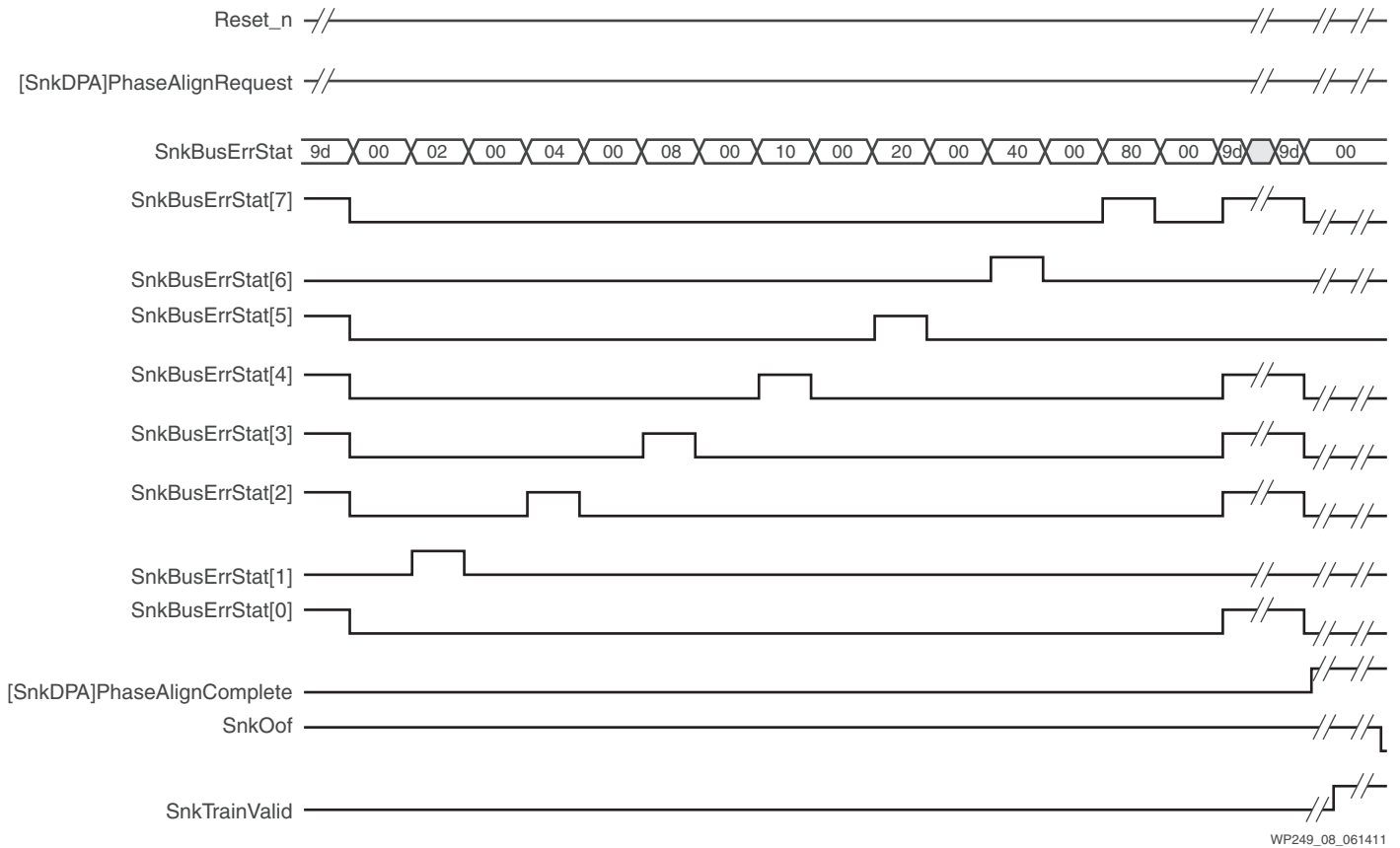
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Figure 8: **DPA Diagnostics Phase 2**

Figure 9 show the third and fourth phase of the diagnostic process. In this phase, a staircase waveform should be observed on SnkBusErrStat[7:0]. Each assertion and deassertion of SnkBusErrStat confirms that the DPA logic has aligned the IDELAY of each data bit of the SPI-4.2 interface to the data eye. For example, assertion of SnkBusErrStat[0] indicates that bit 0 has aligned to the middle of the data eye, and the following deassertion of SnkBusErrStat[0] indicates that bit 1 has aligned to the middle of the data eye.

The staircase waveform only starts at the SnkBusErrStat index that corresponds to the selected bus index. In this case, the selected SPI-4.2 bus index is 1; therefore, the pulse starts at SnkBusErrStat[1]. If the complete staircase waveform up to SnkBusErrStat[7] is not observed, the first bit that is missing a completion flag has not aligned to the data eye. For the example shown in Figure 9, if the staircase waveform stops after SnkBusErrStat[4], then the data bit that failed to align is data bit 10. The problem can be corrected by monitoring that bit through the diagnostic ports. To do this, the bit to be fixed must be specified in the CORE Generator software GUI, and the netlist must be regenerated.

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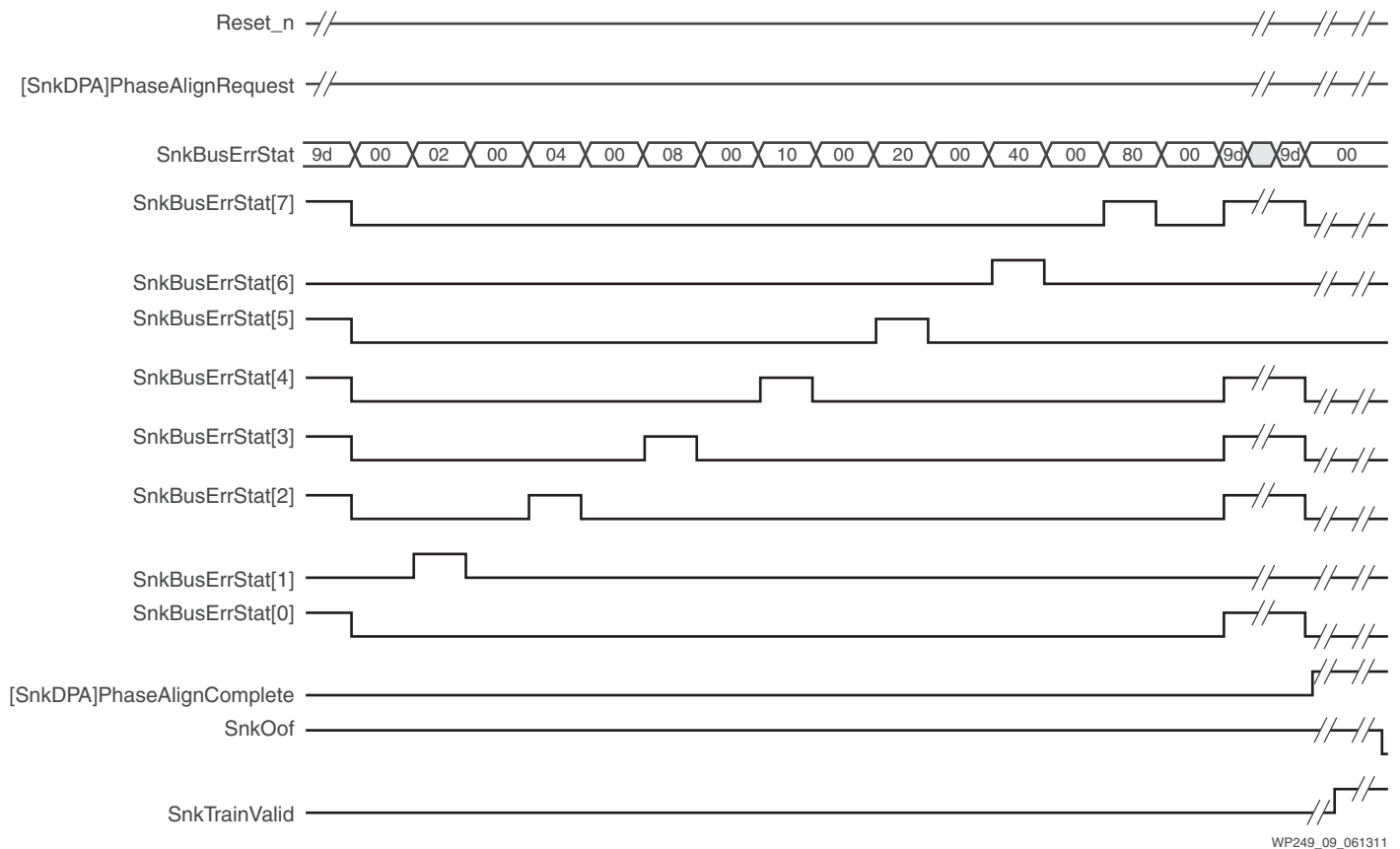
Figure 9: **Diagnostic Phases 3 and 4**

In the fourth phase, the last value 1D on SnkBusErrStat[5:0] before the
`[SnkDPA]PhaseAlignCompleted` is asserted is the final tap value centered in the
data eye of the selected SPI-4.2 data bit.

Advanced DPA Diagnostics (Optional)

This feature allows the Advance DPA Diagnostic ports to be used: SnkDPADiagWin,
SnkDPAAddrRst, and SnkdDPAAddrEn. These ports enable the user to measure and
capture the data valid window for each bit of the SPI-4.2 bus during operation. After
the SnkDPADiagWin is pulsed, the DPA performs a diagnostic sweep. This allows
windowing the data eye, using active traffic on SPI-4.2 bus. The data window
information for each bit is captured and presented on the SnkDPARamAddr and
SnkDPARamData bus when SnkDPAValid is asserted.

This feature should be used for diagnostics only because the diagnostic sweep freezes
the current sampling point regardless of continuous DPA use. The DPA RAM contents
can be accessed by resetting (asserting SnkDPARamRst) the DPA RAM address
counter, and then incrementing (asserting SnkDPARamAddrEn) the DPA RAM
address counter.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/27/06	1.1	Initial Xilinx web release.
10/01/09	1.2	Updated with Virtex-6 FPGA information.
07/06/11	1.3	Updated with 7 series information. Updated `PhaseAlignComplete` to `[SnkDPA]PhaseAlignComplete` throughout document. Updated DPA Operation Overview, DPA Clock Adjustment (Optional)—including the addition of Figure 4 and updating including Figure 5 and Figure 6, Hardware Verification, and DPA Diagnostics.

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